BSM-8800A
BSM-8800J
BSM-8800K

MU-881RA
MU-881RJ
MU-881RK

VD-881RA
VD-881RJ
VD-881RK

RY-881PA

AC-800PA
AC-800PJ
AR-800PA
AW-800PA
AP-800PA
AH-800PA
AE-800PA
AL-800PA
AP-851PA
AP-860PA
AG-800PA
AG-820PA
AG-830PA
ZR-800P
ZB-810PK
ZB-820PK
ZB-821PK
ZB-860PK

Life Scope 14
BEDSIDE MONITOR
BSM-8800

0634-000148F

CONTENTS

Section 1 INTRODUCTION

1-1 General

This service manual consists of information needed to service the Bedside Monitor, BSM-8800J/K, manufactured by Nihon Kohden Corporation.

For easy maintenance, the monitors provide a SELF CHECK PROGRAM system. This system continuously checks the condition of each circuit even when the monitor is operating. If there is any trouble in a circuit, an error code message is displayed on the screen.

To familiarize yourself quickly with the functions, a series of functional block diagrams and explanations have been provided.

NOTE

There is a separate service manual for the input box JA-860/880P.

The major differences between the various models are as follows:

Model	AC power requirement	Safety standard
MU-881RJ VD-881RJ (BSM-8800J)	110–125 V	(IEC)
MU-881RK VD-881RK (BSM-8800K)	220–240 V	(IEC)

1-2 Specifications

◆ Display

CRT	14 inches, colored
Waveform display method	Non-fade, moving method
Number of waveform traces	8 traces max.
Sweep speed	30 mm/sec.
Sweep time	6 sec.

◆ Display waveform

ECG1, ECG2, BP1, BP2, BP3, BP4, respiration, thermodilution waveform, CO_2 waveform, EEG1, EEG2, pulse waveform, external input

◆ Numerical data display

Heart rate, VPC rate,
BP1 (systolic, diastolic and mean)
BP2 (systolic, diastolic and mean)
BP3 (systolic, diastolic, or mean)
BP4 (systolic, diastolic, or mean)
NIBP (systolic, diastolic and mean)
respiration rate, T1, T2, ΔT, Tb
$ETCO_2$, SpO_2, ST level, O_2

◆ Trendgraph

Items	Heart rate, VPC rate, respiration rate apnea (time and frequency) BP1 to 4 (systolic, diastolic and mean) NIBP (systolic, diastolic and mean) T1, T2, Tb, $ETCO_2$, SpO_2, ST level, O_2
Event mark	Asystole, V.Fib, V.Tachy, VPC run, couplet, noise/measure off
Trend time	1 hour, 2 hours, 4 hours, 8+1 hours, and 24+1 hours

◆ Alarm

Alarm items	Vital signs alarm (high/low): Heart rate, respiration rate BP1 to BP4 (systolic, diastolic and mean) NIBP (systolic, diastolic and mean) T1, T2, ΔT, Tb $ETCO_2$, SpO_2, O_2 Apnea alarm Arrhythmia alarm External instrument alarm
Alarm indication	Vital signs or arrhythmia message is reverse shaded and an alarm tone sounds
Alarm suspend	Available (for a specified period of time)

◆ ECG measurement

ECG leads (AC-800P)	5-electrode lead ECG1: Ⅰ, Ⅱ, Ⅲ, aVR, aVL, aVF, V, MCL ECG2: Ⅱ (fixed) 3-electrode lead ECG1: Ⅰ, Ⅱ, Ⅲ ECG2: not available
ECG leads (ZB-810P)	Single-lead
ECG leads (ZB-820P)	Dual-lead
ECG leads (ZB-860P)	Ⅰ, Ⅱ, Ⅲ lead selectable
Defibrillation discharge protection	Provided
ESU interference filter	Provided
Pacing pulse limiter circuit	Provided
Filter	Diagnosis/monitoring selection In monitoring mode: drift rejection on/off and AC filter on/off are available
Frequency response	AC-800P: 0.05 to 100 Hz (diagnosis) 0.3 to 40 Hz (monitoring) Transmitter: 0.4 to 40 Hz
External output sensitivity	1 V/mV ±5%
Heart rate counting range	12 to 300 bpm
Alarm limits	High limit: 10 to 300 bpm Low limit: 5 to 295 bpm Asystole time: selection

◆ Respiration measurement

Measuring method	Impedance method or thermistor method
Respiration rate counting range	0 to 150 bpm
Alarm limits	High: 2 to 150 bpm
	Low: 0 to 148 bpm
	Apnea time: 10 to 40 seconds in 5 second steps

◆ Blood pressure measurement (invasive method)

Measuring range	−50 to +300 mmHg
Input sensitivity	50 μV/V/10 mmHg
BP waveform display scale	Common scale for BP1 to BP4
	Separate scale:
	2 scale for BP1 and BP2 to BP4
	4 scale for BP1 to BP4 respectively
Display value	Systolic/diastolic/mean pressure of each BP channel
Alarm limits	Available for each pressure
	High: 2 to 300 mmHg
	Low: 0 to 298 mmHg
External output sensitivity	1 V/100 mmHg (BP1 only)
BP site label	AP, LAP, PAP, CVP, and ICP

◆ Temperature measurement

Thermistor probe	YSI-400 series
Measuring range	0 to 45 °C (hardwire system)
	5 to 45 °C (telemetry system ZB-860P)
Number of channels	2
Alarm limits	High: 0.5 to 45.0 °C
	Low: 0 to 44.5 °C

◆ Cardiac output measurement

Measuring method	Thermodilution method
Measuring range	0.5 to 20 L/min
Measuring condition	Injection temperature: 0 to 25 °C
	Blood temperature: 15 to 45 °C
	Catheter size: 5F or 7F
	Injection volume: 3 cc, 5 cc, 10 cc (7F)
	1 cc, 2 cc, 3 cc, 4 cc, 5 cc (5F)
	Catheter coefficient can be used
Injection temperature measurement method	Temperature probe or inline sensor
Alarm limits (Tb)	High: 15.5 to 45.0 °C
	Low: 15.0 to 44.5 °C

◆ EEG measurement

Number of channels	2
Display sensitivity	10 mm/100 μV ±10 % (×1) ×0.5, ×1, ×2, ×4
Defibrillator discharge protection	Provided
Frequency response	0.5 to 20 Hz

◆ SpO_2 measurement

Measuring range	50 to 100 %, in 1 % step
Measuring accuracy	80 % ≦ SpO_2 ≦ 100 %: ±2 % 50 % ≦ SpO_2 < 80 %: ±3 %
Alarm limits	High: 51 to 100 % Low: 50 to 99 %

◆ Non-invasive blood pressure measurement

Measuring method	Oscillometric
Display value	Systolic, diastolic, mean pressure
Pressure display range	AP-851PA (adults/children): 10 to 300 mmHg AP-851PA (neonates): 5 to 200 mmHg AP-860PA: 0 to 290 mmHg
Accuracy	AP-851PA: ±4 mmHg AP-860PA: ±3 mmHg (0 to 150 mmHg) ±2 mmHg (150 to 290 mmHg)
Measuring range	AP-851PA (adults/children) Systolic: 60 to 260 mmHg Mean: 45 to 235 mmHg Diastolic: 40 to 220 mmHg AP-851PA (neonates) Systolic: 40 to 180 mmHg Mean: 35 to 155 mmHg Diastolic: 20 to 140 mmHg AP-860PA Systolic: 50 to 260 mmHg Mean: 40 to 240 mmHg Diastolic: 20 to 220 mmHg
Activation of measurement	Manual Continuous: 5 minutes Automatic: 1, 2.5, 5, 10, 15, 30, 60 minute interval, OFF
Safety	Cuff pressure limiter: >301 mmHg (AP-851PA) >300 mmHg (AP-860PA) Rapid deflation in case of power failure
Alarm limits	High: 15 to 260 mmHg Low: 10 to 255 mmHg

◆ CO_2 measurement

Measuring range	0 to 100 mmHg, in 1 mmHg step
Accuracy	0 mmHg ≦ CO_2 ≦ 70 mmHg: ±2 mmHg
	70 mmHg < CO_2 ≦ 100 mmHg: ±5 mmHg
CO_2 curve display scale	20 mmHg, 40 mmHg, 80 mmHg
Alarm limits	High: 12 to 100 mmHg
	Low: 10 to 98 mmHg

◆ O_2 measurement

Measuring range	0 to 100 %, in 1 % step
Accuracy	±3 % (when calibrated with air)
	±2 % (when calibrated with 100 % O_2 gas)
Alarm limits	High: 1 to 100 %
	Low: 0 to 99 %

◆ Arrhythmia recall

VPC detection method	Software algorithm (template matching method)
VPC counting range	0 to 99 beats/minute
	0 to 9999 beats/hour
Arrhythmia alarm	Asystole, V.Fib, V.Tachy, VPC run, couplet, bigeminy, early VPC, and Freq.VPC
Recall display mode	Recall waveform with event history, HR trend or VPC rate trend
Number of recall files	32 (ECG1 only)
	16 (ECG1 + ECG2 or ECG1 + P1)
Storage time per file	8 seconds

◆ Interbed function

Review of another patient for alarm contents, waveform and vital signs

◆ ST level

Number of recall files	7 files (8 waveforms/file)
Trend time	8+1 hours, 24+1 hours
	1 hour, 2 hour, 4 hour

◆ Vital signs list

Items	Heart rate, VPC rate, respiration rate
	BP1, BP2 (systolic, diastolic and mean)
	BP3, BP4 (mean)
	NIBP (systolic, diastolic and mean)
	SpO_2, $ETCO_2$, T1, T2, Tb
Number of lists	120

◆ Hemodynamics list

Items	HR, CO, CI, ASP, ADP, AMP, PASP, PADP, PAMP, PCWP, CVP, SVI, LSWI, SVRI, PVRI, RSWI, RPP, CPP
Number of lists	16

◆ External output

Analog output	ECG connector (front panel): ECG1 BP1 connector (front panel): BP1 CNS or WS connector (rear panel): ECG1, ECG2, BP1, BP2, BP3, BP4, respiration, EEG1, EEG2, CO_2, external input (8 channels are available)
Logic output	CNS connector (rear panel): Alarm, ECG measure ON/OFF
RS-232C interface	RS232C connector (rear panel): Output to the personal computer

◆ Power requirement

Line voltage	MU-881RA, VD-881RA: 117 V AC, 60 Hz MU-881RJ, VD-881RJ: 110, 117, 125 V AC, 50/60 Hz MU-881RK, VD-881RK: 220, 240 V AC, 50/60 Hz
Power consumption	MU-881R: 120 VA (max.) VD-881R: 170 VA (max.)

◆ Environment

Operating temperature	5 – 40 °C 10 – 35 °C (CO_2 sensor)
Operating humidity	30 – 90 % RH

◆ Safety standard

MU	IEC601-1, class I, type BF (AG-800PA, AG-820PA, AP-851PA, AL-800PA), type CF (others)
VD	IEC601-1, class I, type B
Transmitter	IEC601-1, type CF

◆ Dimensions and weight

MU	361 W × 200 H × 400 D mm, 18 kg
VD	370 W × 350 H × 430 D mm, 25 kg
RY	320 W × 50 H × 85 D mm, 0.8 kg

◆ Transmitter

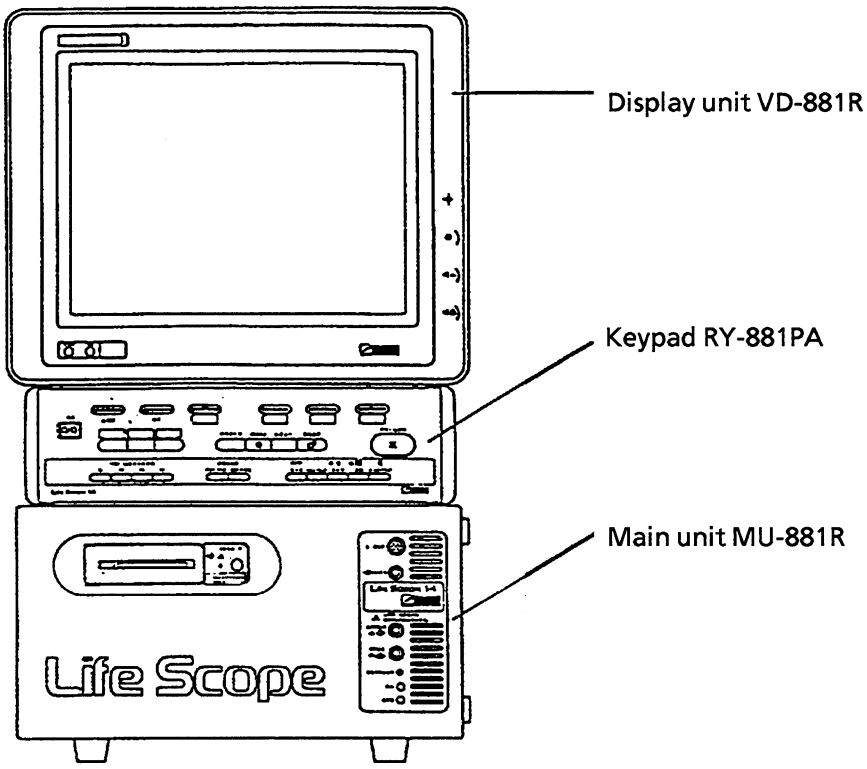
Transmitter frequency	420 to 450 MHz, 12.5 kHz step
	Group J1: 420.0500 to 421.0375 (80 ch)
	Group J2: 424.4875 to 425.9750 (120 ch)
	Group J3: 429.2500 to 429.7375 (40 ch)
	Group J4: 440.5625 to 441.5500 (80 ch)
	Group J5: 444.5125 to 445.5000 (80 ch)
	Group J6: 448.6750 to 449.6625 (80 ch)
Transmission power	0.3 mW (ZB-810P, ZB-820P)
	0.4 mW (ZB-860P)
Modulation method	FSK

◆ Receiver

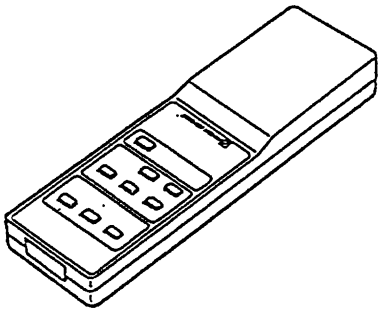
Antenna	Space diversity
Reception frequency	Synthesizer method
	420 to 450 MHz
EMI radiation	4 nW max.

1-3 Panel Explanation

1-3-1 Bedside Monitor, BSM8800

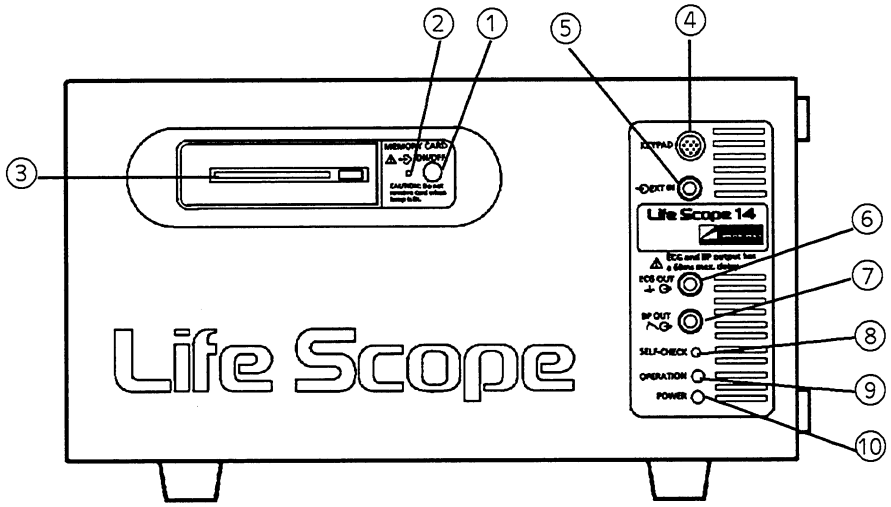


Remote controller RY-001PK

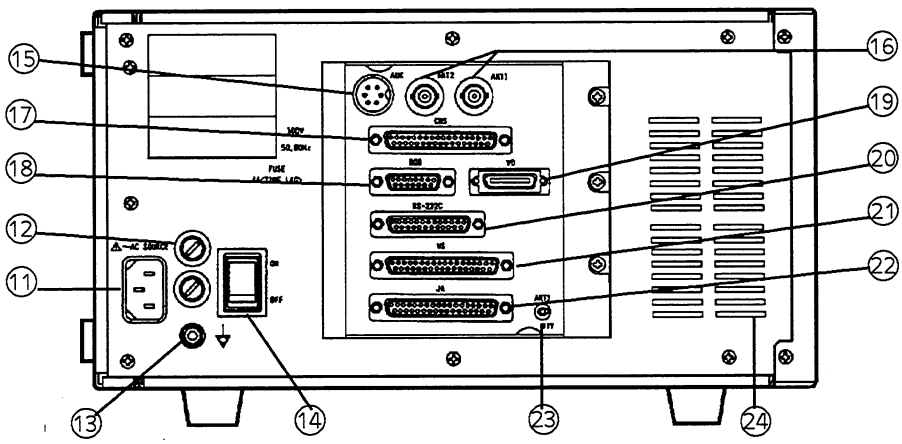


1-3-2 Main Unit, MU-881R

Front

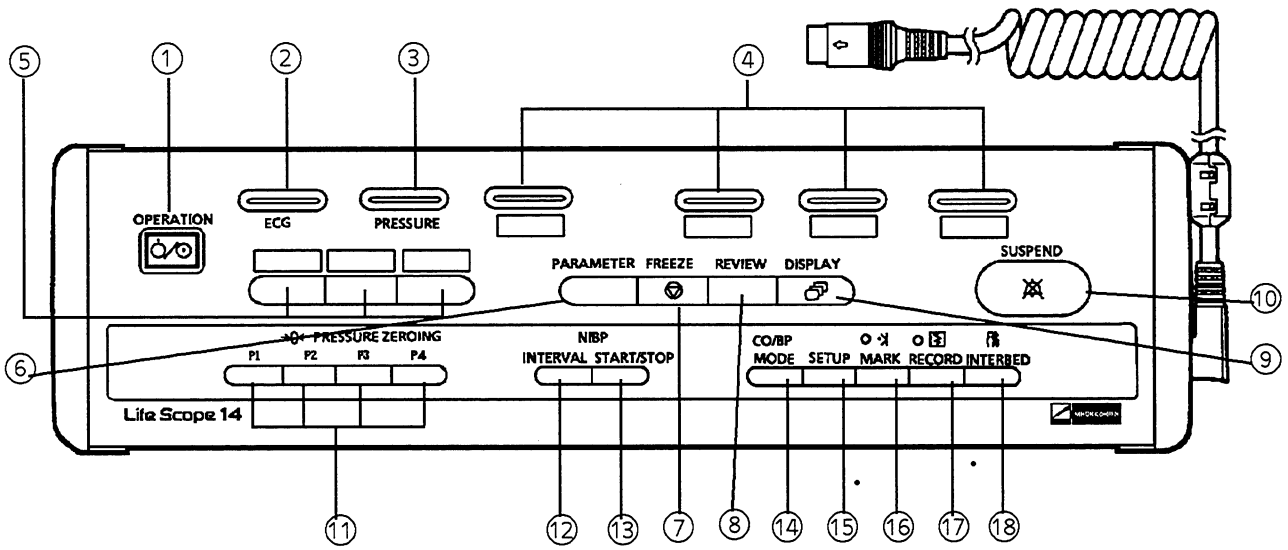


Rear



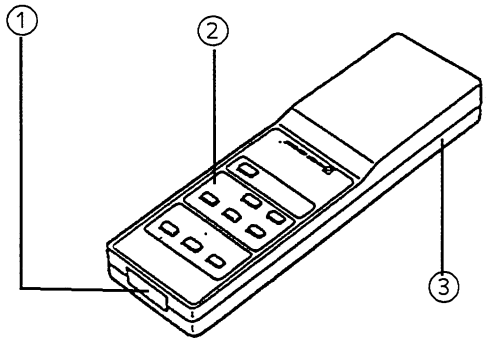
Name	Name
① Memory card switch*	⑬ Equipotential
② Memory card lamp*	⑭ Power switch
③ Memory card slot*	⑮ AUX connector
④ Keypad connector	⑯ ANT1, ANT2 connector
⑤ EXT INPUT connector	⑰ CNS connector
⑥ ECG1 output connector	⑱ RGB output connector
⑦ BP1 output connector	⑲ VD connector
⑧ Self check key	⑳ RS-232C connector
⑨ Power indication lamp	㉑ WS connector
⑩ Main power indication lamp	㉒ JA connector
⑪ AC inlet	㉓ DIV/ANT selection switch
⑫ Fuse holder	㉔ Ventilator

1-3-3 Keypad, RY-881PA

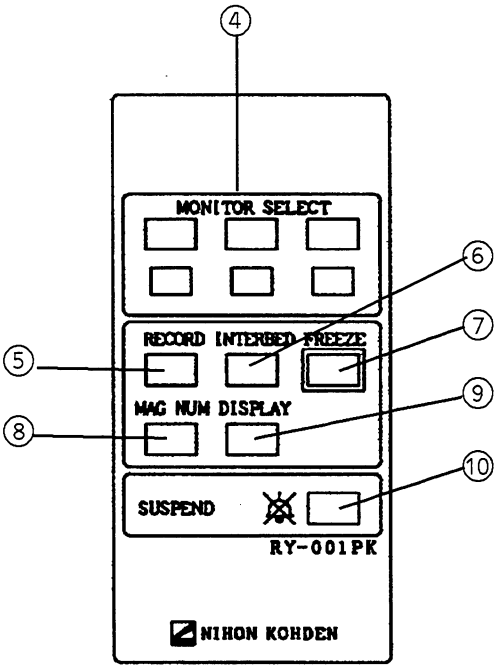


Name	Name
① Power switch	⑩ SUSPEND key
② ECG key (Multi-function key)	⑪ PRESSURE ZEROING keys
③ BP key (Multi-function key)	⑫ NIBP INTERVAL key
④ Multi-function keys 3 to 6	⑬ NIBP START/STOP key
⑤ Universal keys	⑭ CO/BP MODE key
⑥ PARAMETER key	⑮ SETUP key
⑦ FREEZE key	⑯ MARK key
⑧ REVIEW key	⑰ RECORD key
⑨ DISPLAY key	⑱ INTERBED key

1-3-4 Remote Control, RY-001PK

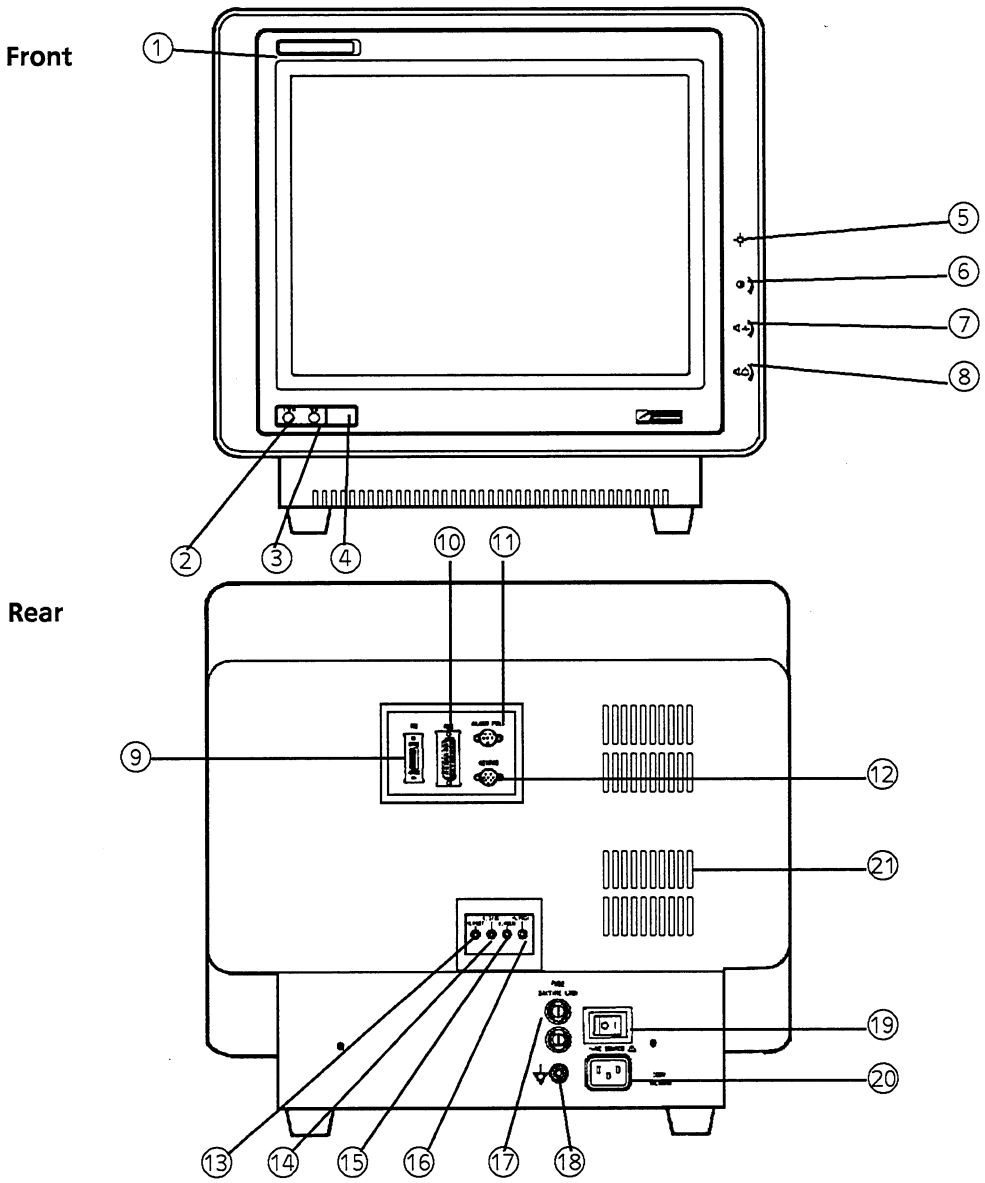


Operation panel



Name
① Signal emitter
② Operation panel
③ Battery cover
④ Monitor select key
⑤ RECORD key
⑥ INTERBED key
⑦ FREEZE key
⑧ Large measurement data display key
⑨ DISPLAY key
⑩ SUSPEND key

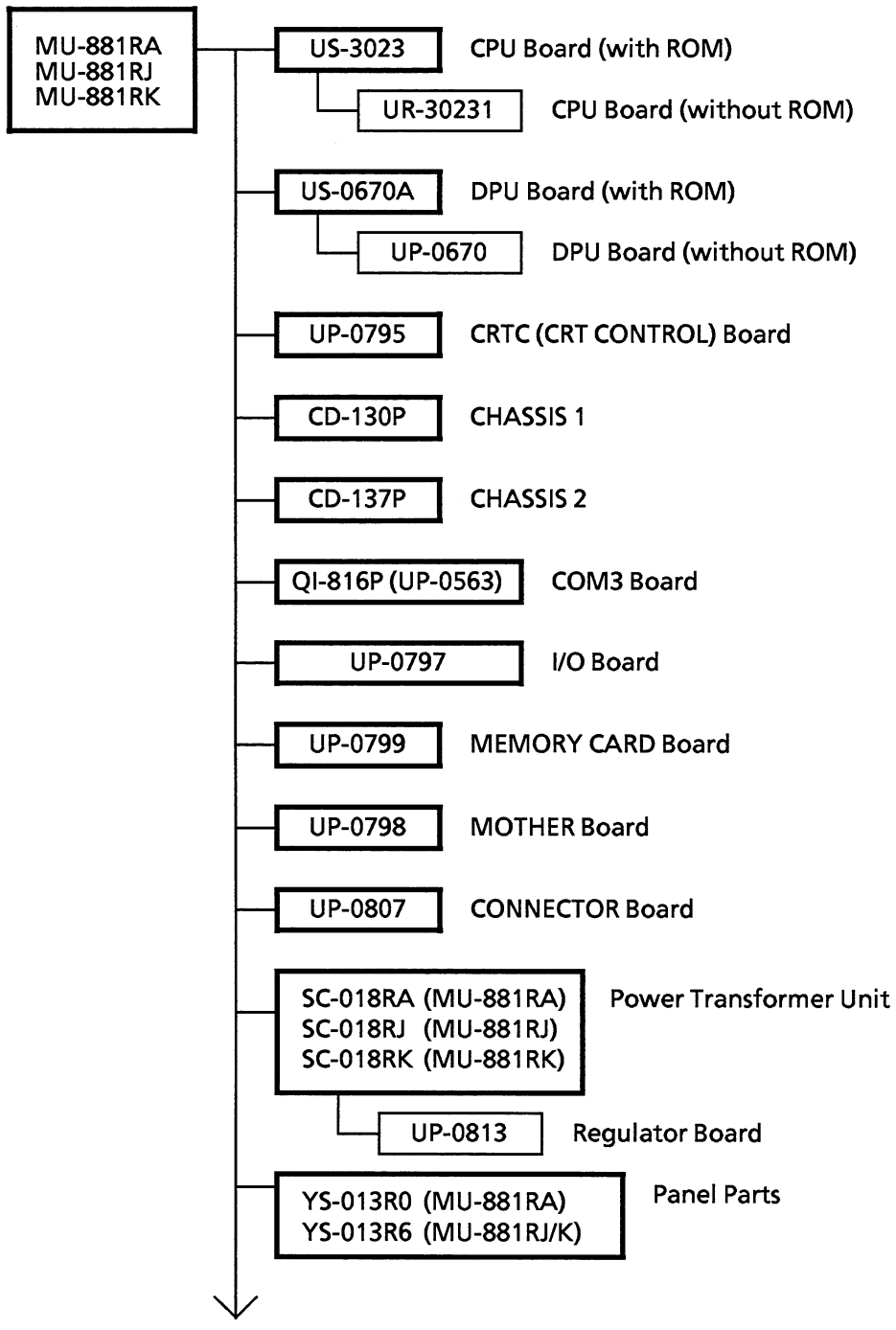
1-3-5 Display Unit, VD-881R

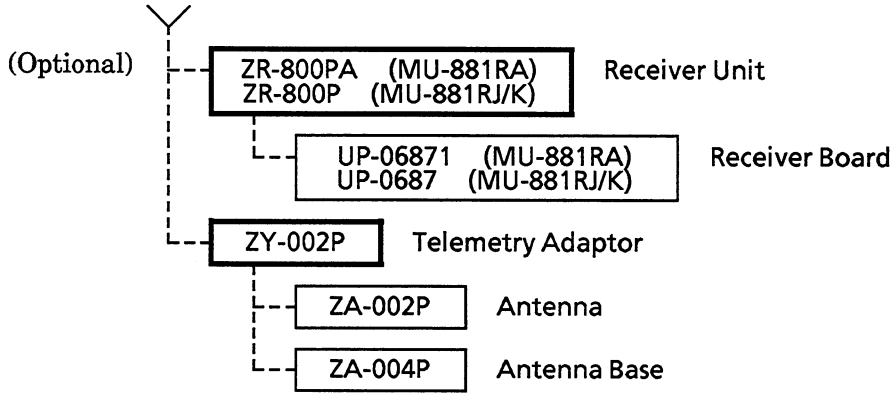


Name	Name
① Remote controller label position	⑫ Keypad connector
② Main power indication lamp	⑬ Vertical position control setting
③ Power indication lamp	⑭ Vertical amplitude control setting
④ Remote control sensor	⑮ Vertical synchronism control setting
⑤ Brightness control setting	⑯ Horizontal position control setting
⑥ Contrast control setting	⑰ Fuse holder
⑦ Synchronous sound control setting	⑱ Equipotential
⑧ Alarm volume control setting	⑲ Power switch
⑨ VD connector	⑳ AC inlet
⑩ VIDEO connector	㉑ Speaker
⑪ Alarm pole connector	

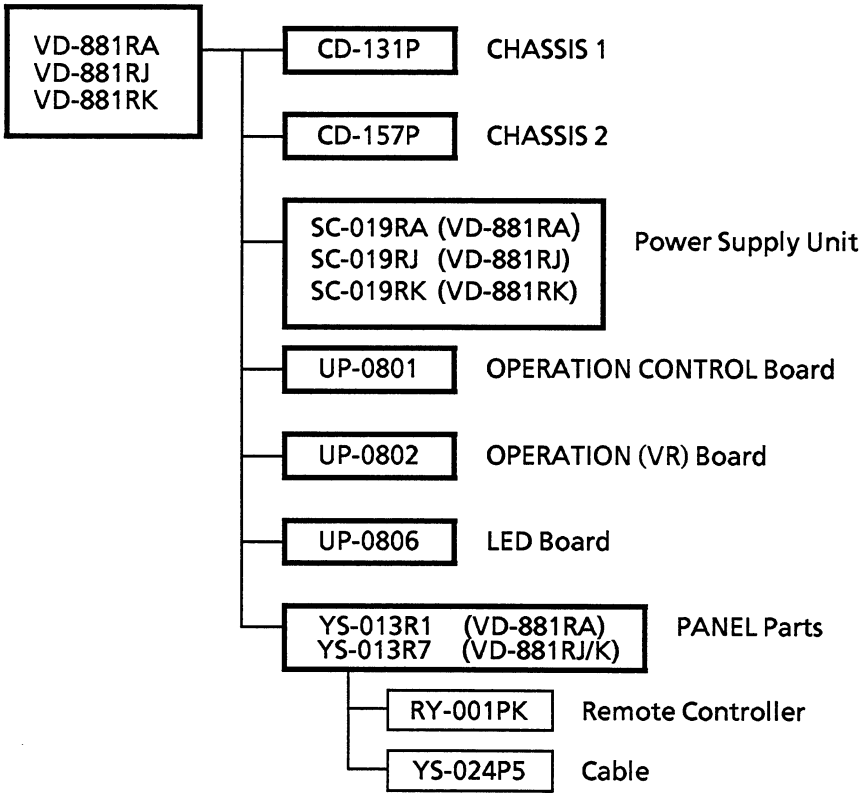
1-4 Composition

1-4-1 Main Unit

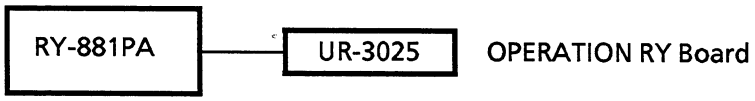




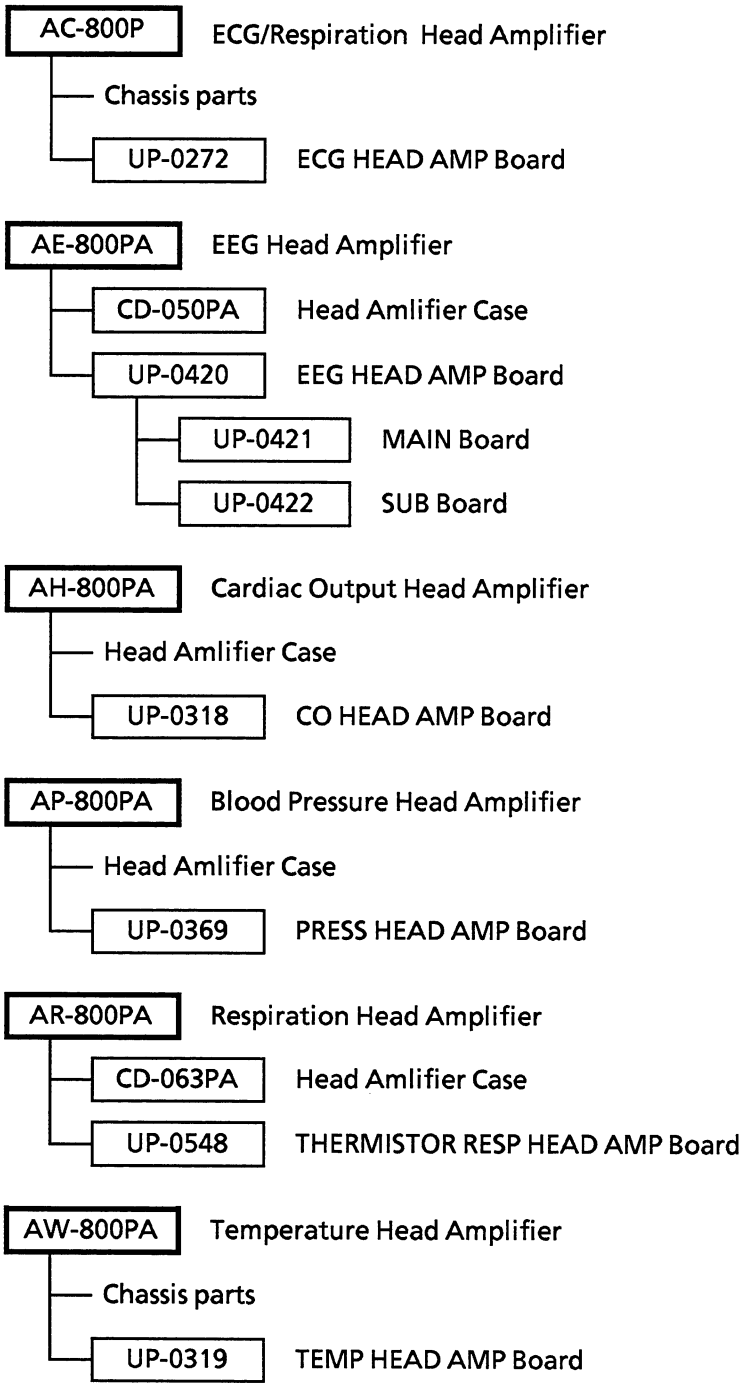
1-4-2 Display Unit

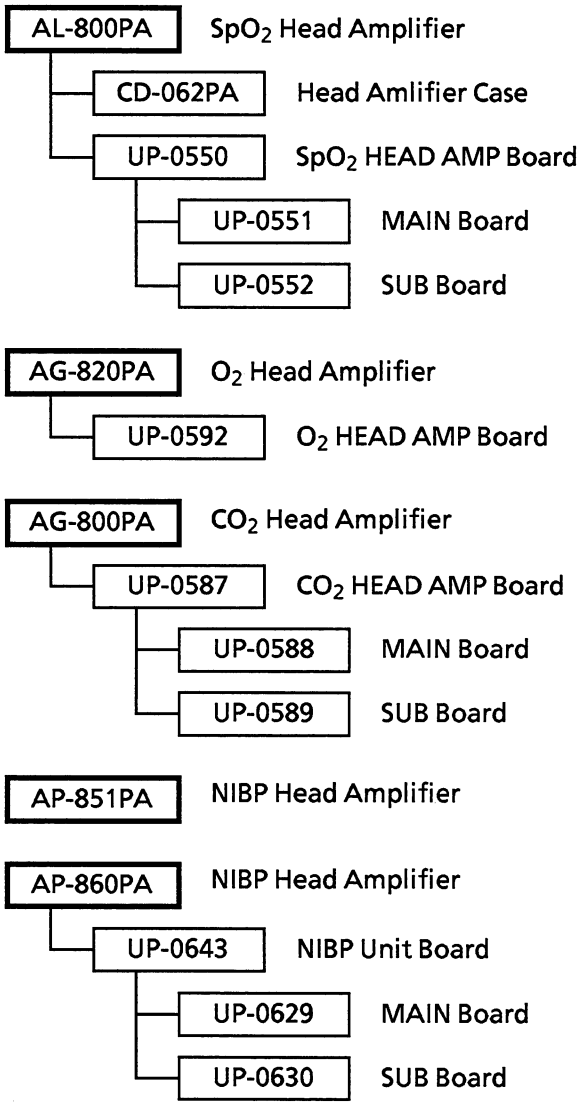


1-4-3 Keypad



1-4-4 Head Amplifiers





1-4-5 Blank Unit

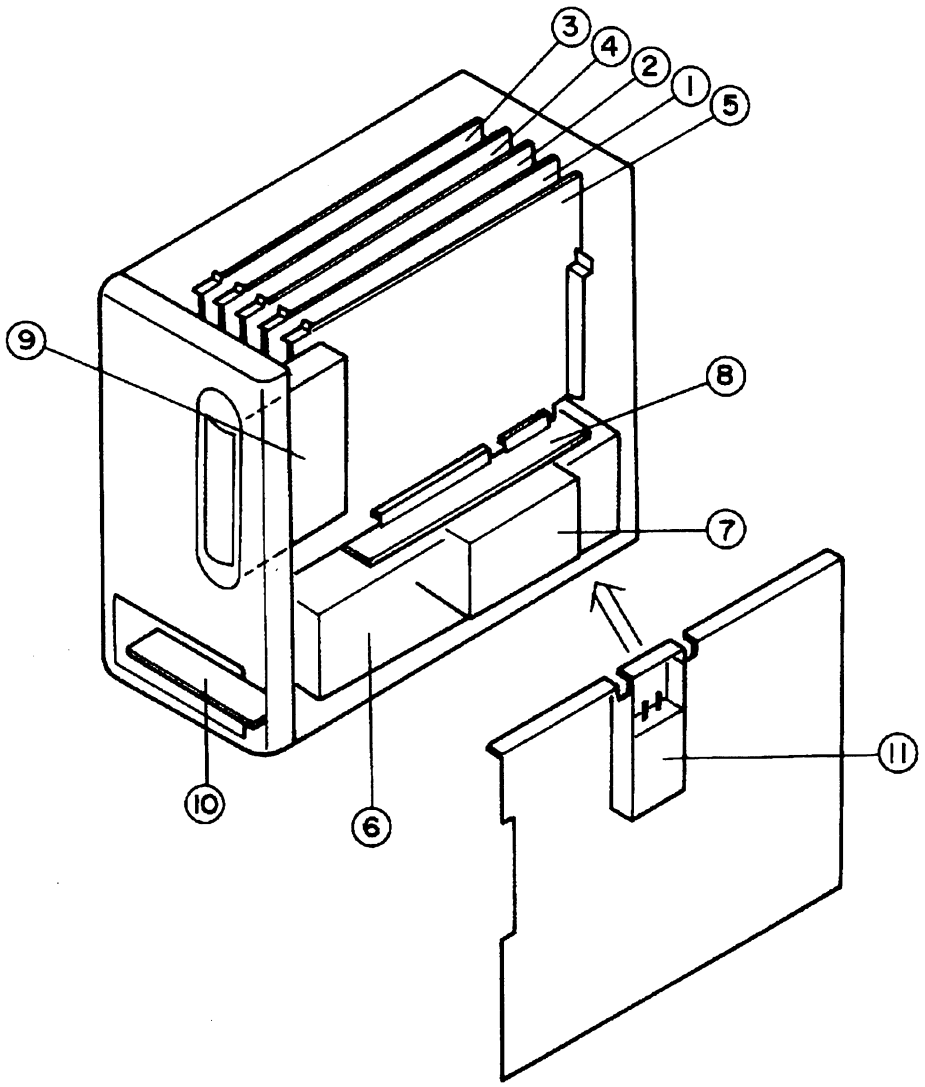
EK-800P

1-4-6 Extension Board

UP-0278 (for UP-0563/0670/0795/0797, UR-3027 in main unit, MU-881R)

1-5 Location

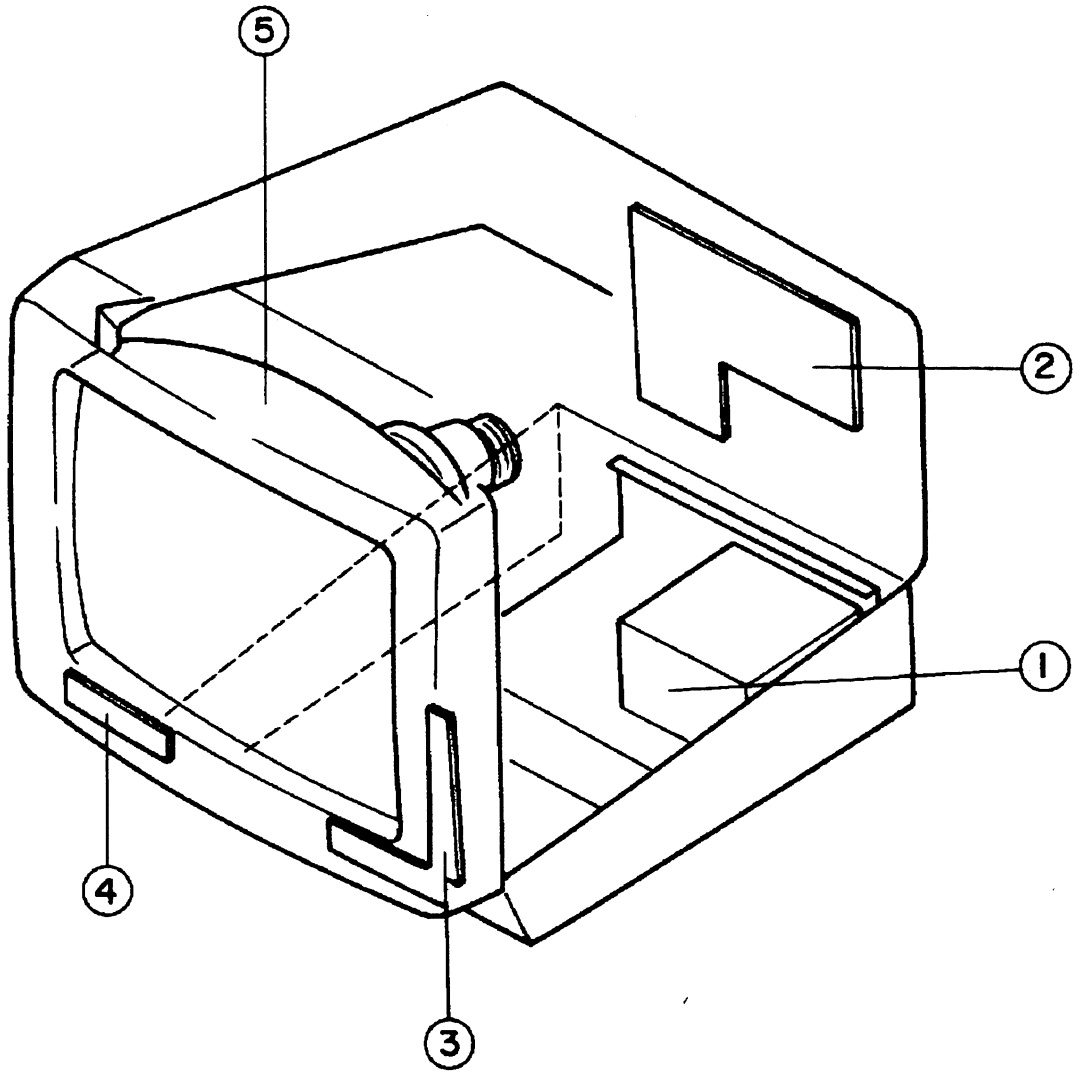
1-5-1 Main Unit, MU-881R



No.	Description	Model
①	CRTC BD (Red ejector)	UP-0795
②	CPU BD (Yellow ejector)	UR-3027
③	DPU BD (Green ejector)	UP-0670
④	COM3 BD (Black ejector)	QI-816P (UP-0563)
⑤	I/O BD (White ejector)	UP-0797
⑥	REGULATOR UNIT	UP-0813

No.	Description	Model
⑦	P.TRANSFORMER UNIT	SC-018R
⑧	MOTHER BD	UP-0798
⑨	MEMORY CARD BD	UP-0799
⑩	FRONT CONNECTOR BD	UP-0807
⑪	RF RECEIVER UNIT (Optional)	ZR-800P

1-5-2 Display Unit, VD-881R



No.	Description	Model
①	POWER SUPPLY UNIT	SC-019R
②	OPERATION CONT. BD	UP-0801
③	VR BD	UP-0802
④	LED BD	UP-0806
⑤	CRT UNIT	

1-6 System Block

The bedside monitor main unit consists mainly of the following boards and units.

- **CPU Board, UR-3027**

The master micro processing unit 68000 is responsible for the whole operation of the bedside monitor. The CPU board not only controls communication with the external units, such as, SOUND (SpO_2 tone) and RS-232C, but also, controls the BSM DPU board and the COM 3 board through their global memory. The CPU board controls the Recorder Unit through the dual-port RAM on the COM 3 board.

- **COM 3 Board, UP-0563**

The slave micro processing unit 8085 on this board controls the communication with the Central Monitor.

- **DPU Board, UP-0670**

The slave micro processing unit 68000 controls the conversion of vital-sign information received from the Input Box, Receiver Unit, and Signal Exchanger, to digital format data for the master micro processing unit. It also converts the digital waveform data to analog waveform data in real time processing.

- **I/O Board, UP-0797**

The single chip CPU on the I/O board controls the generation of the SpO_2 tone, and the Power Supply Unit. The I/O boards also controls the communication with the Display Unit and the Keypad. The Memory Card Interface unit in the I/O board allows communication between the bedside monitor and the memory card. The I/O board provides the communication port for the Signal Exchanger and Central Monitor.

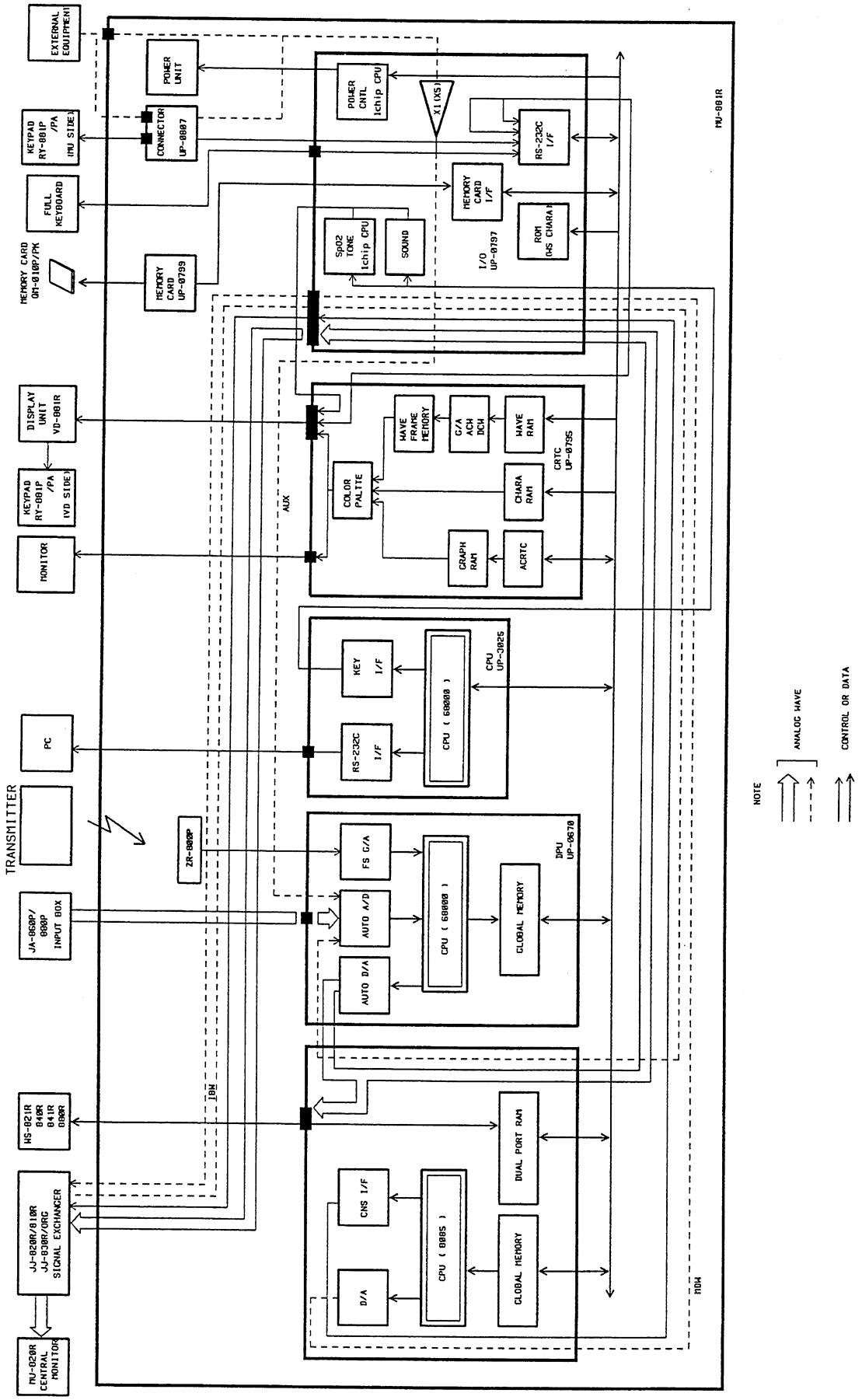
- **CRTC Board, UP-0795**

The CRTC board converts the waveform data, graphic data and character data into video image signals for the Display Unit.

- **Power Transformer Unit, SC-018R**

This unit supplies the power for the individual boards and the fan in the Main Unit, Receiver Unit, Input Box, and Keypad.

System Block Diagram



1-7 Signal Flow

1-7-1 General

The bedside monitor is divided into three major categories, of which they are further sub–divided as follow :

1) Analog Signal Flow

- Input Waveform

Analog signals (ECG, respiration, blood pressure, etc) from the Input Box are converted to digital signals. These digital signals are stored in the DPU board.

- Real-time waveform

The digital waveform signal is converted to analog waveform signal in real-time on the DPU board. The waveform analog signal is then sent to the Central Monitor.

- Delayed ECG Waveform

The ECG waveform for the Central Monitor for remote recording is not done on real-time. There is a delay for the COM 3 board to process the digital ECG signals for the Central Monitor.

- Interbed Waveform

The interbed waveform is the selected ECG waveform of the selected bed. The interbed waveform is then processed in the DPU board.

- Auxiliary Unit

The analog signal from auxiliary unit can be connected to the Main Unit with some changes to the configuration of the Setup.

2) Telemetry Signal Flow

The telemetry serial signal received through the Receiver Unit (optional) is converted to parallel signal by the frame sync gate array on the DPU board.

3) Display Data Signal Flow

- Waveform Data

The CPU board selects the waveform data for display from the processed waveform data received from the DPU board. The selected waveform data is loaded to the WAVE RAM on the CRTC board. The selected waveform data read out by the WAVE RAM is gated by the gate array ACW,DCW to the WAVE FRAME MEMORY for conversion to dot image signals. These dot image signals are color palette coded to form R, G, B signals.

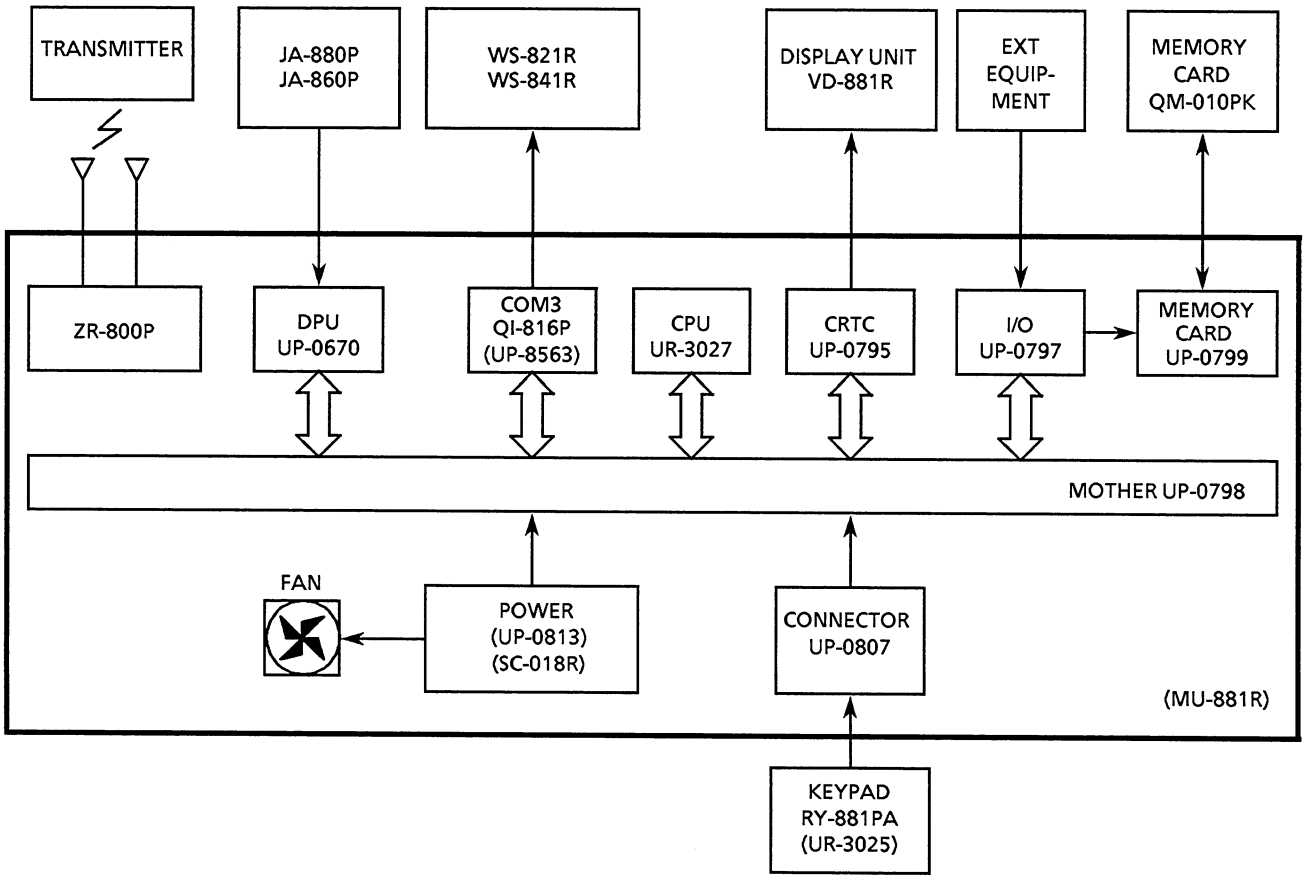
- Graphic Data

The graphic data is loaded to the Graphic RAM through the ACRTC on the CRTC board. The graphic data is read out from the GRAPHIC RAM as dot image signals which are then color palette coded to form R, G, B signals.

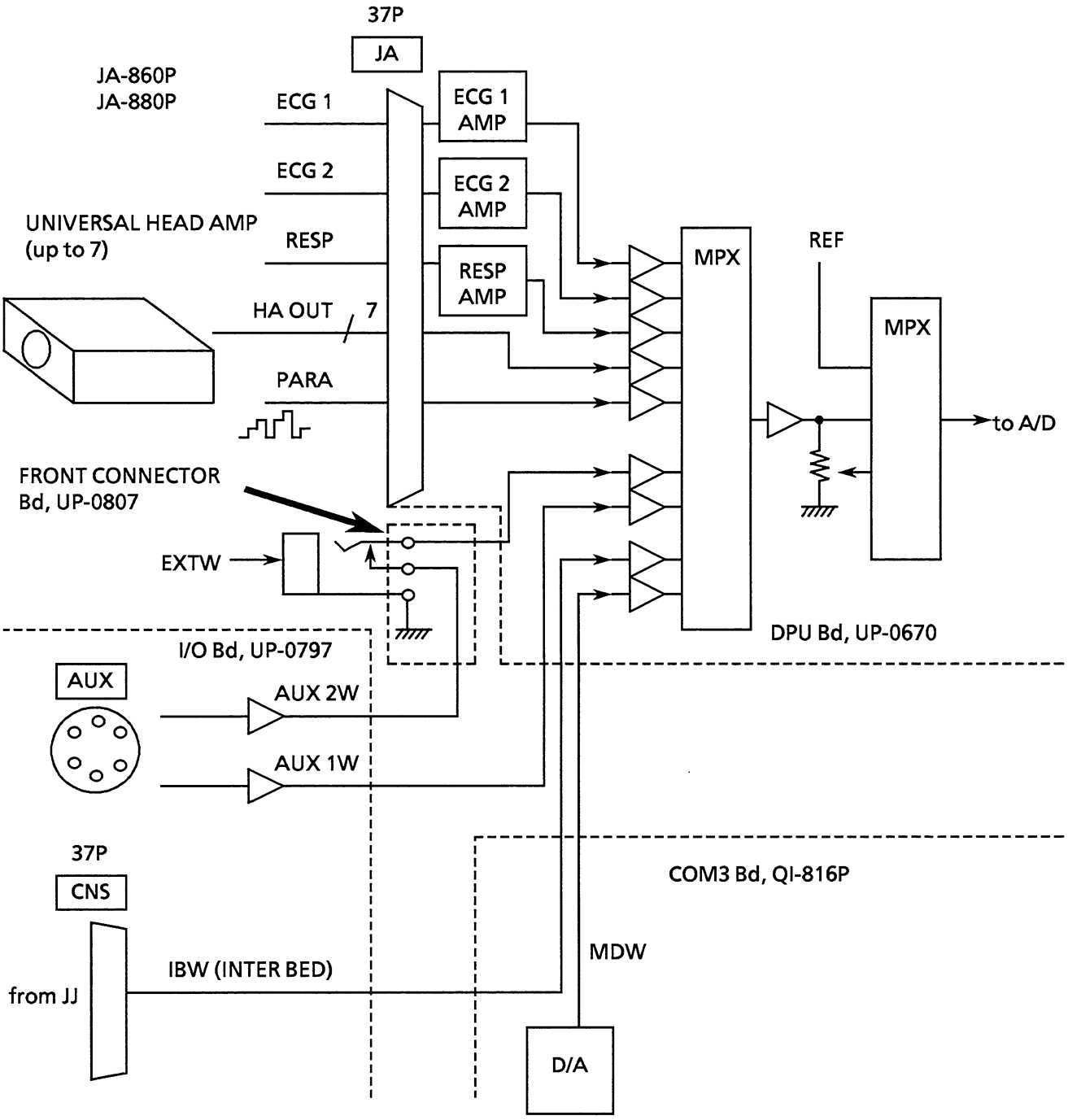
- Character Data

The character is loaded to the CHARACTER RAM on the CRTC board. The character data is read out from the CHARACTER RAM as dot image signals which are then color palette code to form R, G, B signals

System Signal Flow

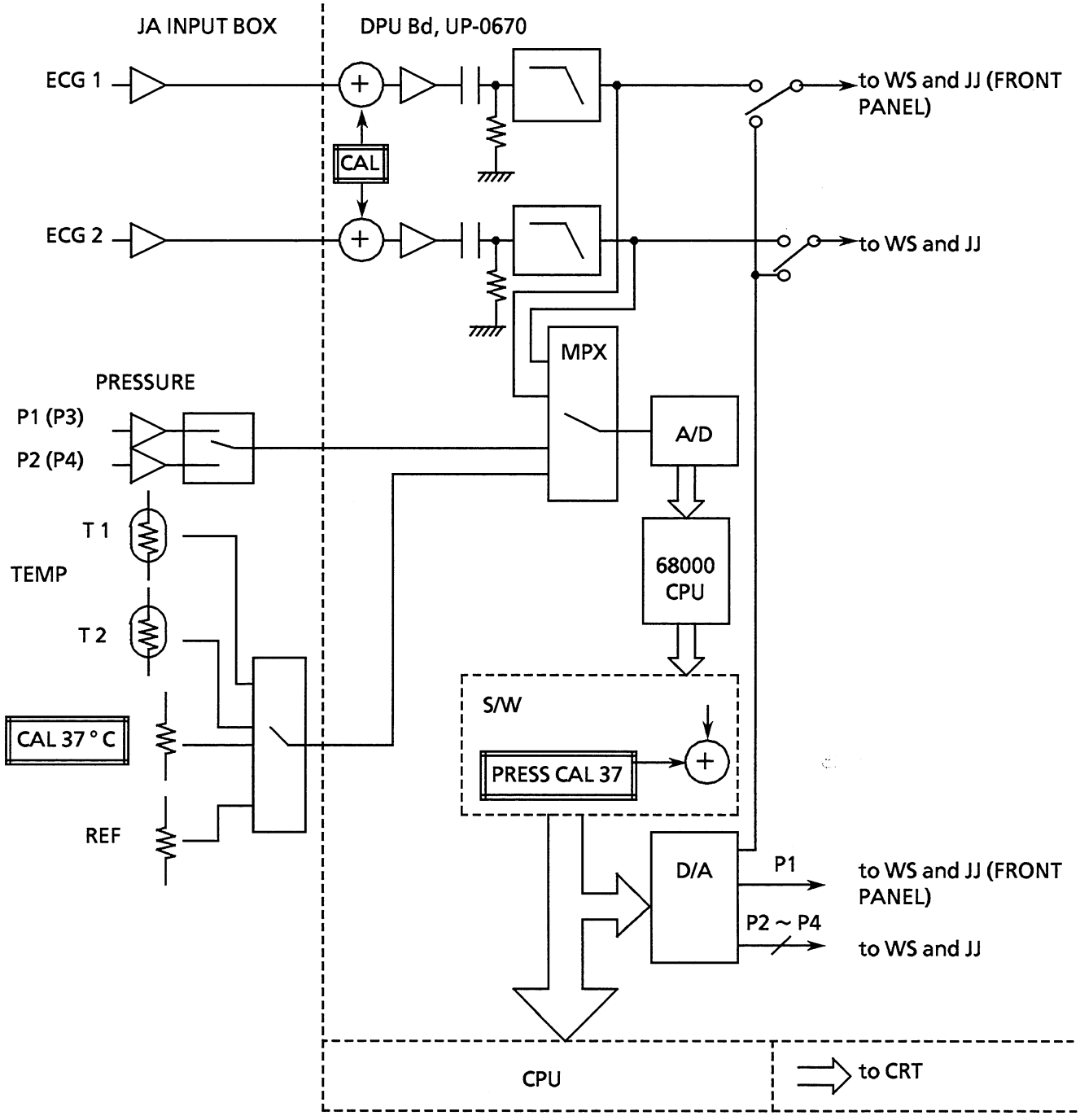


1-7-2 Input Signal Flow



1-7-3 Calibration Signal Flow

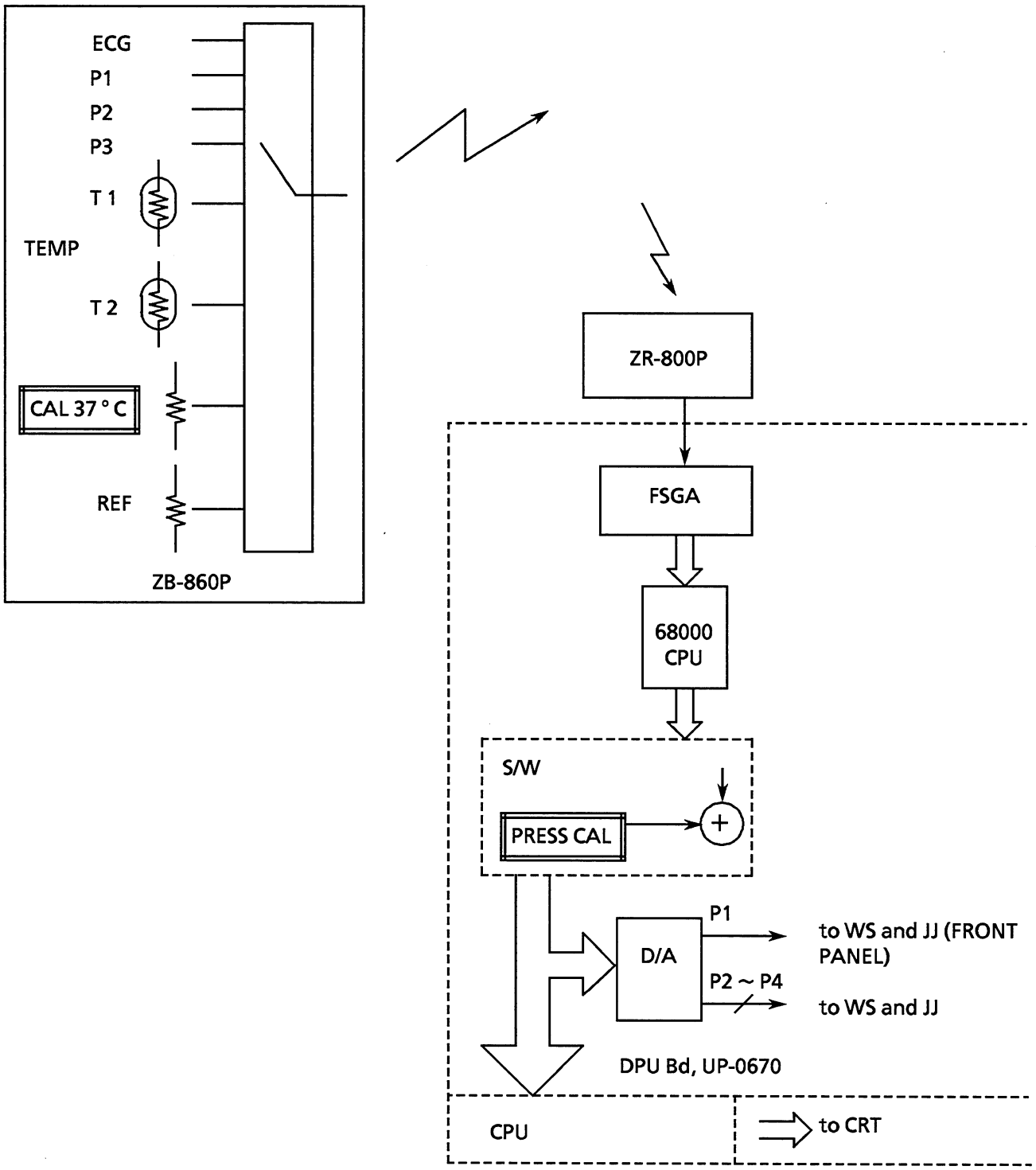
[Hardwire system]



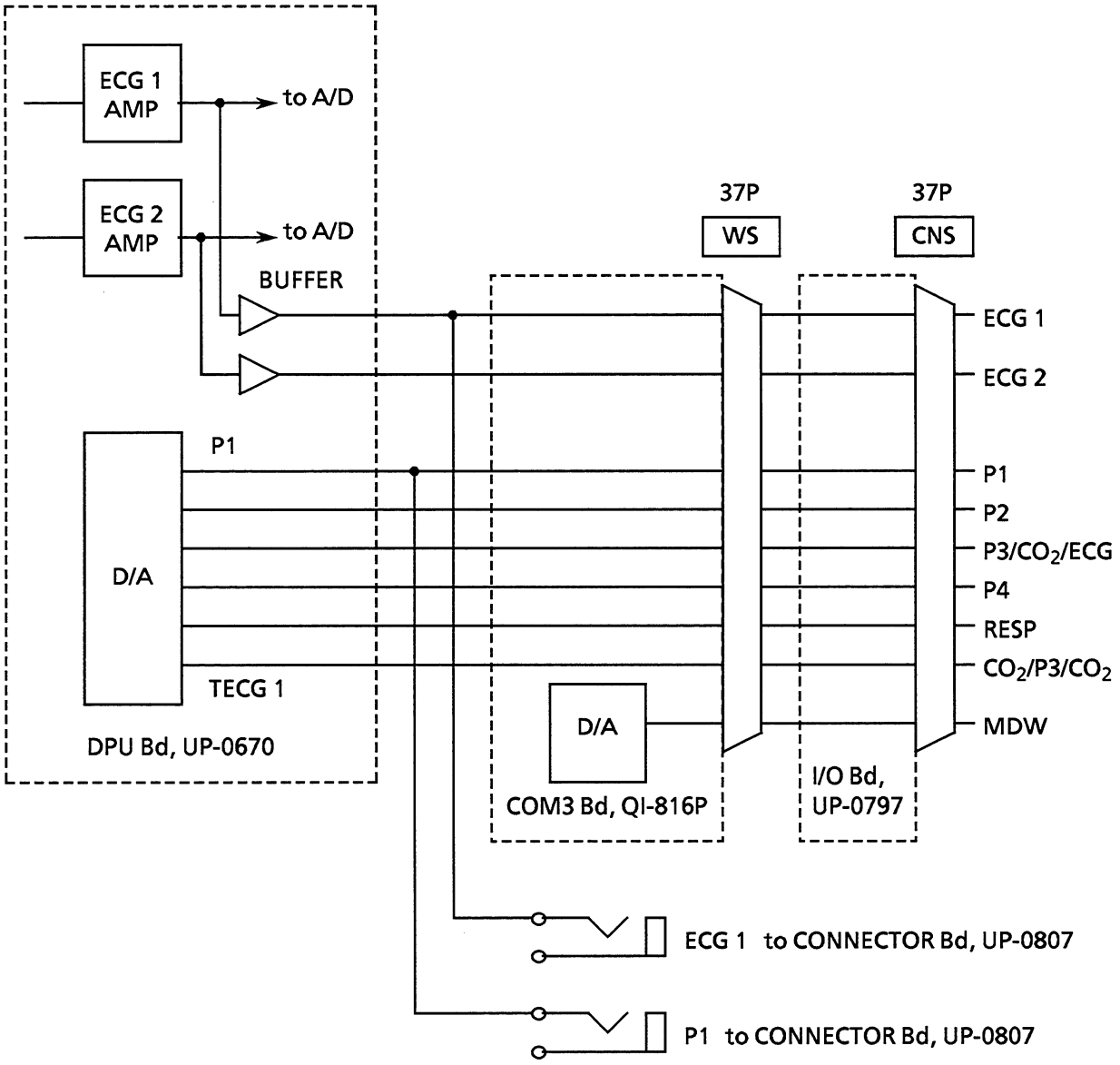
NOTE

1) ECG CAL CHECK : Effective from ECG time constant circuit on DPU board.
2) PRESSURE CAL CHECK : Effective from D/A convertor on DPU board.
3) TEMPERATURE CAL CHECK : Effective from AW-800PA.

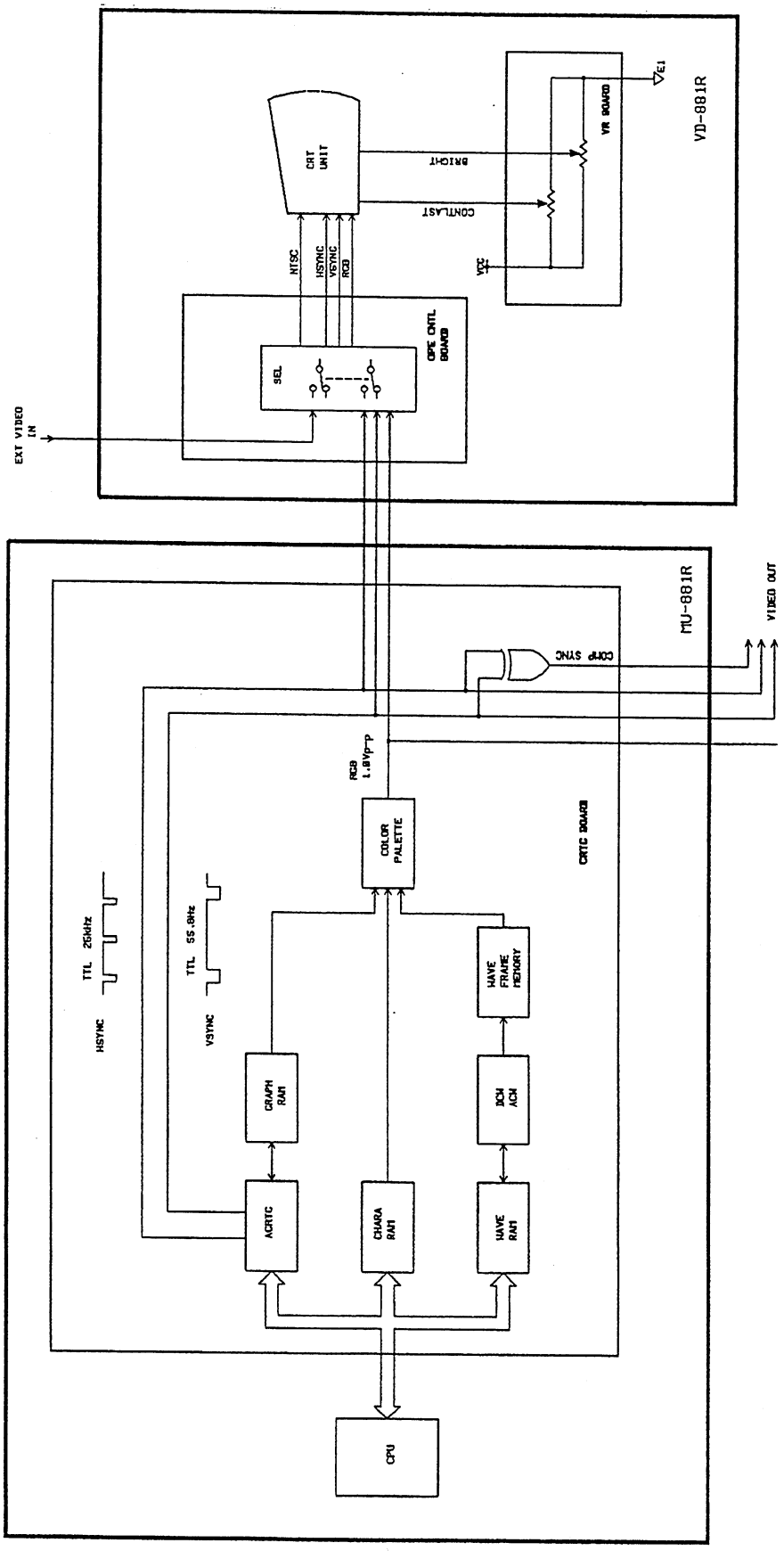
[Telemetry system]



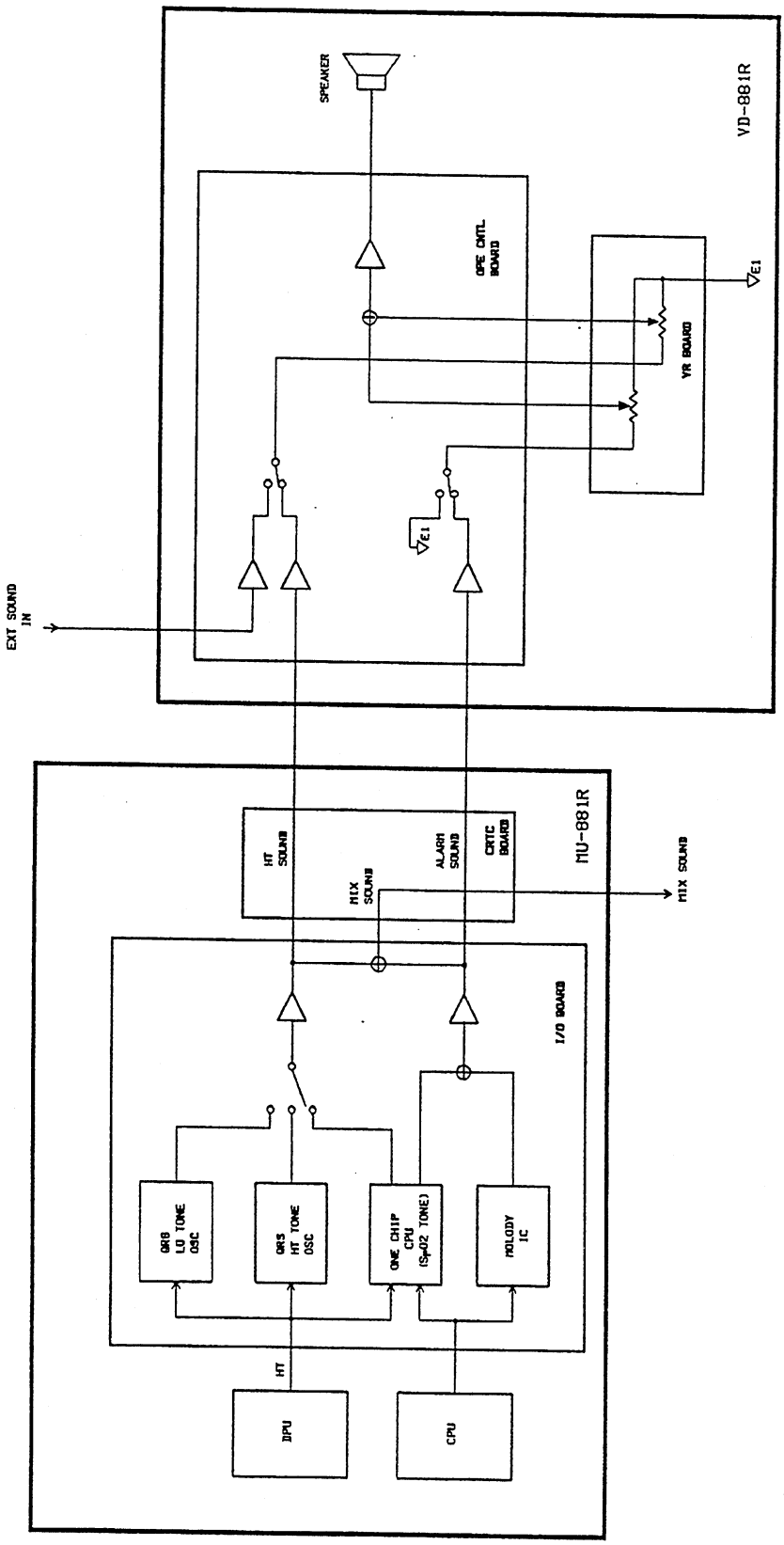
1-7-4 Output Signal Flow



1-7-5 Video Signal Flow

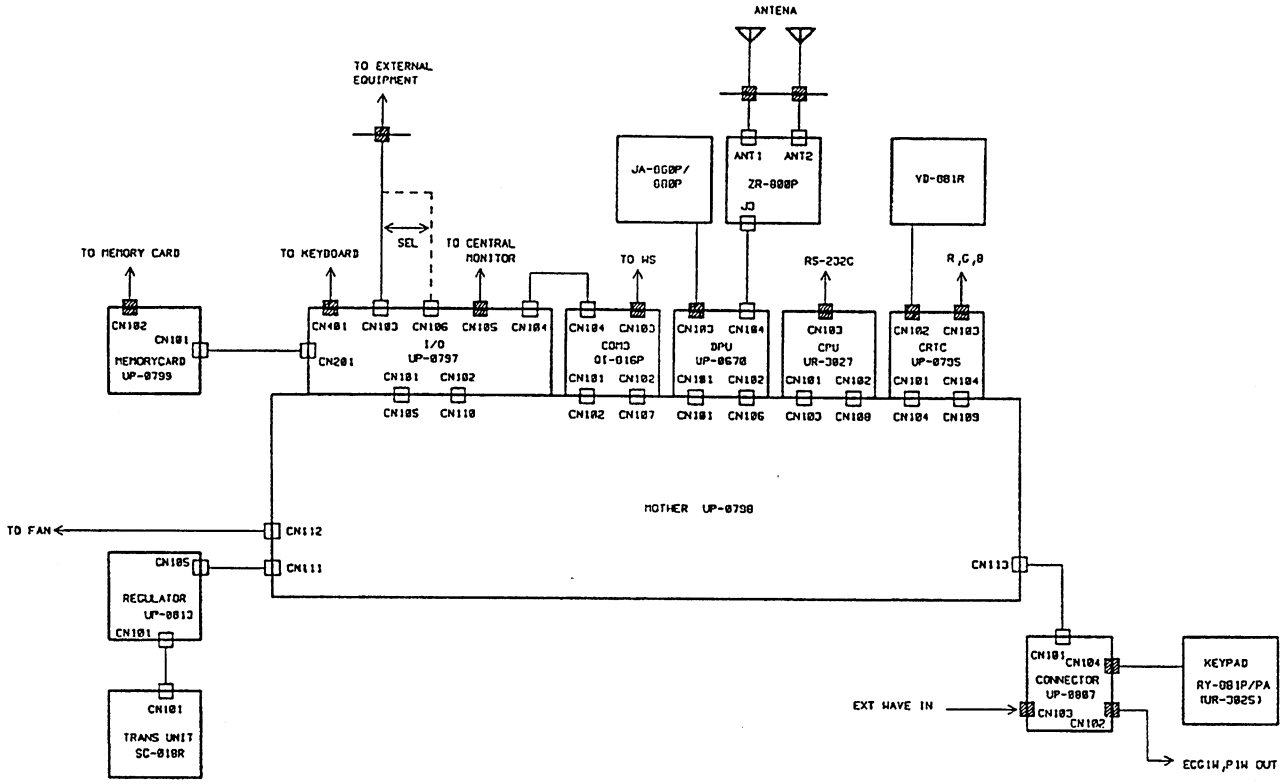


1-7-6 Sound Signal Flow

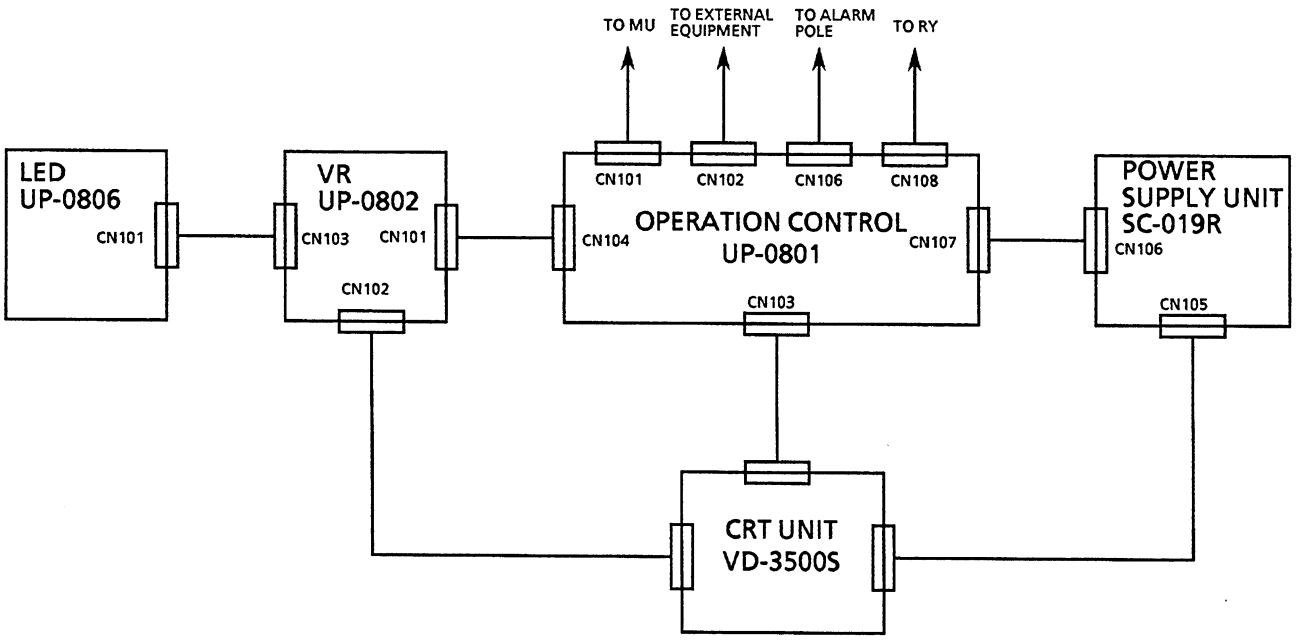


1-8 Connection Diagram

1-8-1 Main Unit, MU-881R

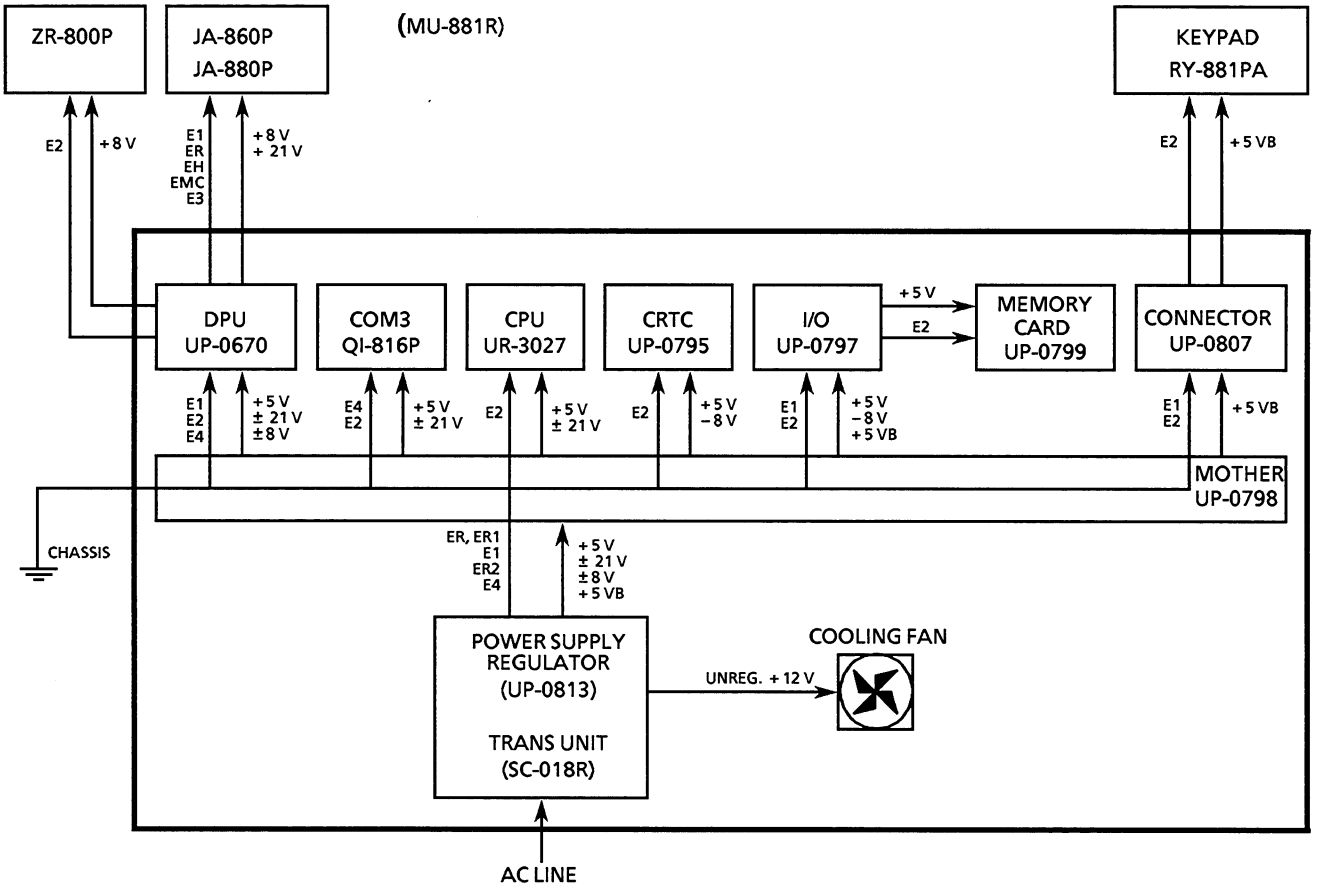


1-8-2 Display Unit, VD-881R

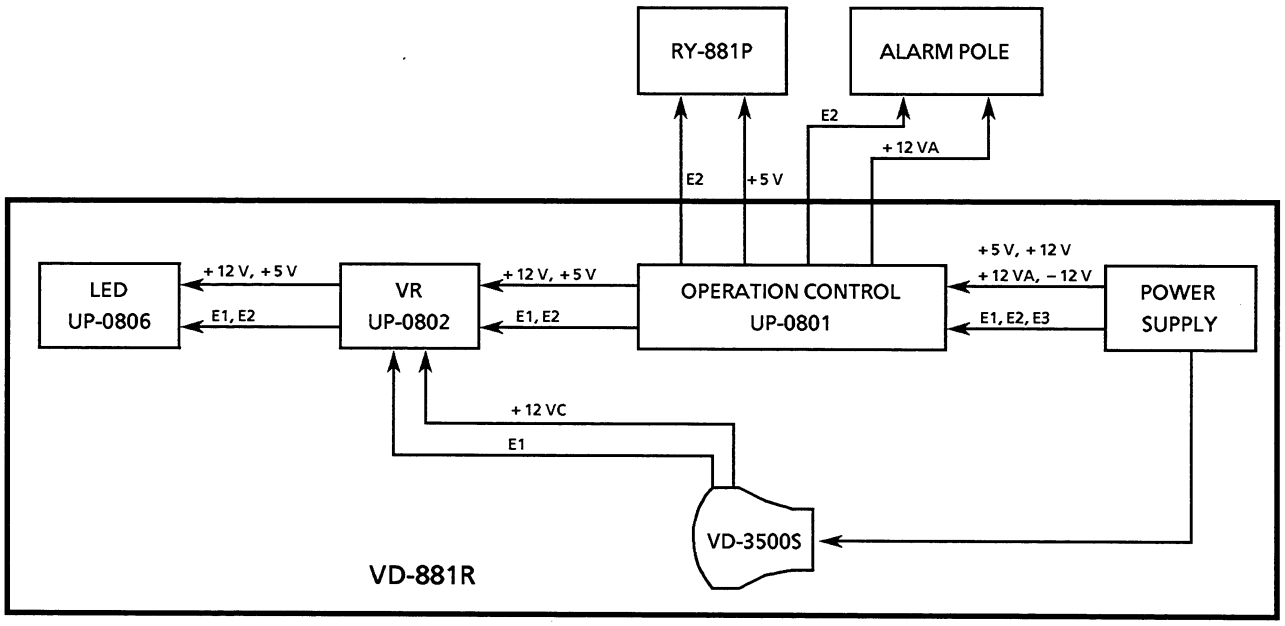


1-9 Power System Diagram

1-9-1 Main Unit, MU-881R



1-9-2 Display Unit, VD-881R



1-10 Related Instruments Connection

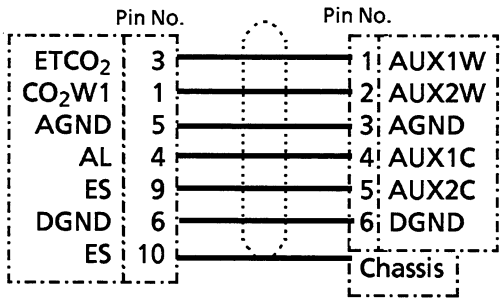
Firstly, select one of the following instruments on the SETUP display.

Related Instruments	Input signal			
	AUX1W	AUX2W	AUX1C (Active-low)	AUX2C (Active-low)
CO_2 Monitor (OIR-7101)	$ETCO_2$ (20 mmHg/V)	CO_2 Waveform (20 mmHg/V)	$ETCO_2$ Alarm Signal	CO_2 Measure Signal
External Alarm Signal	——	——	——	Alarm (Error) Indication Signal
External Analog Signal	——	External Waveform	——	——

——: Don't care

[OIR-7101]
Connector
: S-1628G
: P-1628A-CA(20)
: P-1628A-STA(01)

Connection cable: YS-005P8



[BSM-8800]
Connector
: RM12BPG-6P
Parts No. 078541

Section 2 SIGNAL LIST

2-1 Main Unit, MU-881R

2-1-1 COM 3 Board, UP-0563

Prefix "X" means negative logic.
For example: A/XM
High level (5V): Address recognition signal (active-high)
Low level (0V) : Message recognition signal (active-low)
If a signal is not found, search the symbol from "X + signal name" lists.
If a signal "X + symbol" is not found, search the symbol from "signal name-X".

Symbol	Function	Part
ALE 85	8085 address latch enable signal from 8085	4/10
A0L-A10L	Recorder CPU address bus	9/10
AX0-12	Global memory address bus	3/10
CLK 3M	8085 clock (3MHz)	4/10
CLK 96	Transmitting/receiving clock	7/10
CS	COM3 Board select signal	1/10
DOL-D7L	Dual port RAM data bus	9/10
DX0-7	Global memory data bus	3/10
DX85 0-15	8085 data bus	4/10
DX85 0-7	8085 data bus	4/10
IO0-7	Recorder CPU data bus	9/10
MDW	Delayed ECG waveform	6/10
MSK 7.5	RST 7.5 interrupt request signal mask signal	5/10
RD	CNS data reception signal	5/10
RD RET	CNS data reception return signal	5/10
RES 85	8085 external unit reset signal from 8085	4/10
RST 6.5	CNS data reception interrupt request signal	5/10
RST 7.5	Watch dog timer periodic interrupt request signal	7/10
RSTIN	8085 reset signal for CPU (CPU Board) from 8085	7/10
SD	Data transmit signal for CNS	5/10
SD RET	Data transmit return signal for CNS	5/10
SEL85	Global memory bus select signal	2/10
WDT	Software watch dog timer control signal	4/10
WDTINT	Watch dog timer interrupt request signal	7/10

2. SIGNAL LIST

Symbol	Function	Part
X6.5CLR	RST6.5CLR output flip-flop clear	4/10
X8251S	8251 select signal	4/10
XAL	Alarm signal	5/10
XBUSY2	BSM busy line signal for CNS	5/10
XBUSY2 RET	BSM busy line return signal for CNS	5/10
XBUSYL	Dual port RAM wait request signal for recorder CPU	9/10
XBUSYR	Dual port RAM wait request signal for CPU (CPU Board)	9/10
XCOMW	Recorder CPU memory write control signal	9/10
XCS0	WS reset port select signal	1/10
XCS1	8085 dual port RAM select signal	1/10
XCS3	CG ROM select signal	1/10
XCS4, 5	Printer buffer RAM select signal	1/10
XCSRST85	8085 reset port select signal from CPU (CPU Board)	2/10
XD/ASEL	DA port select signal	4/10
XDOS	Output port (IC146) select signal	4/10
XGLS 68	Global memory access request signal from CPU (CPU Board)	2/10
XGLS 68A	Global memory select signal from CPU (CPU Board)	2/10
XGLS85	Global memory select signal from 8085	4/10
XINT11	Interrupt request signal for CPU (CPU Board) from CPU (WS)	9/10
XINT16	Interrupt request signal for CPU (CPU Board) from 8085	5/10
XINTL	CPU (CPU Board) interrupt request signal for recorder signal	9/10
XIORD	8085 read control signal for output port	4/10
XIORST85	CPU (CPU Board) 8085 reset signal	2/10
XIOWR	8085 write control signal for output port	4/10
XLEDS	LED port select signal	4/10
XMRD	8085 read control signal for global memory	4/10
XMWR	8085 write control signal for global memory	4/10
XRAMC	Recorder CPU memory read	9/10
XRDL	Lower 8 bit data read	2/10
XRDU	Upper 8 bit data read	2/10
XRESET	CPU (CPU Board) reset request signal	9/10
XSWS	Dip switch port select signal	4/10
XWRL	Lower 8 bit data write	2/10
XWRU	Upper 8 bit data write	2/10

2-1-2 DPU Board, UP-0670

Symbol	Function	Part
*MA6	A/D RAM memory address	8/19
16M	16MHz clock	1/19
A1-23	Address bus lines 1-23	1/19
ADINT	AD interrupt (every 2msec)	6/19
ADSFT	A/D convertor shift voltage	15/19
ANT11	Diversity switching	10/19
AUX1C, AUX2C	External unit's waveform input control	10/19
AUX1W, AUX2W	Auxialiary input analog waveform signal	12/19
BERR	Bus error	1/19
CA0	A/D convertor data width control	7/19
CE	A/D convertor chip enable	8/19
CH1W/P1W	Channel-3 waveform/blood pressure 1 waveform	16/19
CH4W/P2W	Channel-4 waveform/blood pressure 2 waveform	16/19
CH5W/P3W	Channel-5 waveform/blood pressure 3 waveform	16/19
CH6W/P4W	Channel-6 waveform/blood pressure 4 waveform	16/19
CH7W/RW	Channel-7 waveform/respiration waveform	16/19
CH8W/EXTAUX	Channel-8 waveform or external input unit	16/19
CH9W	Channel-9 waveform	16/19
CLK	RF unit clock	10/19
CLK16M	16MHz system clock	3/19
CLK16MC	16MHz clock	3/19
CLK500K	500kHz	2/19
CLKSAMPL	8msec clock	3/19
D/A	D/A cconverted waveform signal	15/19
D0-15	Data bus lines 0-15	1/19
DATA	RF unit setting data	11/19
DTACK1	Data acknowledge 1	3/19
DTACK2	Data acknowledge 2	4/19
ECG, ECG2	2ch ECG regenerated ECG signal	11/19
ECG1AD, ECG2AD	Processed ECG amplifier output signal	13/19
EN1	Peak hold enable signal	8/19
FC0-2	Function code	1/19
FSSTS	Frame shift gate array status signal	8/19
G1-2	Gain select signal	14/19

2. SIGNAL LIST

Symbol	Function	Part
GMSLC	Global memory select signal	3/19
HA2-8	Individual head amplifier output signal	11/19
HAECG1	ECG1 signal	17/19
HAECG2	ECG2 signal (fixed lead II ECG)	17/19
HARESP	Respiration waveform	18/19
HICUT	ECG high cut filter select signal	11/19
HUM	ECG hum filter	11/19
IBW	Interbed waveform signal	12/19
INST	ECG instantaneous short circuit signal	11/19
INT1	Interrupt request signal from CPU to DPU	3/19
JACLK	JA communication clock	7/19
JACNTL	JA control signal	9/19
JADLWL	JA lower byte write	2/19
JAFCLK	JA floating clock	7/19
JARCLK	Respiration detection carrier generator clock	7/19
JASTS	JA status signal	9/19
L1	Auto D/A lower byte data latch signal	8/19
L2	Auto D/A upper byte data latch signal	8/19
LE	RF unit data latch enable signal	10/19
LMA2-4	Multiplexer switching control signal	8/19
LMA6	Analog input multiplexer inhibit control signal	8/19
MA0	Auto A/D or D/A memory address 0	7/19
MA1	A/D RAM memory address control (or select) signal	8/19
MDW	Delayed ECG waveform	12/19
MPX	Multiplexed waveform	11/19
PARA	Head amplifier recognition or measure status signal for input box	12/19
QB	256 kHz clock	7/19
R/XC	A/D convertor read/convert control (or select) signal	8/19
R/XW	Read/write control (or select) signal	1/19
R/XWB	System read/write control (or select) signal	3/19
R/XWC	System read/write control (or select) signal	3/19
RCT8MS	125Hz (8msec) clock	3/19
REF10V	+10V reference voltage	14/19
RESPAD	Respiration waveform signal for A/D convertor	11/19
RINST	Respiration wave instantaneous short circuit signal	11/19

Symbol	Function	Part
RSSI	Receiver field strength signal	15/19
RTC	ECG high cut filter control (or select) signal	11/19
S0	Hardwire or telemetry switching control signal	10/19
TC3.2	ECG time constant control signal (H:3.2sec;L:0.5sec)	11/19
TECG1W, TECG2W	Telemetry analog ECG waveform	15/19
TEST	1mV calibration control signal	11/19
TST	AD RAM test	8/19
W/XR	Write/read control (or select) signal	1/19
XADDR1-13	System address bus A1-13	5/19
XADDR17-23	System address bus A17-23	3/19
XADRCS	A/D RAM chip select signal	2/19
XADWR	AD RAM memory write	8/19
XAS	Address strobe signal	1/19
XASB	System address strobe signal	3/19
XCLK0	8MHz clock	4/19
XCNT	Counter status read	2/19
XCPUINT	Interrupt request for CPU board	2/19
XCS	A/D RAM memory write control signal	8/19
XDIPSW	Dip switch read	2/19
XDTACK	Data acknowledgement signal	1/19
XDTACK	System data acknowledgement signal	3/19
XE0	A/D RAM memory read	8/19
XFSCLR	Frame sync clear	2/19
XGARD	FS Gate array read	2/19
XGMCS	Global memory chip select signal	4/19
XGMCSC	System global memory chip select signal	4/19
XGMRL	Global memory lower byte read	4/19
XGMRU	Global memory upper byte read	4/19
XGMSL	Global memory select	2/19
XGMWL	Global memory lower byte write	4/19
XGMWU	Global memory upper byte write	4/19
XHALT	Halt	1/19
XHIFCM	ECG write control signal	2/19
XHO	ECG measure signal	10/19
XHT	ECG synchronizing signal	10/19
XIA	Interrupt request signal acknowledge	2/19

2. SIGNAL LIST

Symbol	Function	Part
XINT13	Interrupt request signal from DPU to CPU	3/19
XIORST	I/O port reset signal (SYSTEM)	3/19
XIORSTC	I/O reset signal	2/19
XIPL0-2	Interrupt request priority level	1/19
XJADLR	JA lower 16 bits status read	2/19
XJADLWU	JA lower upper byte write	2/19
XJADUR	JA upper 16 bits status read	2/19
XJADUWL	JA upper byte write	2/19
XJADUWU	JA upper upper byte write	2/19
XLDS	Lower byte data strobe signal	1/19
XLDSB	System lower byte data strobe signal	3/19
XLDSC	System lower byte data strobe signal	3/19
XLED	LED write output port	2/19
XLEN2	D/A multiplexer inhibit control signal	8/19
XRAMCS	RAM chip select signal	1/19
XRDLS	Lower byte read	1/19
XRESET	Reset signal	1/19
XRESTS	RF status read	2/19
XRFCNTL	RF write	2/19
XRO	JARCLK preset signal	7/19
XROMCS	ROM chip select signal	1/19
XSATA0-15	System data bus D0-15	5/19
XSTR	Pacing pulse strobe signal	8/19
XSYNC2	Frame shift gate array SYNC	8/19
XUDS	Upper byte data strobe signal	1/19
XUDSB	System upper byte data strobe signal	3/19
XUDSC	System upper byte data strobe signal	3/19
XVPA	Valid peripheral address	1/19
XWDLS	Lower byte write	1/19

2-1-3 CRTC Board, UP-0795

Symbol	Function	Part
16MHz	16MHz clock	8/20
16MHzC	16MHz clock	7/20
2MHz	ACW Synchronizing clock	8/20
32MHz	32MHz clock for graphic processing	2/20
32MHzG	32MHz clock	8/20
64MHz	Clock for palette code	18/20
A1D0-3	Latched individual signal A1SD0-3	6/20
A1SD0-3	Waveform serial data A 1,3,5,7 trace EVEN	6/20
A2D0-3	Latched individual signal A2SD0-3	6/20
A2SD0-3	Waveform serial data A 2,4,6,8 trace EVEN	6/20
A3D0-3	Latched individual signal A3SD0-3	6/20
A3SD0-3	Waveform serial data A 1,3,5,7 trace ODD	6/20
A4D0-3	Latched individual signal A4SD0-3	6/20
A4SD0-3	Waveform serial data A 2,4,6,8 trace ODD	6/20
AA00-07	Upper screen frame memory address	8/20
ADDL	Character ROM address latch	16/20
ALSND	Alarm sound signal	19/20
AREA	ACW setting signal (Input port signal)	8/20
ASD0-3	Waveform serial data A EVEN	7/20
ATR B	Character attribute (B) select signal	16/20
ATR BL	Character attribute blink select signal	16/20
ATR G	Character attribute (G) select signal	16/20
ATR I	Character attribute (I) select signal	16/20
ATR R	Character attribute (R) select signal	16/20
ATR RV	Character attribute reverse signal	16/20
ATRL	Character attribute signal latch	16/20
B1D0-3	Latched individual signal B1SD0-3	6/20
B1SD0-3	Waveform serial data B 1,3,5,7 trace EVEN	6/20
B2D0-3	Latched individual signal B2SD0-3	6/20
B2SD0-3	Waveform serial data B 2,4,6,8 trace EVEN	6/20
B3D0-3	Latched individual signal B3SD0-3	6/20
B3SD0-3	Waveform serial data B 1,3,5,7 trace ODD	6/20
B4D0-3	Latched individual signal B4SD0-3	6/20
B4SD0-3	Waveform serial data B 2,4,6,8 trace ODD	6/20

2. SIGNAL LIST

Symbol	Function	Part
BA00-07	Lower screen frame memory address	8/20
BAM00-15	Waveform data (B)	14/20
BBM00-15	Delayed waveform data (B)	15/20
BCONT	CPU bus control	5/20
BSD0-3	Waveform serial data B EVEN	7/20
C1D0-3	Latched individual signal C1SD0-3	6/20
C1SD0-3	Waveform serial data C 1,3,5,7 trace EVEN	6/20
C2D0-3	Latched individual signal C2SD0-3	6/20
C2SD0-3	Waveform serial data C 2,4,6,8 trace EVEN	6/20
C3D0-3	Latched individual signal C3SD0-3	6/20
C3SD0-3	Waveform serial data C 1,3,5,7 trace ODD	6/20
C4D0-3	Latched individual signal C4SD0-3	6/20
C4SD0-3	Waveform serial data C 2,4,6,8 trace ODD	6/20
CHA0-12	Character ROM address	16/20
CHD0-7	Character ROM output data	17/20
CHRA0-3	Character ROM address	17/20
CK2M	Character 2MHz clock	16/20
CK4M	Character 4MHz clock	16/20
CMA0-12	Character RAM address	16/20
CMD0-15	Character RAM output data	16/20
CSD0-3	Waveform serial data C EVEN	7/20
CUD CD	Character delayed timing signal	16/20
DASD0-3	Waveform serial data A ODD	7/20
DBSD0-3	Waveform serial data B ODD	7/20
DCSD0-3	Waveform serial data C ODD	7/20
DDISP1	Displayed timing 1 (delayed) signal	8/20
DISP B	Character display timing (delayed 2 clock) signal	16/20
DISP F	Character display timing (delayed 4 clock) signal	16/20
DSLD	Waveform data change start signal (delayed)	8/20
ESND	Ground for sound	19/20
EXTRDY	Ready signal	19/20
G.CHVB	Graphic and character composite video (B) signal	17/20
G.CHVG	Graphic and character composite video (G) signal	17/20
G.CHVI	Graphic and character composite video (I) signal	17/20
G.CHVR	Graphic and character composite video (R) signal	17/20
GA0-8	Graphic RAM address	2/20

Symbol	Function	Part
GAM00-15	Waveform data (G)	12/20
GBM00-15	Delayed waveform data (G)	13/20
GSD0-15	Graphic serial data	3/20
GVB	Graphic video (B) signal	3/20
GVG	Graphic video (G) signal	3/20
GVI	Graphic video (I) signal	3/20
GVR	Graphic video (R) signal	3/20
H.C.	Color hardcopying signal	18/20
HSYNC	Horizintal synchronizing signal	2/20
HTSND	QRS synchronized pulse sound signal	19/20
LCK	Gate array space control (ACW-DCW) signal	6/20
LDP1, 2	Shift register load 1,2	8/20
M/XS SEL	Master/slave select signal	19/20
MA16-19	Memory address select signal (GRAPHIC)	2/20
MAA00-07	Upper screen latched frame memory address	8/20
MAD0-15	Memory address/data (GRAPHIC)	2/20
MBA00-07	Lower screen latched frame memory address	8/20
MCYC	Memory cycle	2/20
MIXSND	Alarm sound signal mixed with QRS sycnchronized pulse sound signal	19/20
PLOL3	Palette overwrite input signal	18/20
PLPT7	Palette pixel input signal	18/20
R,G,B	RGB signal	19/20
R/XWC	Read/write control (or select) signal	1/20
RAM00-15	Waveform data (R)	10/20
RBM00-15	Delayed waveform data (R)	11/20
RxD1	Main unit inputted data for Display	19/20
RxD2	Main unit inputted data for keypad	19/20
SAS	Frame memory serial shift signal	8/20
SAS0, 1	Frame memory serial shift 0, 1 signal	8/20
SCLK	Change waveform clock	6/20
TxD1	Main unit outputted data for Display	19/20
TxD2	Main unit outputted data for keypad	19/20
VSYNC	Vertical synchronizing (every one frame) signal	2/20
W SC	Graphic RAM data transmission serial clock	2/20
WA1-16	Waveform RAM address	4/20

2. SIGNAL LIST

Symbol	Function	Part
WBVA	Waveform video (B) data	14/20
WBVB	Delayed waveform video (B) data	15/20
WD0A-15A	Waveform data 1,3,5,7 trace EVEN	4/20
WD0B-15B	Waveform data 2,4,6,8 trace EVEN	4/20
WD0C-15C	Waveform data 1,3,5,7 trace ODD	5/20
WD0D-15D	Waveform data 2,4,6,8 trace ODD	5/20
WD08-15	ACW setting data	8/20
WDISP	Waveform display timing	8/20
WGVA	Waveform video (G) data	12/20
WGVB	Delayed waveform video (G) data	13/20
WRVA	Waveform video (R) data	10/20
WRVB	Delayed waveform video (R) data	11/20
X16MHzC	16MHz clock (reverse shaded)	7/20
X32MHz	32MHz clock	8/20
X8MHz	8MHz clock	2/20
XACRTCIRQ	Interrupt request signal from ACRTC	1/20
XACRTCSL	ACRTC select signal	1/20
XASC	Address strobe signal	1/20
XC LOAD	Character load timing control signal	16/20
XCAS	Graphic RAM column address strobe signal	2/20
XCASA	Upper screen frame memory column address strobe signal	8/20
XCASB	Lower screen frame memory column address strobe signal	8/20
XCHOEH	Upper byte character RAM read	1/20
XCHOEL	Lower byte character RAM read	1/20
XCHRDAK	Character data acknowledge signal	1/20
XCHRSL	Character RAM select signal	1/20
XCHWEH	Upper byte character RAM write	1/20
XCHWEL	Lower byte character RAM write	1/20
XCRDTAK	ACRTC data acknowledge signal	1/20
XCS0, 1	Waveform RAM select 0, 1 (delayed) signal	4/20
XCS2	Gate array space control (ACW-DCW) signal	6/20
XCSJ	Gate array space control (ACW-DCW) signal	6/20
XCSYNC	Composite synchronizing signal	17/20
XCUD D	Delayed display timing 1 (XCUD1) control signal	2/20
XCUD1	Display timing 2 control signal	2/20
XDAT	Gate array space control (ACW-DCW) control signal	6/20

Symbol	Function	Part
XDG0-3	Waveform data buffer enable	4/20
XDG0-3	Waveform data buffer enable	5/20
XDISP1	Display timing 1 signal	2/20
XEXSYNC	Auxiliary unit synchronizing signal	2/20
XGDTAK	Waveform data acknowledge (from gate array) signal	1/20
XHSYNC	Horizontal synchronizing (reverse shaded) signal	2/20
XHSYNCD	Delayed horizontal synchronizing signal	8/20
XHT	QRS synchronized pulse for alarm pole	19/20
XIORD	I/O port read	1/20
XIOWR	I/O port write	1/20
XIRQ	Interrupt request signal from ACW	1/20
XKEYRST1	VD reset signal	19/20
XKEYRST2	Keypad reset signal	19/20
XLDSC	Lower byte data strobe signal	1/20
XMD0	Gate array space control (ACW-DCW) signal	6/20
XOE0, 1	Graphic RAM read	2/20
XOEA	Upper screen frame memory read	8/20
XOEB	Lower screen frame memory read	8/20
XOEH	Waveform RAM upper byte data read	5/20
XOEH	Waveform RAM upper byte data read	4/20
XOEL	Waveform RAM lower byte data read	5/20
XOEL	Waveform RAM lower byte data read	4/20
XPALRD	Read palette code	1/20
XPALWR	Write palette code	1/20
XPS.CTL2	Power state status signal	19/20
XRAS	Graphic RAM row address strobe signal	2/20
XRASA	Upper screen frame memory row address strobe signal	8/20
XRASB	Lower screen frame memory row address strobe signal	8/20
XRST	System reset signal	1/20
XS0G, 1G	Graphic RAM serial enable signal	2/20
XSE0-7	Frame memory serial enable signal	8/20
XSLD	Waveform data change start signal	6/20
XUDSC	Upper byte data strobe signal	1/20
XVSYNC	Vertical synchronizing (reverse shaded) signal	2/20
XWARSL	Waveform RAM select signal	1/20
XWE0, 1	Graphic RAM write	2/20

2. SIGNAL LIST

Symbol	Function	Part
XWE0-3H	Waveform RAM upper byte data write 0-3	4/20
XWE0-3H	Waveform RAM upper byte data write 0-3	5/20
XWE0-3L	Waveform RAM lower byte data write 0-3	4/20
XWE0-3L	Waveform RAM lower byte data write 0-3	5/20
XWEA	Upper screen frame memory write	8/20
XWEB	Lower screen frame memory write	8/20

2-1-4 I/O Board, UP-0797

Symbol	Function	Part
ALSND	Alarm sound signal	3/6
AUX1C, AUX2C	Auxiliary input waveform control signal	1/6
AUX1W, AUX2W	Auxiliary input waveform 1 , 2	1/6
BNK0-6	Memory card bank switching signal	2/6
BVD1,2	Memory card battery voltage detection signal	2/6
CH3W/P1W	Channel-3 waveform/blood pressure 1 waveform	1/6
CH4W/P2W	Channel-4 waveform/blood pressure 2 waveform	1/6
CH5W/P3W	Channel-5 waveform/blood pressure 3 waveform	1/6
CH6W/P4W	Channel-6 waveform/blood pressure 4 waveform	1/6
CH7W/RW	Channel-7 waveform/respiration waveform	1/6
CH8W/EXTAUX	Channel-8 waveform/auxiliary unit waveform	1/6
CHRSL1, 2	Character ROM select signal	4/6
DTACKB1, 2	Data acknowledge for internal timing signal	2/6
ECG1W, ECG2W	ECG waveform 1, 2 signal	1/6
ESND	Ground for sound control board	1/6
HI/LO	Synchronized with QRS pulse high/low tone switching signal	3/6
HTLO	Low tone synchronized QRS pulse	3/6
HTSND	Synchronized QRS pulse sound signal	3/6
IB SEL	Interbed select signal	1/6
IBW	Interbed waveform signal	1/6
KD0-7	Character ROM data signal	6/6
LATCHA	Memory card address latch signal	2/6
M/XS SEL	Display unit master/slave select signal	5/6
MA1-18	Memory card address A1-18 control (or select) signal	2/6
MCLED	Memory card indication LED signal	2/6
MD0-15	Memory card data D0-15	2/6
MDW	Delayed ECG waveform	1/6
MIXSND	Mixed sound (alarm and synchronized QRS pulse) signal	3/6
ON/OFF	Synchronized QRS pulse sound on/off switching signal	3/6
OUTB0-3	8279 (CPU Board) output signal B	3/6
RD	CNS data reception signal	1/6
RD RET	CNS data reception return signal	1/6
RDY/XBSY	Ready/busy status signal	2/6
RWRCTL	Power supply control signal	5/6

2. SIGNAL LIST

Symbol	Function	Part
RxD1	Receiving data (for display unit)	4/6
RxD2	Receiving data (for keypad when connected to video display VD)	4/6
RxD3	Receiving data (for keypad when connected to main unit MU)	4/6
RxDF	Receiving data signal (full key board)	4/6
SaO2	SaO2 tone/normal synchronized with QRS pulse sound signal	3/6
SD	Data transmission signal for CNS	1/6
SD RET	Data transmission return signal for CNS	1/6
SL0-3	CPU Board 8279 scan line signal	3/6
SNDINH	Sound inhibit signal	3/6
SRSL1-4	Shift register select signal	4/6
STNBY	Power standby control signal	5/6
TCCLR	Timer condenser clear signal	5/6
TOSC	Tone oscillator signal	3/6
TxD1	Transfering data (for display unit)	4/6
TxD2	Transfering data (for keypad when connected to video display VD)	4/6
TxD3	Transfering data (for keypad when connected to main unit MU)	4/6
TxDF	Transfering data (full key board)	4/6
W/XR	Read/write control (or select) signal	2/6
WP	Memory card write protect signal	2/6
X1CHIPW	Write signal for 1CHIP CPU	4/6
XAL	Alarm signal	1/6
XBUSY2	CNS data transmission interrupt request signal	1/6
XBUSY2 RET	CNS data transmission interrupt request return signal	1/6
XCD1, 2	Memory card detection signal	2/6
XCE1, 2	Memory card enable signal	2/6
XDEL	Lower byte data bus buffer enable signal	2/6
XDEU	Upper byte data bus buffer enable signal	2/6
xDSRF	Data set to ready signal (full key board)	4/6
XERESET	Auxiliary reset signal to CPU board	5/6
XEXTRST	Auxiliary reset (switch) signal	5/6
XHO	ECG measure signal	1/6
XHT	Synchronized QRS pulse signal	3/6
XHTOUT	ECG synchronized signal	1/6
XINTR	Communication interrupt request signal	1/6

Symbol	Function	Part
XINTR RET	Communication interrupt request return signal	1/6
XIOSL1-3	I/O port select signal	2/6
XLEDSEL	LED select signal	4/6
XMCPORTR	Memory card port read	2/6
XMCPORTW	Memory card port write	2/6
XMCSW	Memory card switch status signal	2/6
XOE	Output enable signal	2/6
XRCLK	Clock latch signal	4/6
XRD1, 2	72001 read	4/6
XRDYF	Ready signal (full key board)	4/6
XREG	Attribute memory space select signal	2/6
XRETRN	Retry control port enable signal	4/6
XRSTF	Reset signal (full key board)	4/6
XRTYF	Retry signal (full key board)	4/6
XSRSEL	Serial clock select signal	4/6
XWE	Write enable signal	2/6

2-1-5 UR-3027, CPU Board

Symbol	Function	Part
A01-23	Internal address bus 01-23	1/16
CEXT	RAM's buffer condenser terminal	14/16
CLK16M	16MHz System clock	1/16
CLK2M	2MHz clock	2/16
CLK500K	500kHz clock	2/16
CLKSAMPL	Syncronization signal for copying waveform data	16/16
CNTL/STB	8279 control/strobe signal	13/16
CTS	Clear signal to send from 71051	12/16
D00-15	Internal data bus 00-15	1/16
DSR	71051 data set to ready	12/16
DTR	71051 data terminal ready	12/16
ERESET	External reset signal (positive logic)	4/16
FC0-2	Interrupt request encoding signal	1/16
FG	Ground	12/16
I51TXRDY	Ready to transmit signal from 8251	6/16
I51XRXDY	Ready to receive signal from 8251	6/16
I54OUT2	71054 signal 2 counter	6/16
I6242STD	6242 standard clock	6/16
I79IRQ	Interrupt request signal from 8279	6/16
IACK	Interrupt request acknowledge signal	3/16
INT10-17	Interrupt level 10-17	6/16
LDS	Lower byte data strobe signal on system bus	1/16
OUTA0-3	8279 data output A0-3	13/16
OUTB0-3	8279 data output B0-3	13/16
R/XE	High level read;Low level write	1/16
R/XWB	System read/write control signal	16/16
RL0-7	8279 return lines 0-7	13/16
RTCSL	Real time clock select signal	3/16
RTS	Data request signal for sending data from 71051	12/16
RXD	Receive data	12/16
SG	Ground signal	12/16
SHIFT	8279 shift signal	13/16
SL0-3	8279 scan lines 0-3	13/16
TXD	Transmit data	12/16

Symbol	Function	Part
VB	Battery voltage	11/16
WRDL	Lower byte write signal	2/16
WRDU	Upper byte write signal	2/16
WTDERR	Watch dog timer error signal	4/16
WTDSTOP	Watch dog timer stop control signal	4/16
XADDR01-23	System address bus (negative logic)	15/16
XAS	Address strobe signal	1/16
XASB	System address strobe signal	16/16
XBERR	Bus error	1/16
XDATA00-16	System data bus (negative logic)	15/16
XDRACK	Data acknowledge signal	1/16
XDS/LEDS	Dip switch/LED select signal	3/16
XDTACKB	System data acknowledge signal	16/16
XE2PSL	EEPROM select signal	11/16
XE2PSL	EEPROM select signal	3/16
XEBUS	System bus select signal	3/16
XERESET	External reset signal (negative logic)	4/16
XHALT	Halt signal for CPU	1/16
XI51SL	71051 select signal	3/16
XI54ACK	71054 acknowledge signal	6/16
XI54SL	71054 select signal	3/16
XI62ACK	6242 acknowledge signal	6/16
XI79SL	8279 select signal	3/16
XIACK1-2	Interrupt acknowledge signal 1-2	5/16
XIACK10-17	nterrupt acknowledge 10-17	6/16
XINT10-50	Interrupt signal 10-50	16/16
XINT7	Interrupt level 7	4/16
XIO	I/O port select signal	3/16
XIORD	I/O port read signal	2/16
XIORST	System reset signal	16/16
XIOWR	I/O port write signal	2/16
XIPL0-2	Interrupt request priority level	1/16
XLDSB	System lower byte data strobe signal	16/16
XPDOWN	Power down indication signal (generated in UP-0315)	4/16
XPWDWN	Voltage down indication signal	11/16
XRAM	RAM select signal	3/16

2. SIGNAL LIST

Symbol	Function	Part
XRAM0SL-XRAM3SL	RAM0-3 select signal	3/16
XRDL	Lower byte read signal	2/16
XRDU	Upper byte read signal	2/16
XRESET	Reset signal for CPU	1/16
XROM	ROM select signal	3/16
XROM0SL-XROM3SL	ROM0-3 select signal	3/16
XRTCSL	6264 select signal	11/16
XST/WTDS	Status/watch dog select signal	3/16
XUDS	Upper byte data strobe signal on system bus	1/16
XUDSB	System upper byte data strobe signal	16/16
XVPA	Valid peripheral address	1/16
XWTDLAMP	Watch dog timer lamp control signal	4/16
XWTDSTB	Watch dog timer strobe signal	4/16

2-2 Keypad, RY-881PA

2-2-1 CONSOLE Board, UR-3025

Symbol	Function	Part
READY	Ready	
RxD2	Receiving data signal	
TxD2	Transmit data signal	
XP.SCTL2	Power status control signal	
XRESET	Keypad reset signal	

2-3 Display Unit, VD-881R

2-3-1 OPERATION CONTROL Board, UP-0801

Symbol	Function	Part
ALSND	Alarm sound	3/4
ALSND20	Alarm sound signal amplified 20 times	3/4
ALSNDGND	Ground for alarm sound	3/4
ALSNDOFF	Alarm sound OFF	2/4
CLICK	Key sound	2/4
CMPS	CRT unit NTSC signal	1/4
COMP	NTSC signal input control from auxiliary unit (output port)	1/4
CSND	Composite SND signal	3/4
ECOMPS	NTSC signal from auxiliary unit	1/4
EHSYNC	Horizontal synchronizing signal from auxiliary unit	1/4
ER,EG,EB	RGB signals from auxiliary unit	1/4
ERG,EGG,EBG	Ground for individual RGB signals from auxiliary unit	1/4
EVIDEO	RGB signals input control from auxiliary unit (output port)	1/4
EVSYNC	Vertical synchronizing signal from auxiliary unit	1/4
EXSN	Auxiliary unit input sound	4/4
EXSNDGND	Ground for auxiliary unit input sound	4/4
EXSNDSEL	Auxiliary unit input sound select	2/4
HSYNC	CRT unit horizontal synchronizing signal	1/4
HTSND	QRS synchronized pulse sound	3/4
HTSND25	QRS synchronized pulse sound signal amplified 25 times	3/4
HTSNDGND	Ground QRS synchronized pulse sound	3/4
KREADY	Keypad ready signal	2/4
M/XS SEL	Master/slave select	2/4
MHSYNC	Horizontal synchronizing signal from main unit	1/4
MR,MG,MB	RGB signal from main unit	1/4
MRG,MGG,MBG	Ground for individual RGB signals from main unit	1/4
MVSYNC	Vertical synchronizing signal from main unit	1/4
R,G,B	CRT unit RGB signals	1/4
READY	Ready signal	2/4
REMOTE	Remote control infra-red signal	2/4
RxD1	Receiving data signal to main unit	2/4

Symbol	Function	Part
RxD2	Receiving data signal to keypad	2/4
SALSND20	Select ALSND20 signal	4/4
SCSND	Select CSND signal	3/4
SLEEP	Sleep screen port output	2/4
SPKR+	Speaker signal	3/4
SPKR-	Speaker signal	3/4
TxD1	Transferring data to main unit	2/4
TxD2	Transferring data to keypad	2/4
VALSND	ALSND signalwith volume information added	3/4
VHT/EXSND	HT/EXT SND signal with volume information added	3/4
VSYNC	CRT unit vertical synchronizing signal	1/4
WSLEEP	Sleep sound	3/4
XALPLG	Alarm pole GREEN output	2/4
XALPLR	Alarm pole RED output	2/4
XALPLY	Alarm pole YELLOW output	2/4
XCOMP	CRT unit NTSC signal input control signal	1/4
XEVIDEO	RGB signals input control signal from auxiliary unit signal	1/4
XEXCOMP	NTSC signal input control signal from auxiliary unit signal	1/4
XHT	QRS synchronized pulse signal for alarm pole	2/4
XP.SCTL1	Power status control signal to power supply unit signal	2/4
XP.SCTL2	Power status control signal to main unit signal	2/4
XP.SCTLIN	Power status control signal from keypad	2/4
XRESET1	VD reset	2/4
XRESET2	Keypad reset	2/4

2-3-2 OPERATION (VR) Board, UP-0802

Symbol	Function	Part
BRIGHT	Brightness control signal	
CONT	Contrast control signal	

Section 3 CIRCUIT DESCRIPTION

3-1 JA-DPU Analog Signal Processor

Each head amplifier board amplifies the measuring parameter and transfers the analog signals to the DPU board (UP-0670).
The DPU board time-shares the analog signals with a 16-channel multiplexer and converts the analog signals to digital signals with a 12 bit D/A converter through a d.c. level shift circuit and sample hold circuit according to each specified timing.
The digital signals are displayed on the CRT after being gain-controlled, filtered and formatted by software while the digital signals are converted to analog signals for a recorder or central monitor.
All the signal process timings are synchronized with a SYNC signal (16 msec interval clock)

Each measuring parameter signal is processed as follows.

3-1-1 Electrocardiogram (ECG) Signal

On the ECG Head Amp board (UP-0272), two leads of an ECG signal are pre-amplified and time-shared to be one signal (2ch ECG).
On the JA I/F Main board (UP-0270), a 2ch ECG signal is demultiplexed to be the two leads of an ECG signal (ECG1 & ECG2). The output signal is kept to be 15 times as much as the input signal on UP-0272 so that a polarization voltage (DC component) on a electrode causes saturation since ECG1 and ECG2 signals include a DC component.
On the DPU board (UP-0670), ECG1 and ECG2 from the UP-0270 are amplified to be 1V to 15mV through 15mV calibration, the Pacing pulse limiter circuit, DC eliminator time constant selector and Auto-instantaneous short circuit. ECG1 and ECG2 are converted to digital signals through the HUM filter ON/OFF selector while ECG1 and ECG2 are branched to be ECG1W and ECG2W signals for the recorder (WS) or central monitor (CNS). ECG1W and ECG2W are real-time signals through the Low-pass filter ON/OFF selector since the A-D and D-A converter circuit cannot minutely reproduce the high frequency component (up to 100Hz).

3-1-2 Respiration Signal

On UP-0272, impedance variation(Ω) between electrode "R"(RA) and "F"(LL) led by respiration is transferred to the transformer (T003).
On the RESP Amp board (UP-0271), the impedance variation induces the minute amplitude variation on an 80kHz sine carrier wave. The minute signal is amplified up to 50 mV/Ω, including the DC component.
On UP-0670, the signal is amplified up to 1V/Ω, excluding the DC component, and converted to a digital signal.

3-1-3 Blood Pressure Signal

On the PRESS Head Amp board (UP-0369), Blood pressure signals P1 and P2 are individually amplified, time-shared with the analog switch (IC003A), modulated/demodulated with the 64kHz clock (F-CLK) for floating and outputted to UP-0670 up to 1 V/100 mmHg.
On UP-0670, the signal is inputted to the 16ch multiplexer, doubled by the Gain selector circuit, added to the ADSFT signal to shift DC level in auto-zeroing operation and converted to a digital signal. Blood Pressure signal for WS or CNS is the output signal (P1W to P4W) after D-A converter (8 msec sampling).

3-1-4 Cardiac Output (CO) Signal

On the CO Head Amp board (UP-0318), the following four signals are time-shared during a 16msec interval on a SYNC signal.

1) REF: 0 V Reference voltage for 0 °C in Ti or 27 °C in Tb
2) Ti: Voltage for Injection fluid temperature (1 V/10 °C)
3) Tb: Voltage for Blood temperature (1 V/5 °C)
4) ΔTb: Voltage for Blood temperature variation in fluid injection (1V/0.5 °C)

On UP-0670, the signals are converted to digital signals synchronized with the output from UP-0318.

3-1-5 Temperature Signal

On TEMP Head Amp board (UP-0319), the following four signals are time-shared during a 16 msec interval on a SYNC signal.

1) REF27: Reference voltage for 27 °C in T1 or T2
2) CAL37: Calibration voltage for 37 °C (1V/5 °C)
3) T1: Voltage for Temperature-1 (1 V/5 °C)
4) T2: Voltage for Temperature-2 (1 V/5 °C)

On UP-0670, the signals are converted to digital signals synchronized with the output from UP-0319.

3-2 Main Unit, MU-881R

3-2-1 COM3 Board, UP-0563

◆ General

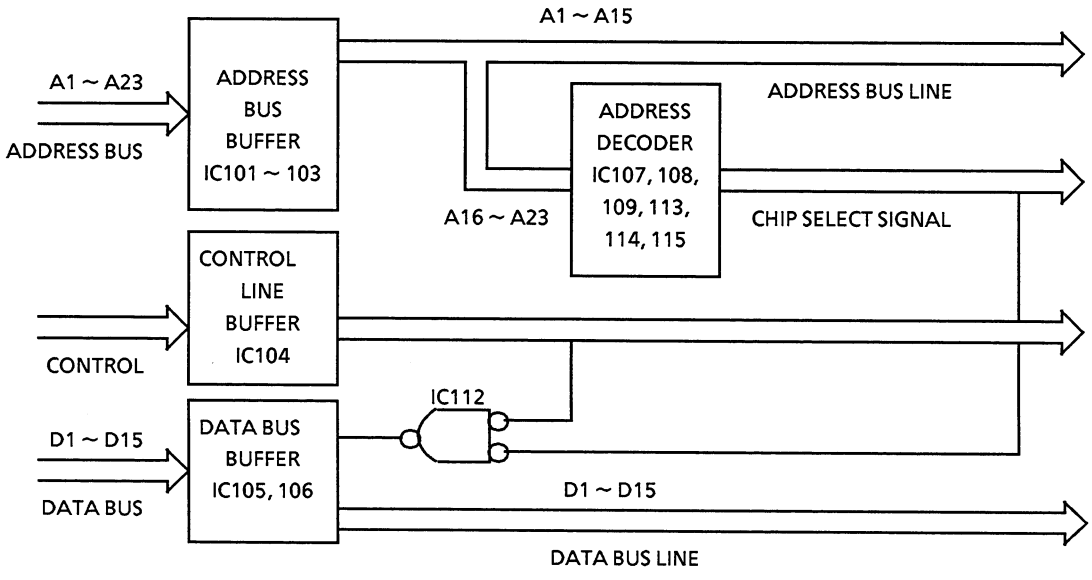
The COM3 board mainly functions as CNS interface and WS recorder interface through the dual-port RAM.

◆ Decoder

• Address decoder, Buss buffer

IC101,102 and 103(HCT240) are used for the buffer of address bus.
IC104(HCT244) is used for the buffer of control line.
IC105 and 106 (HCT640) are used for the buffer of data bus.
IC107,108(HC138),IC113(HC130),IC114(F04) and IC115(F20) are used as address decoder.
IC112(HC32) operates as gate opener & closer of data buss buffer.
In decoder part, each chip select signal(CS) is asserted by following devices.

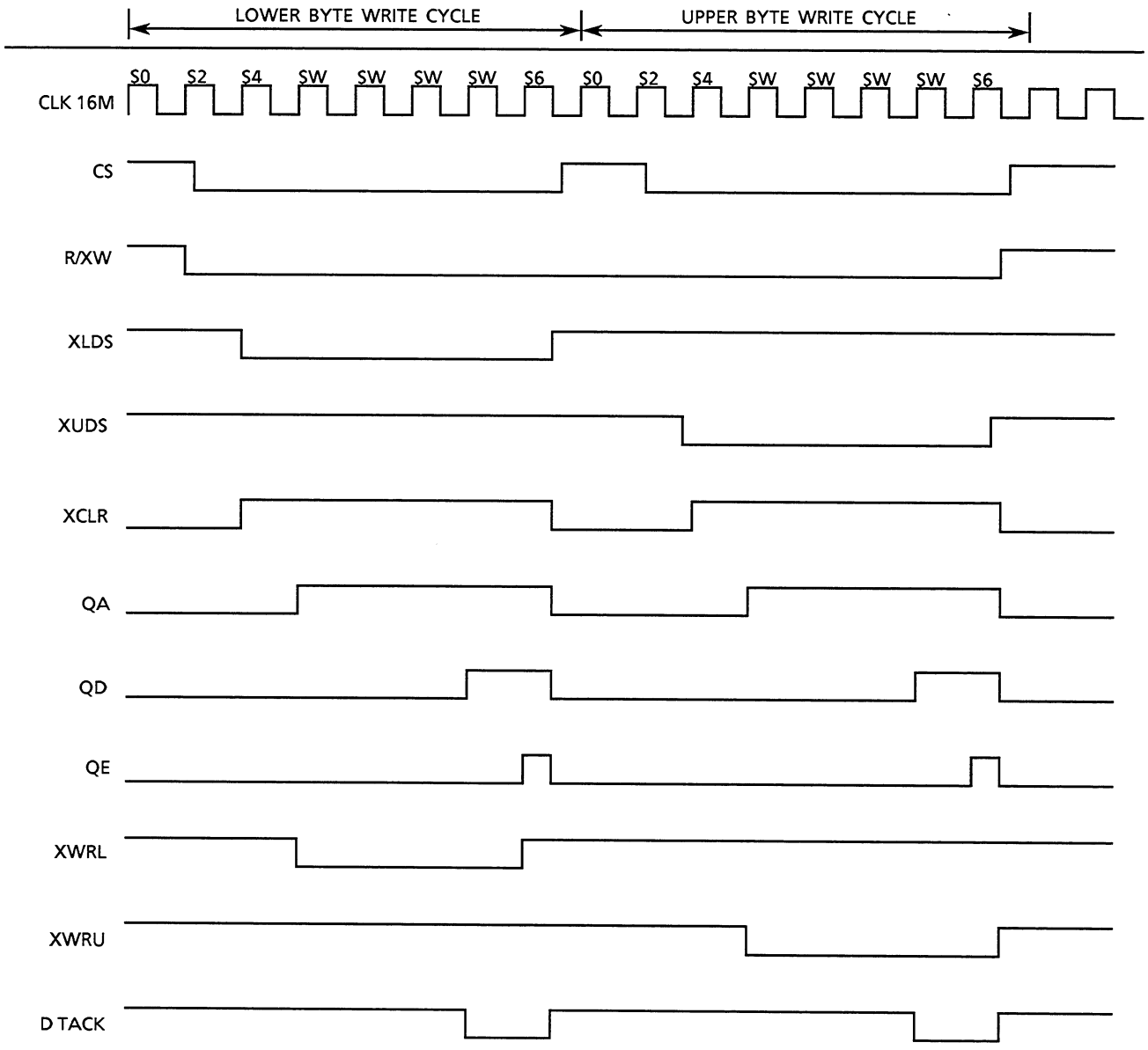
CS	DEVICE
XCS3	ROM 128 KByte
XCS4	SRAM 64 KByte
XCS5	SRAM 64 KByte
XCS1	MB8421(2 port RAM,using lower byte only)
XCS0	WS Recorder RESET port(IC118)



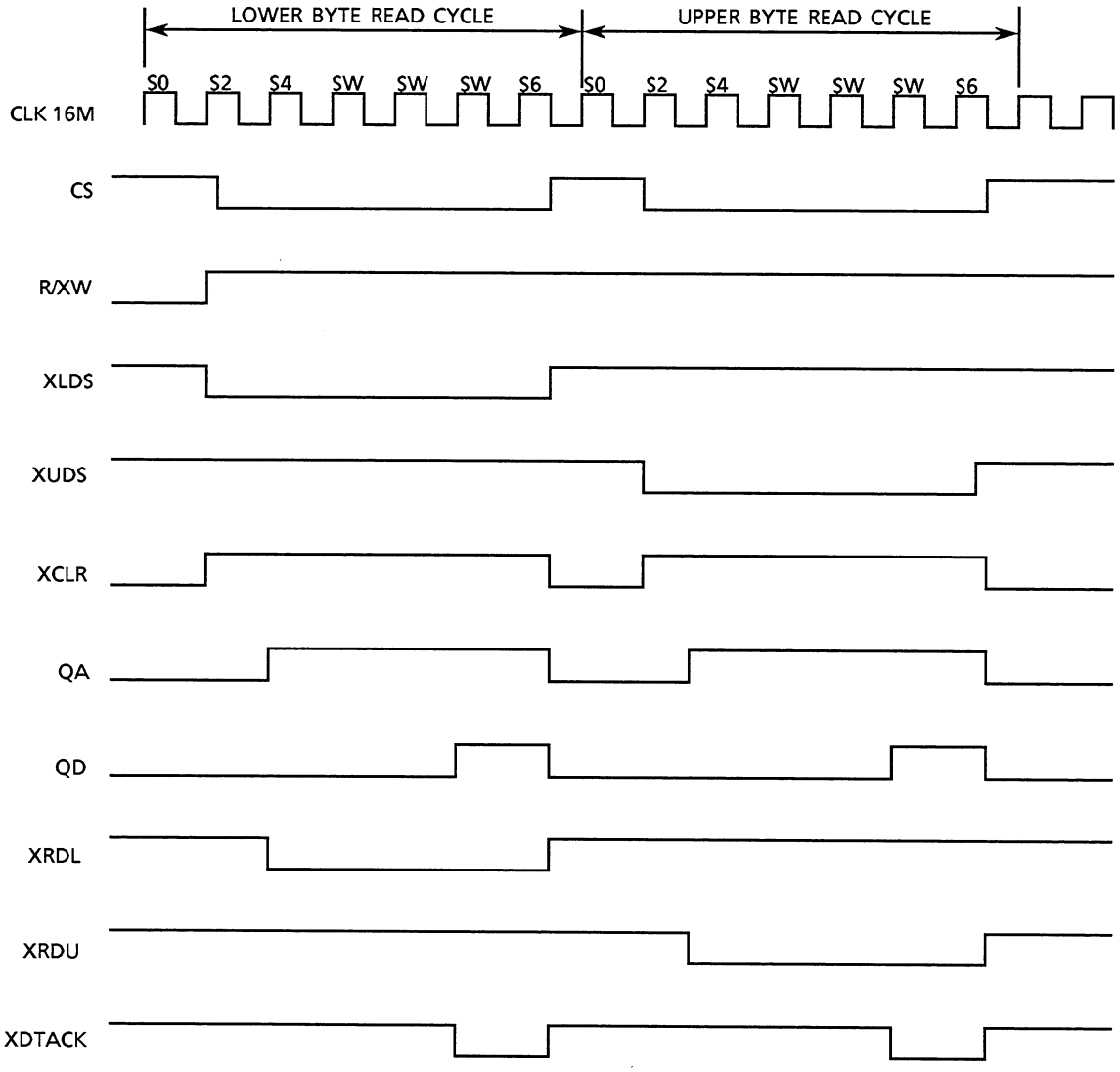
• XWR,XRD,XDTACK Generator

When CPU68000 on the CPU board accesses COM3 board, the decoder operates and the chip select signal on IC116(F164) falls into assert condition "H".
If the request from CPU board comes later than XBUSYR, the CPU request falls into wait condition.

*** WRITE CYCLE TIMING CHART**



*** READ CYCLE TIMING CHART**



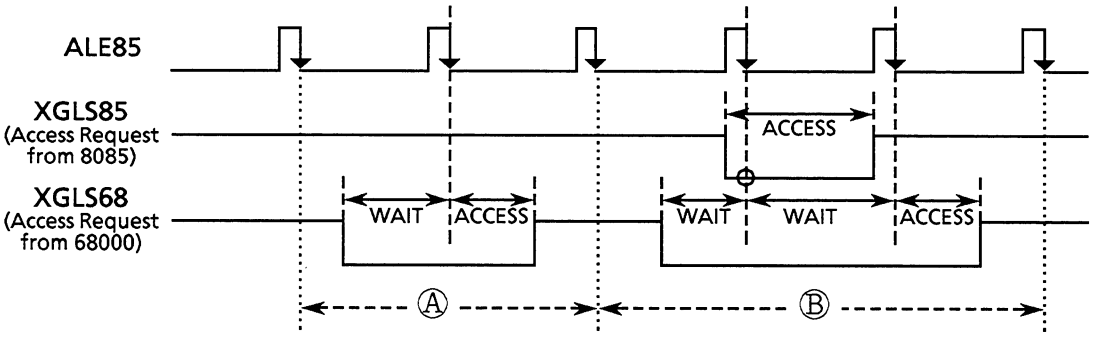
◆ Global Memory & Control Circuit

• Global Memory Control circuit

The circuit controls the access request to the global memory (IC012) RAM from both MPUs (8085 on this board and 68000 on the CPU board).

1) Access Priority Timing Chart

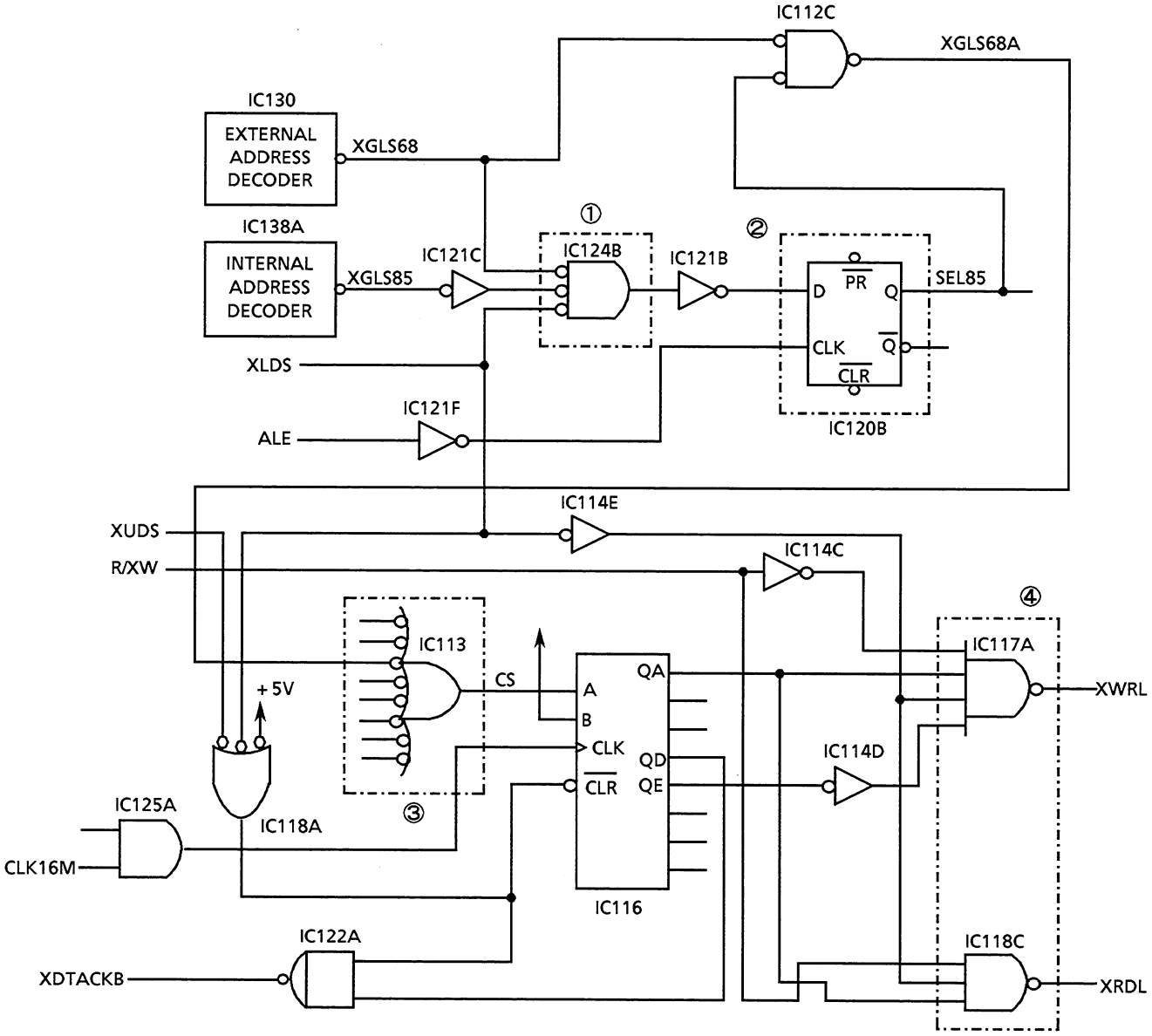
The access to the RAM (IC012) from the MPU8085 always governs.
The access to the RAM (IC012) from the MPU68000 is done according to the following timing chart.



Ⓐ When there is an access request from the MPU68000 only, the circuit accepts the access from the MPU68000 and starts the access with the negative going edge of ALE85 signal.

Ⓑ When there are access requests from both the MPU8085 and 68000, the circuit leads the access from the MPU8085 and starts with the negative going edge of ALE85 signal. After completing the access from the MPU8085, the circuit starts the access from the MPU68000 with the next negative going edge of ALE85 signal.

2) Access Priority Judgment Function



① When there are access requests from both the MPU8085 and 68000, the circuit blocks the access request from the MPU68000.

② The circuit judges whether there is an access request from the MPU8085 at the negative going edges of ALE85 signal.

③ When there is an access request from the MPU8085 (SEL85: High level), the Shift Register (IC006) is not reset and doesn't transfer the XDTACK signal to the MPU68000. Therefore, the MPU68000 keeps on waiting for access to the RAM (IC126) until the access from the MPU8085 is completed.

④ The circuit blocks the control signals to the RAM (IC126) from the MPU68000, XWRL & WRDL, under the above condition ①.

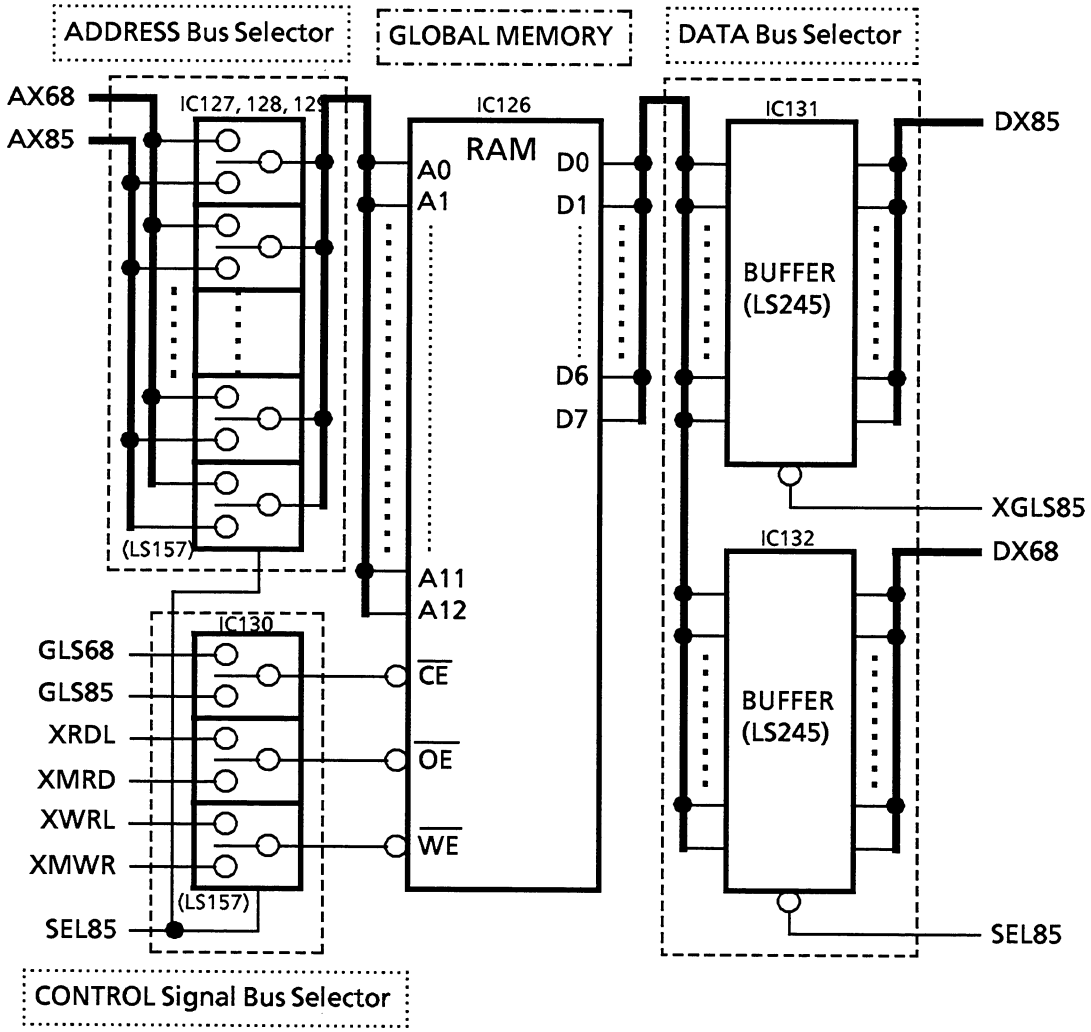
• **Global Memory circuit** (Bus Selector)

The circuit (Bus selector) selects the Internal Bus (from 8085) or System Bus (from 68000) to connect with the global memory RAM (IC126) according to the Global Memory Control circuit.

The bus selector consists of the Address Bus Selector, Control signal Bus Selector and Data Bus Selector.

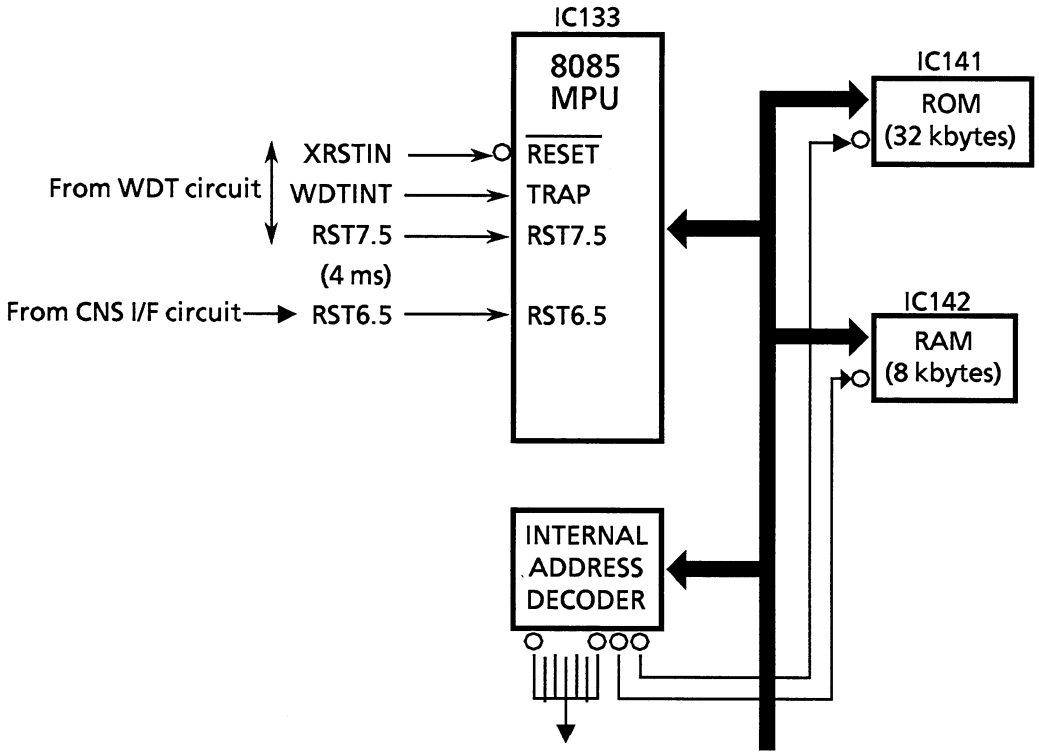
The former two are controlled by the Analog Switches (IC025/039/040, 024), LS157.

The latter one is controlled by the Buffer (IC131, 132), LS245.



◆ **CNS Interface**

• **CPU/ROM/RAM circuit**

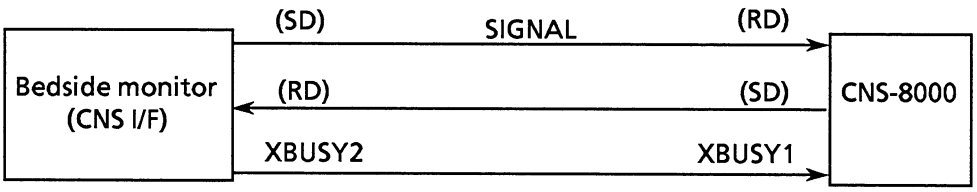


The circuit consists of MPU8085 (IC053), ROM (IC141), RAM (IC142) and the Internal Address Decoder.
The circuit controls the other circuits on the COM3 board.
The MPU8085 on the circuit provides the following Input/Output for Control signals.

Pins	Description
RESET	Reset Input
TRAP	Watch Dog Timer Error Interrupt Request Input
RST7.5	Periodic Interrupt Request Input (every 4msec)
RST6.5	Interrupt Request Input upon receipt of Address/Command signal from CNS (I/F)

• CNS I/F (Interface) circuit

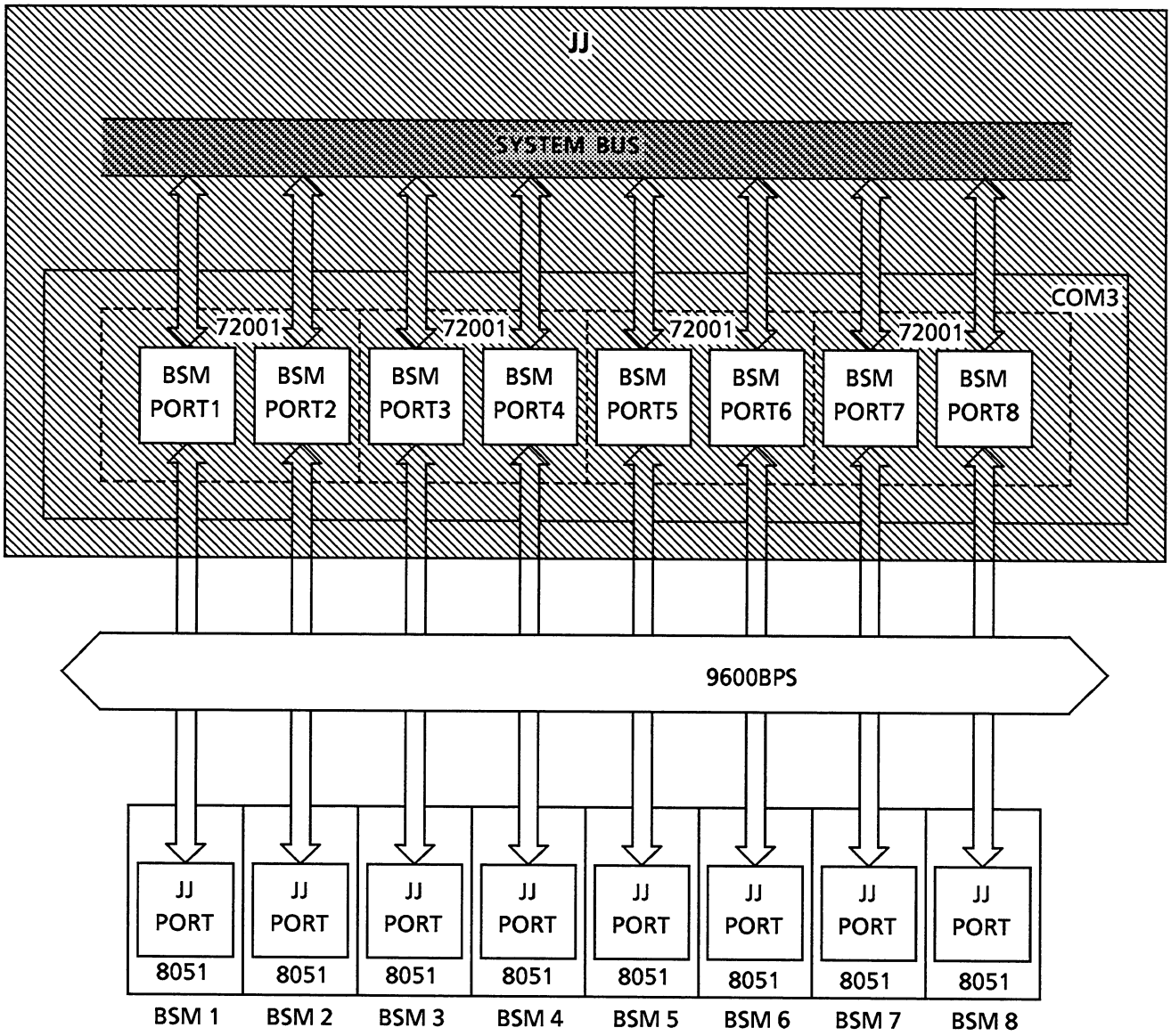
The circuit provides communication functions with the Central Monitor (CNS-8000 series) as follows:



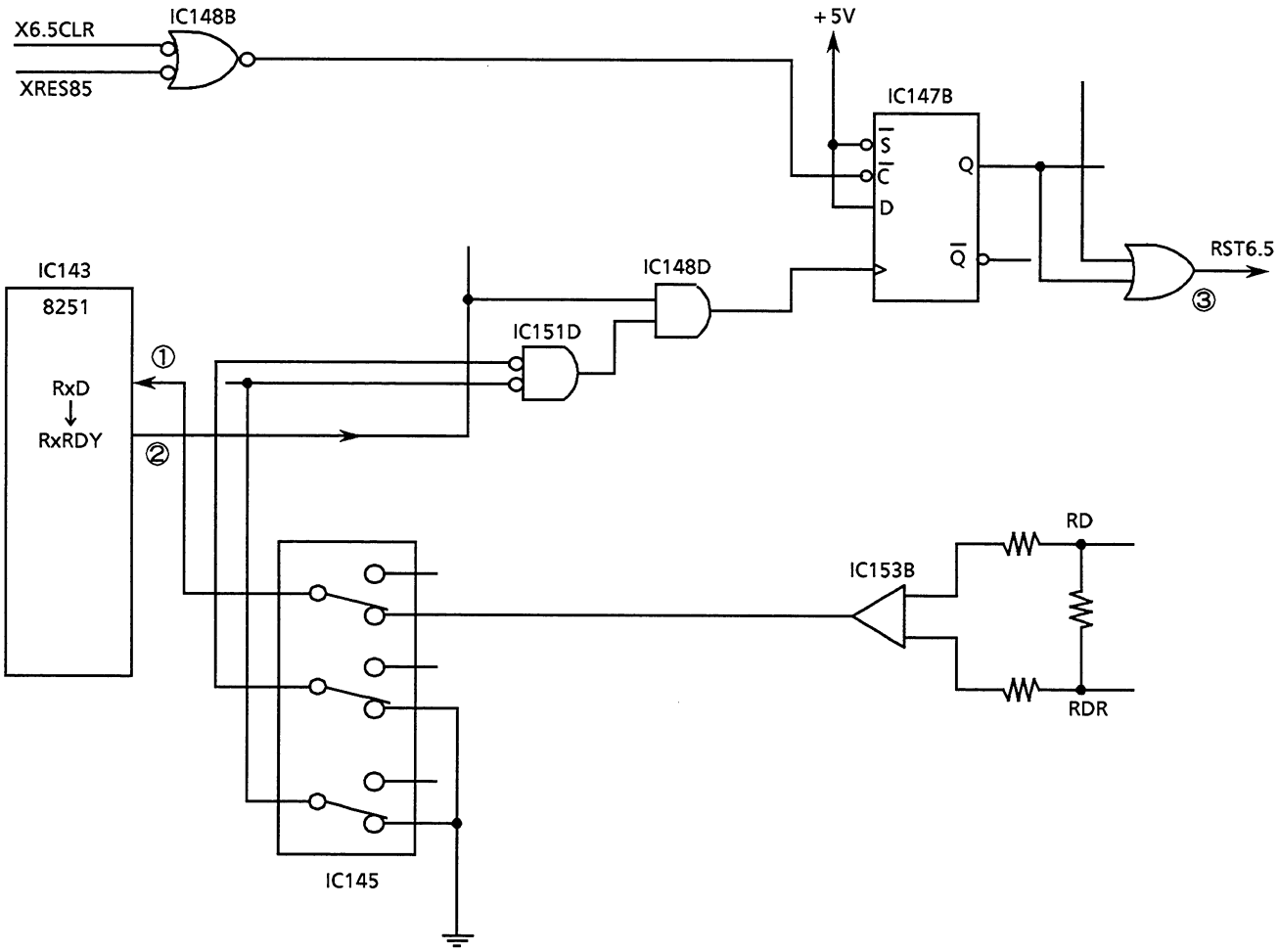
Symbol	Transfer direction	Description
SD	MONO	Send Data (asynchronous, 9600 bps)
RD	MONO	Receive Data
XBUSY2	MONO	Data is transferring to CNS and any request signal is rejected

• BSM-JJ communication sequence

Each bedside monitor communicates independently with the independent port of JJ. The communication method is a double-asynchronous method with baud rate of 96000 bps.



• Address Receive operation



① A receive data is transferred to the RxD terminal on the IC143 from CNS through the SIGNAL line.

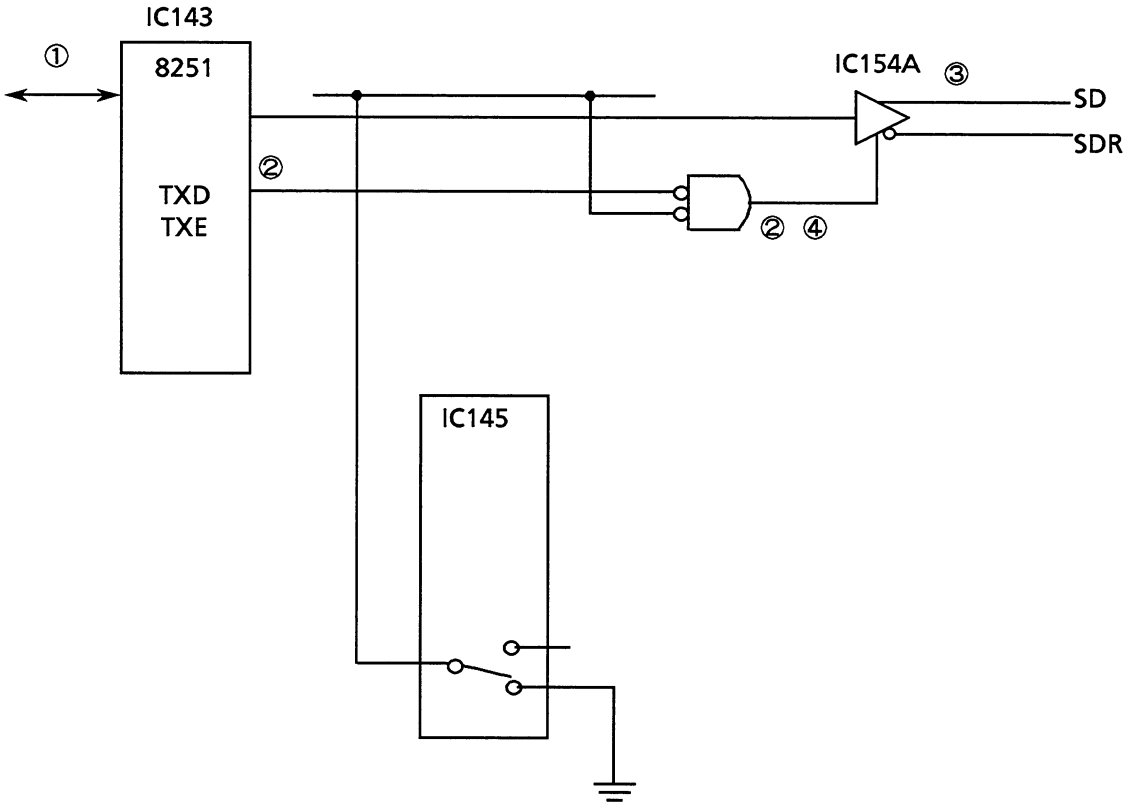
② Receive Interrupt Request signal RxRDY is asserted while the data is set on the Receive Register in the IC143.

③ Interrupt Request signal to the MPU8085, RST6.5, is generated.

When RST6.5 is generated, the MPU8085 reads the data on the Receive Register.

After reading the data, RxRDY is cleared and RST6.5 is also reset.

● **Data Transmit operation**



① A transmit data is set on the Transmit Register in the IC143 (8251) by the MPU8085.

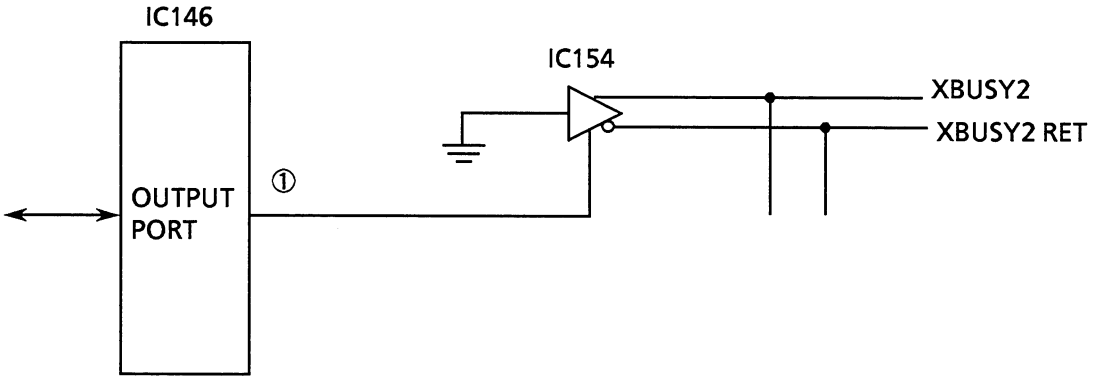
② A receive data is blocked while the Transmit Driver (IC145) is set to enable by setting the TxE signal to be active-low.

③ The transmit data is transferred to the SIGNAL line.

④ When the transmit data is completed to transfer, the Transmit Driver is set to disable by setting the TxE signal to be inactive-high.

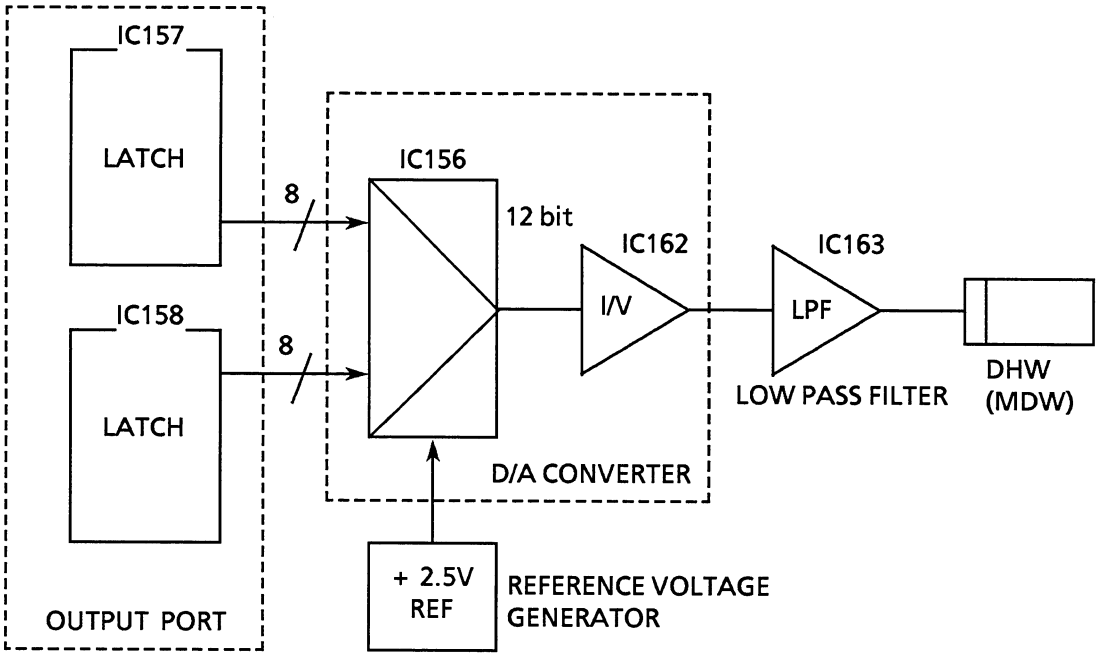
●"BUSY" signal Transmit operation

When the processing work of MPU8085 is going to be overload,XBUSY control signal is set to active in order to let the transmit operation from JJ wait.

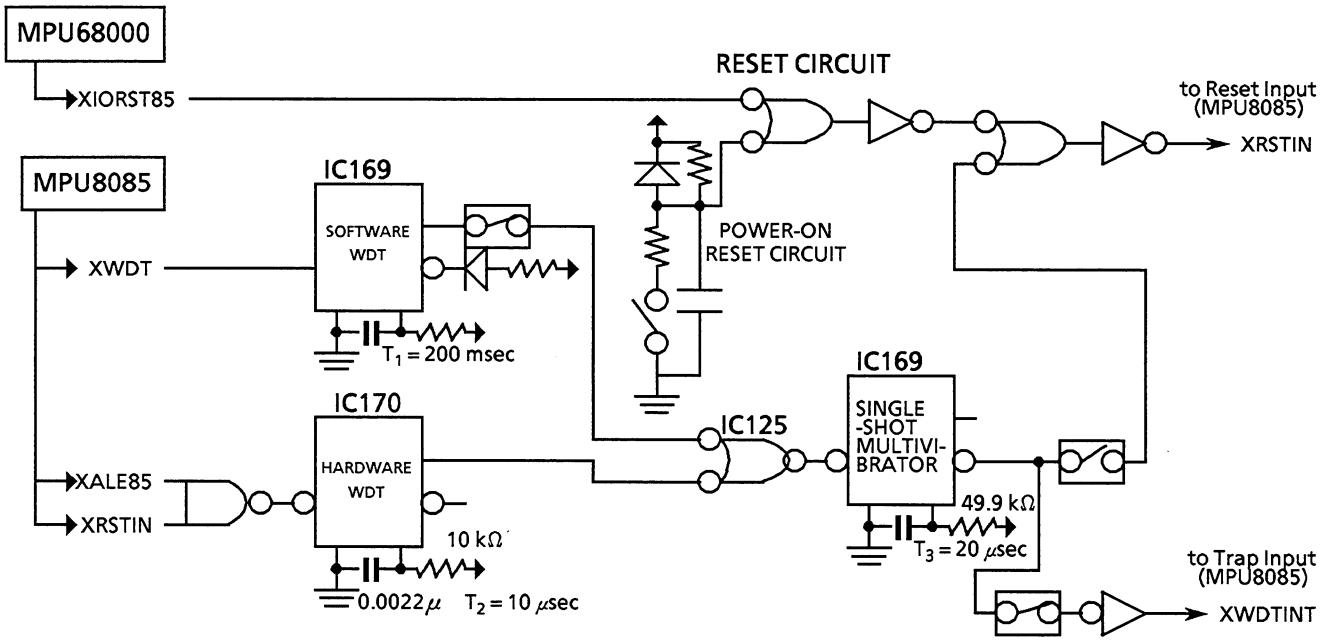


◆ Delayed ECG Waveform(MDW) Generator

The delayed ECG waveform is generated by this part to transmit them to CNS for remote recording.
The circuit consists of Output port, D/A converter, Low pass filter, and Reference voltage generator.
The delayed ECG waveform,which is obtained CPU board through global memory, is output at every 4ms to output port of IC157/158 by CPU(IC133) of COM3 board.
The reference voltage generator supplies DC + 2.5 V to D/A converter.



◆ **WDT/LED/SW Circuit**



• Watch Dog Timer (W.D.T.) circuit

If the MPU8085 runs away, the circuit generates a TRAP Interrupt Request signal, WDTINT.

The circuit consists of the Software WDT and Hardware WDT.

*** Software WDT**

The software WDT, Single-shot Multivibrator (IC169), keeps on outputting "High" level by receiving a periodic access signal controlled by software, XWDT. If the XWDT signal is not transferred to the IC169 for 200msec. or more, the IC169 output terminal (Q) is set to "Low" level from "High" level due to the Timeout.

*** Hardware WDT**

The hardware WDT, Single-shot Multivibrator (IC170), keeps on outputting "High" level by receiving an Address Latch Enable signal from the MPU8085, XALE85. If the XALE85 signal is not transferred to the IC170 for 10 μsec or more, the IC170 output terminal (Q) is set to "Low" level from "High" level due to the Timeout.

Both outputs of the IC169 and IC170 are connected to the IC035 (Wired OR).
The output of the IC035 is processed to be 20 μsec width pulse by the single-shot multivibrator (IC169B) if either IC169 or IC170 is set to "Low" level. The 20 μsec width pulse goes to the TRAP terminal of the MPU8085 to interrupt the MPU operation.

• Reset circuit

The circuit generates a Reset signal (XRSTIN) and sends it to the Reset terminal of the MPU8085 in the following cases.

2-1)Power-on Reset circuit

The XRSTIN signal is generated for 100 msec after turning on the power switch.

2-2)Reset Command from CPU board XIORST

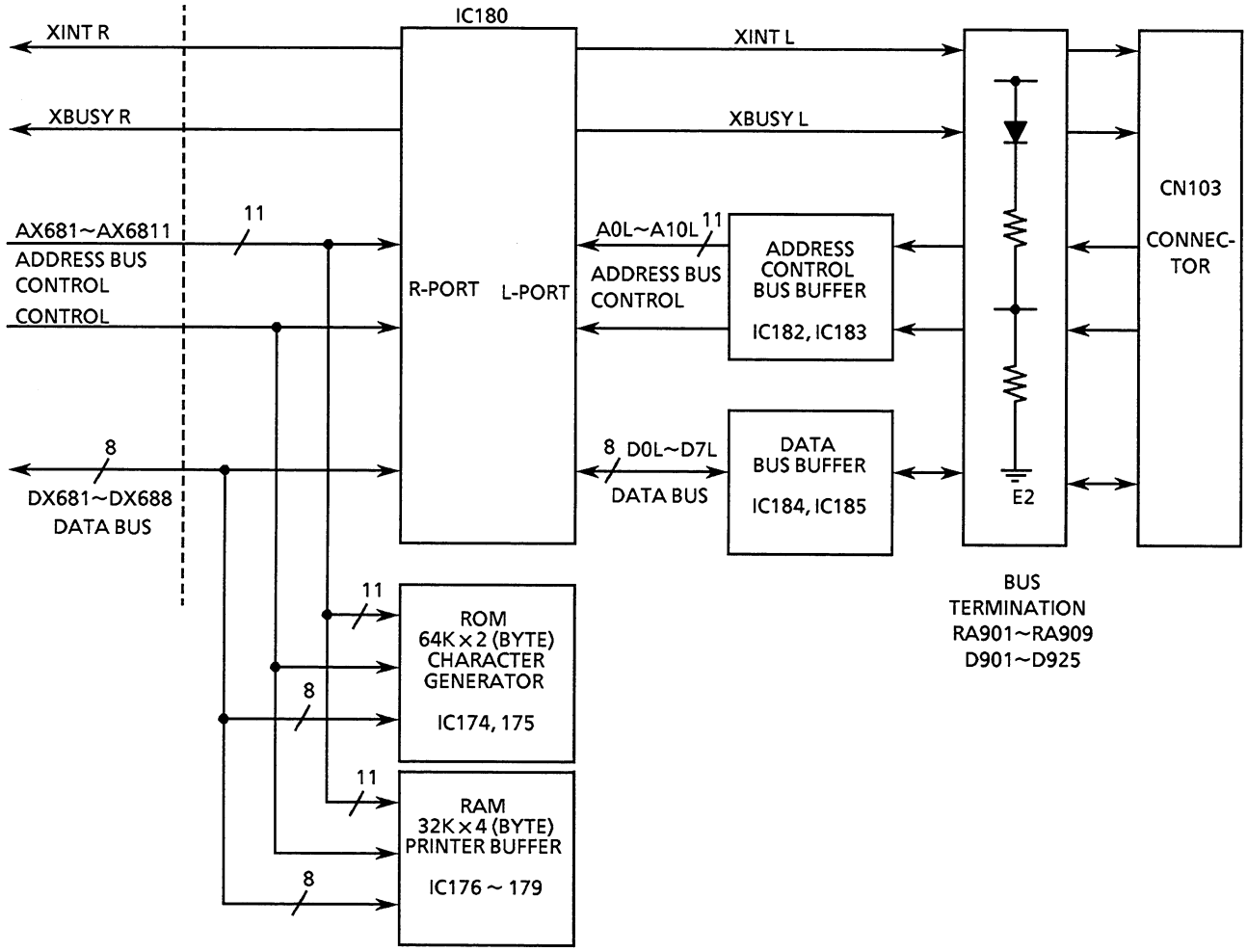
The XRSTIN signal is generated by the XIORST signal through the decoder from the MPU68000 on the CPU board.

2-3)Reset Switch SW103

The XRSTIN signal is generated by depressing the SW103. The SW103 is provided for debugging.

◆WS Interface

• General



Dual port RAM IC180 (MB8421) is for receive/transmit data and command between the COM3 board and the externally connected thermal array recorder.
Address bus, data bus and control lines from the CPU that control the COM3 are inputted to the IC180 R (right) port while address bus from the WS-841R is inputted to the IC180 L (left) port. This address bus is inputted from the CN103 connector (WS) on the rear panel of the main unit and connected to the IC180 L port through the terminator composed of resistors and diodes, and address bus buffer composed of IC182 and IC183 (LS244). In the same manner as the address bus lines, control lines are connected to the IC180 L port through the bus terminator and buffer.
Data bus lines from the thermal array recorder are inputted from the CN103 and after bus terminator, the lines are buffered by different buffers during read cycle and write cycle.

* **Write cycle**
  Data is connected to the IC180 data bus through the data bus buffer IC184 (LS244).

* **Read cycle**
  Data is outputted from the IC180 and connected to the WS-841R through the data bus buffer IC185 (LS641). XINT and XBUSY signal from the IC180 L port are inverted by IC186 (LS04) to change the format to open collector output and inverted again by IC187 (LS38). These reinverted lines are also of open collector output format.
  XINT signal from the IC180 R port is buffered twice by IC186 (HC04) and inputted to the XINT11 terminal.
  XINT and XBUSY lines on both R and L ports are pulled up by 4.99kohm resistors to match the signals to the open drain format XBUSY and XINT terminals of the device.
  XINT and XBUSY lines on both R and L ports are open collector outputs to avoid the break down of CPU on WS by power failure during the recording

• Printer Buffer, Character Generator

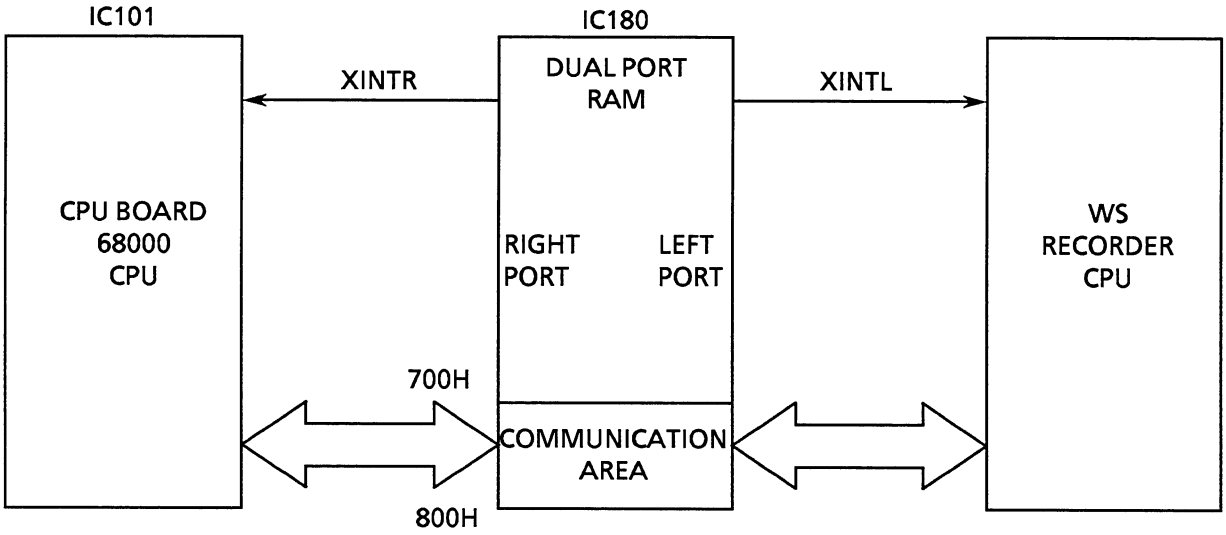
IC174,175 are used as a character generator for WS recorder.

IC176 ~ IC179 are used as a printer buffer for WS recorder.

XINT signal is a interrupt signal to CPU on the CPU board and CPU on WS.

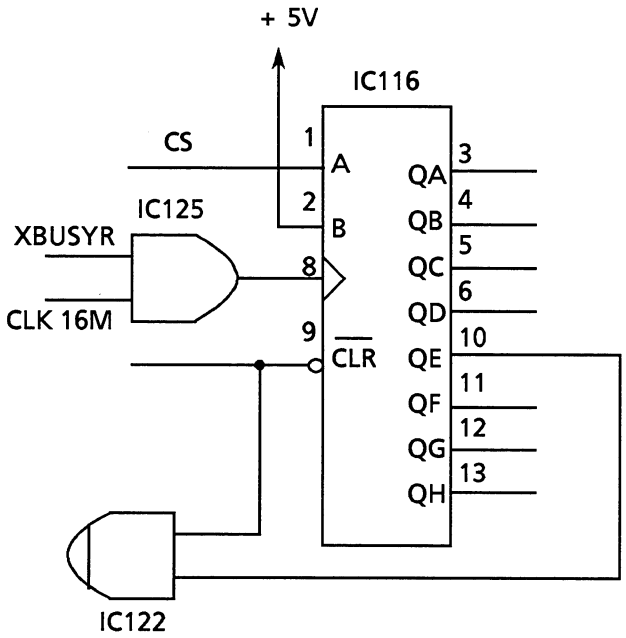
For example, when the data is written on address 7FFH of R port of Dual-port RAM from CPU, XINTL is generated.

XINTL is used for the direct communication between CPU on the CPU board and WS.

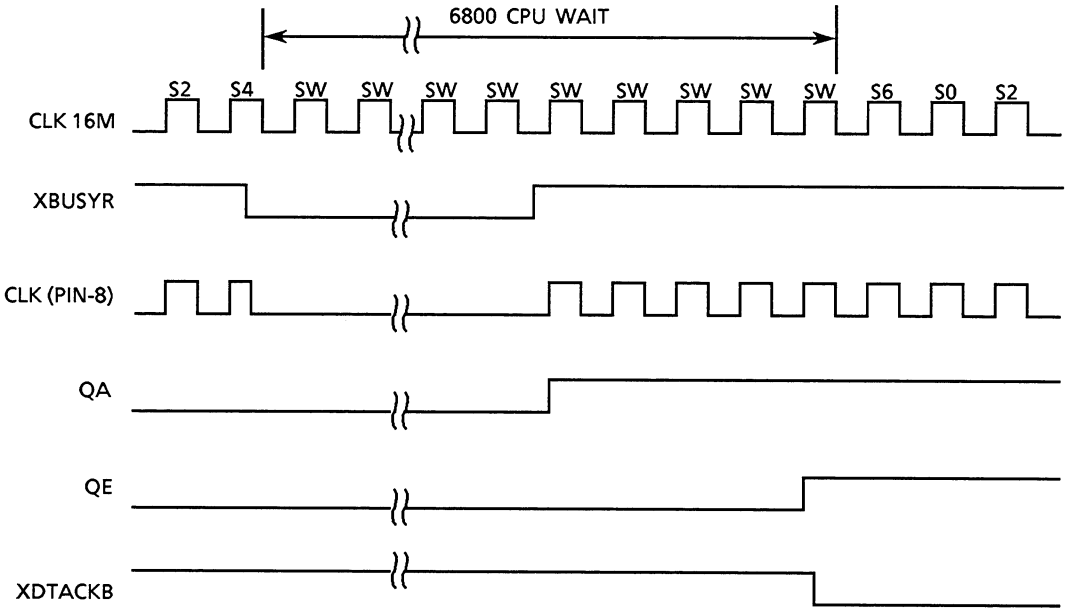


• Access Address Competition Avoidance(XBUSY signal)

On Dual port RAM, when the same address on the both port is accessed by "WRITE" and "READ"signals, the data on "READ" side may be changed during the read cycle.
In order to avoid the above matter, "XBUSY" signal us output from IC180(MB8421).
When the same address is accessed,the latter access signal(from CPU) is rejected and and XBUSY signal is asserted.



XBUSY Timing Chart

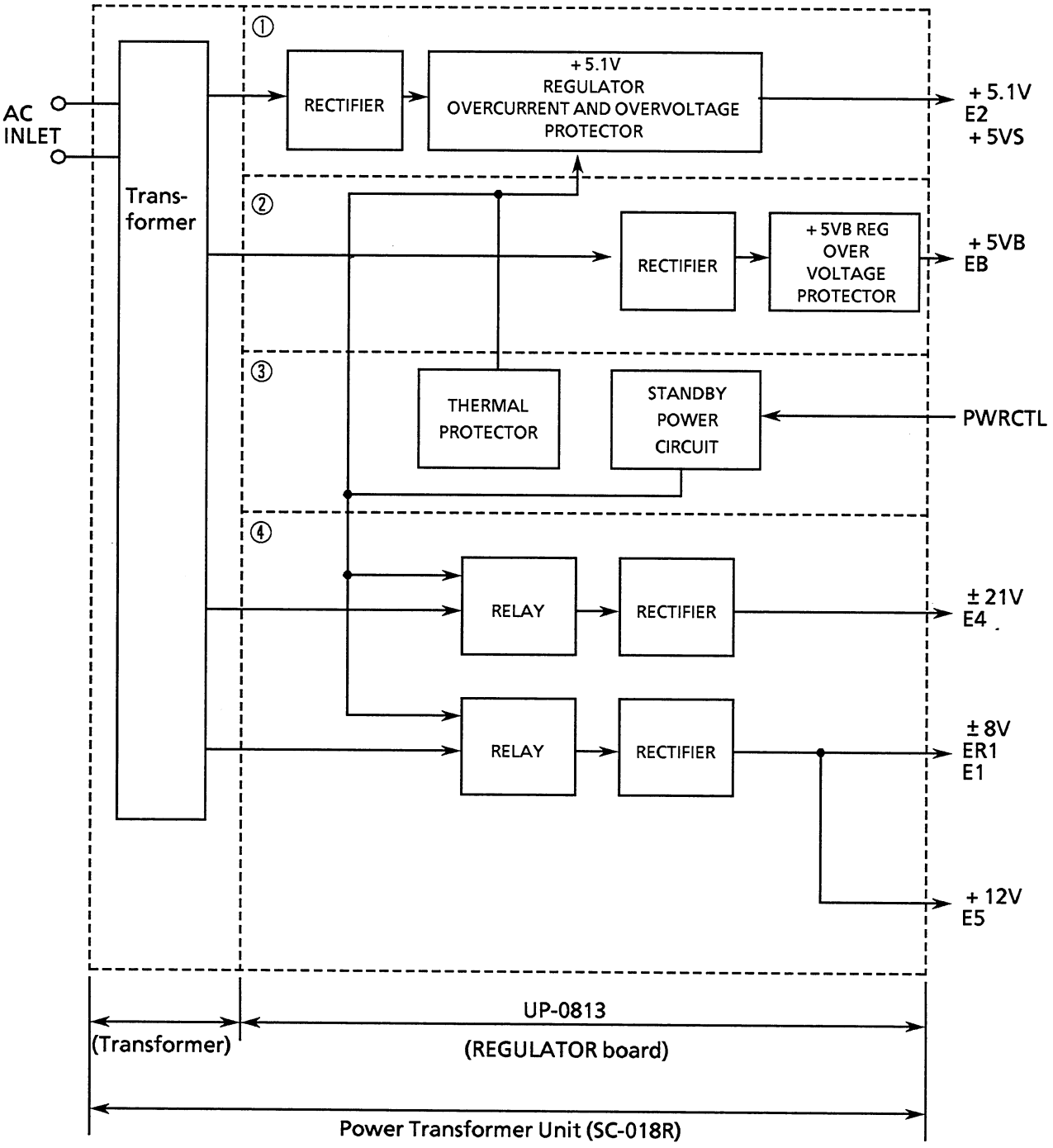


3-2-2 Power Transformer Unit, SC-018R

The power transformer unit (SC-018R) consists of the transformer and the regulator board.

◆ **General**

Block diagram



The regulator consists of the following circuits ;
① +5.1V regulating circuit
② +5VB regulating circuit
③ Overheat protector and standby power circuit (for 5VB)
④ ±21, ±8, ±12V power generating circuit

Each power is processed as follows:

Voltage	Processing Method	Use
+5.1V	Chopper Switching	for digital circuit
+5VB	Dropper	for digital circuit
±21V	Unregulated	for analog circuit
±8V	3 terminal output regulator	for analog circuit
+12V	Unregulated	for fan motor

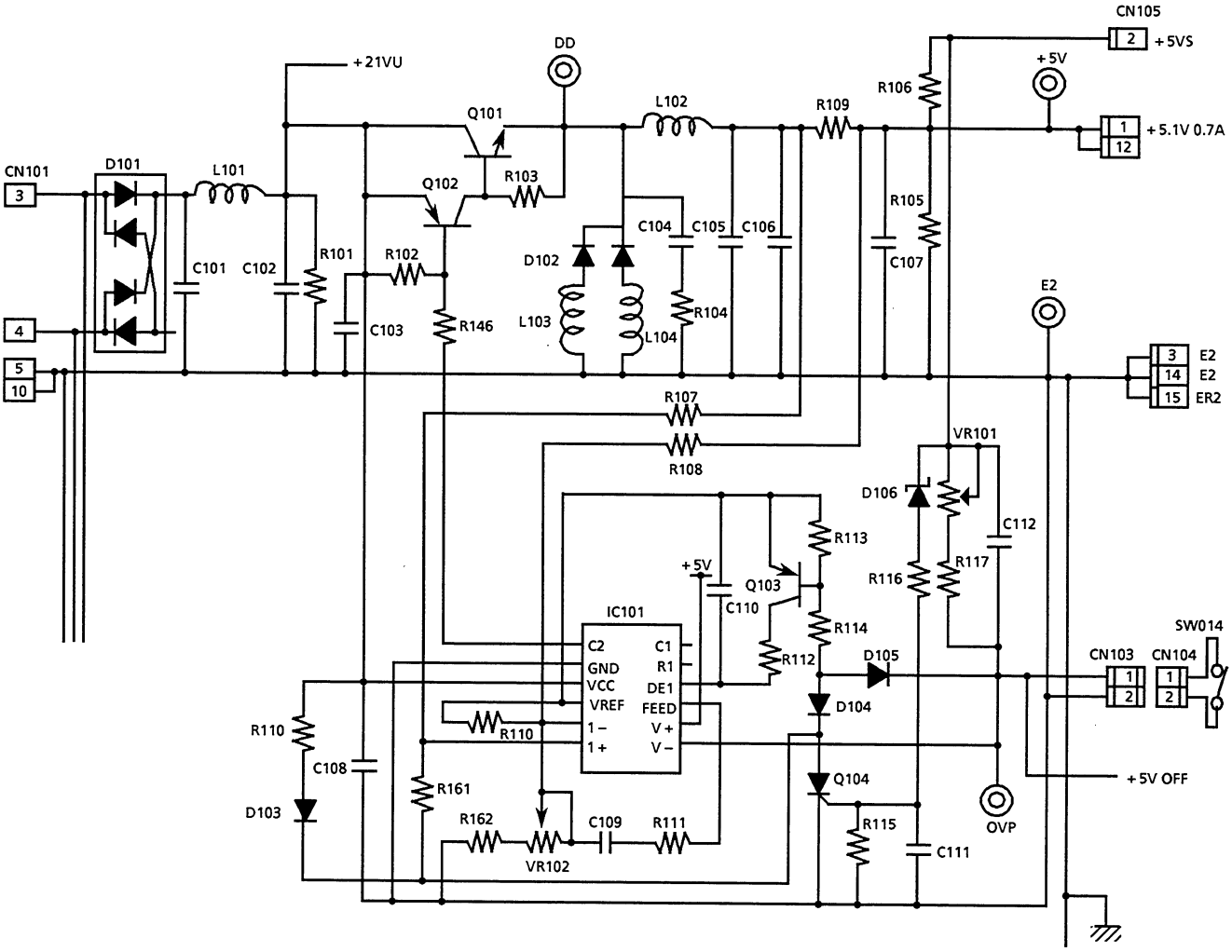
Refer to section 1-9 for the Power System Diagram.

◆ + 5.1V Regulating Circuit

The circuit consists of the rectifier (D111), overvoltage protector, + 5.1V switching regulator with overcurrent protection.

• Overvoltage Protector

The circuit protects all the parts against overvoltage as follows:
When the + 5.1V power supply exceeds + 6V, the Thyristor (Q104) is turned on since a voltage drop across the Zener diode (D106) is more than + 6V of zener voltage. The switching regulator, Q101 is set to off since a heavy current is pulled into the Q104 to stop the + 5V power supply.

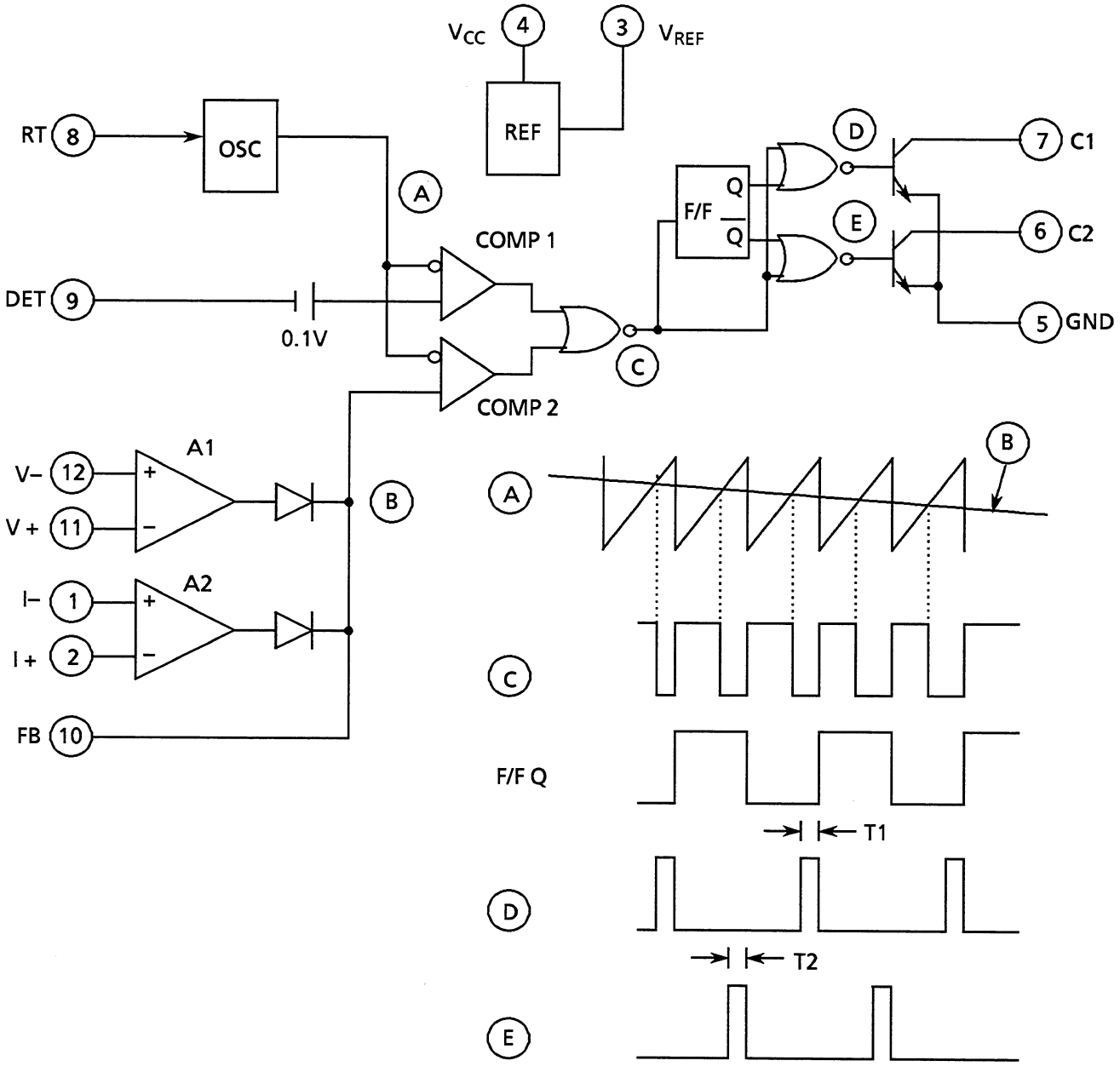


• +5.1V Switching Regulator with Overcurrent Protection

The circuit generates +5.1V Switching regulated power for the digital circuit with pulse width control.

The pulse width control is executed by SWC-01 (IC101), .

IC101 is a custom hybrid IC composed of a Sawtooth Oscillator (OSC), two Comparators (COMP1 and COMP2), two Amplifiers (A1 and A2), and a +5V Reference Voltage Generator.



The COMP1 controls the maximum pulse width in low level to obtain the dead time.
The COMP2 controls the pulse width by comparing the output signal from the A1 and A2 with the sawtooth signal from the OSC.
The A1 functions as a feedback amplifier by feeding back +5V Remote Sense Line (5VS).
The A2 functions as an amplifier with overcurrent protection by feeding back the voltage drop across the resistor (R109).

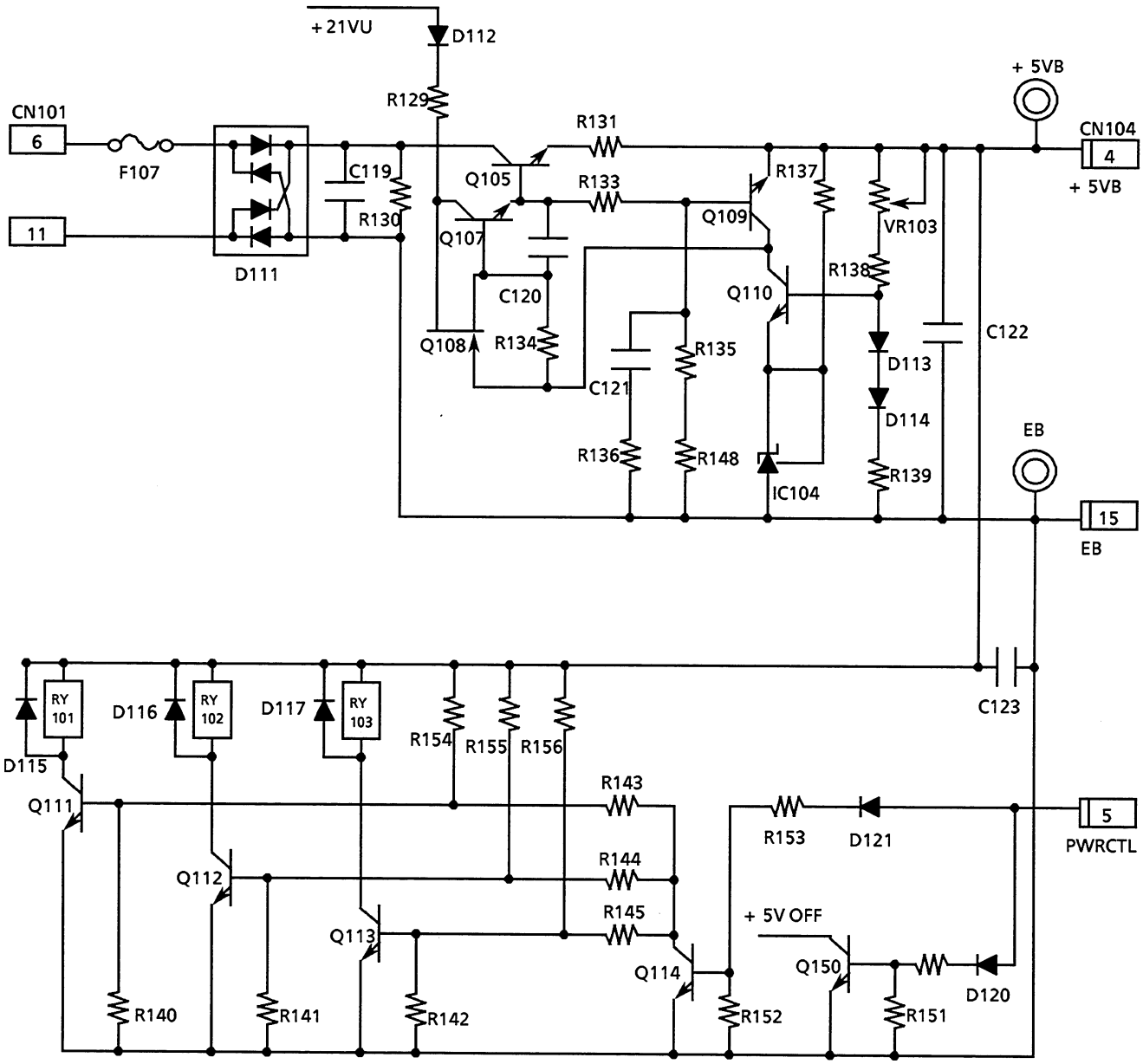
The switching signal from the C2 port of SWC-01, drives Transistors (Q101 & Q102).
The output from the emitter of Q101 is converted to +5V regulated power through the L-C Filter (L102, C105, 106,and 107).

VR101 is an adjustor to set a current value (threshold level) to start the overcurrent protection.

VR102 is an adjustor for the +5.1V regulated power output.

◆ + 5VB Regulating Circuit With Overvoltage Protector

The circuit consists of the rectifier (D111) and a overvoltage Protector. When the +5VB power exceeds +5V, the drop across resistor R131 increases. This switches on the transistor Q109, which in turn, controls the output of the transistor Q105.



◆Overheat Protector & Standby Power Circuit

• Overheat Protector (90°C or more)

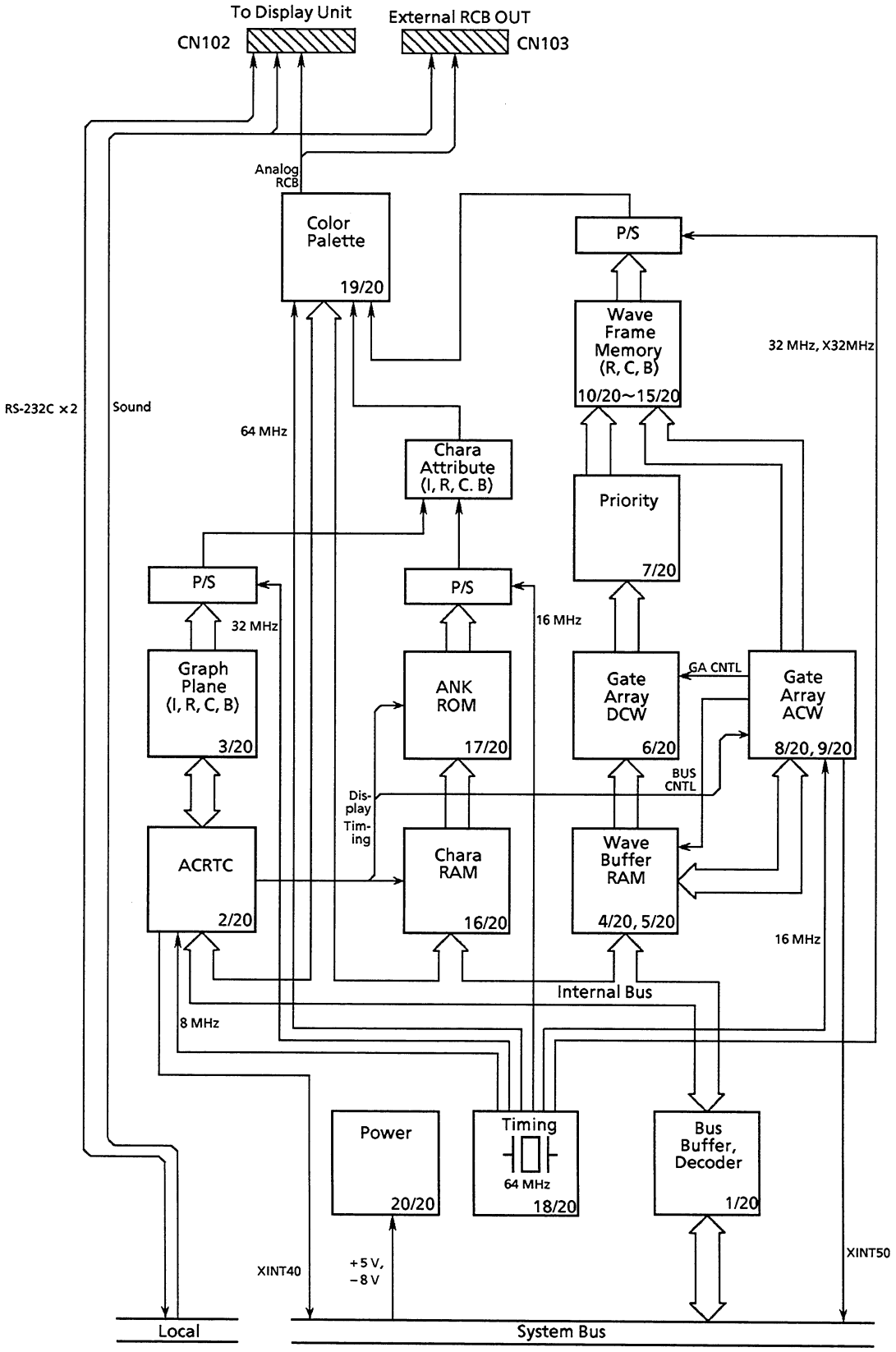
If the main unit warms up to 90°C or more due to a fan motor or other malfunction, the circuit stops the main thermal source, +5.1 V, to protect all the parts against overheating. The thermal switch (SW102) is turned on by overheating (90°C or more) or when the voltage at terminal PWRCTL is +5V. This set the transistor Q101 to off.

• Standby Power

When the voltage at the PWRCTL terminal reads +5 V, the relays RY101 ~ RY103 and transistor Q101 are switched off. This switches off all, except the +5VB power supply

3-2-3 CRTC Board, UP-0795

Block Diagram Description



◆ General

The CRTC board consists of the following circuits.

1) Bus Buffer Decoder Circuit
   This circuit provides the buffer for the system bus as well as generates the bus control signals.

2) Timing Circuit
   The various clock signals used in the CRTC board are derived from a 64MHz oscillator located on this board.

3) ACRTC
   The ACRTC 63484 controls the display timing, and outputs the graphic display control signals to the GRAPHIC RAM.

4) Graph Plane
   The graph plane is used to display up to 4 parameter graphs on the display unit.

5) Character RAM
   This dual-port character RAM contains the character code.

6) Foreign Character ROM and Japanese Character ROM
   There are two character ROMs; one Foreign character ROM and one Japanese character ROM.

7) Wave Buffer RAM
   This RAM stores the waveform data from the CPU board, and the gate array setting data. When the gate array is being accessed, the RAM negates it bus lines to the CPU board.

8) DCW Gate Array
   This circuit interpolates the waveform data before transferring it to the priority circuit.

9) ACW Gate Array
   This controls wave buffer RAM, DCW gate array, and frame memory.

10) Priority Circuit
    This circuit designates the priority level to the various parts of the waveform according to their importance.

11) Wave Frame Memory
    This stores the waveform display data.

12) Parallel/Serial
This shift register converts the parallel video signal to serial video signal.

13) Character Attribute
This supply the display attribute data for the character video signal.

14) Color Palette
The color setting on this circuit is controlled by the CPU board. Then, this circuit adds the color palette code to the video signals to form the R, G, B signals.

◆ Bus Buffer and Decoder Circuit

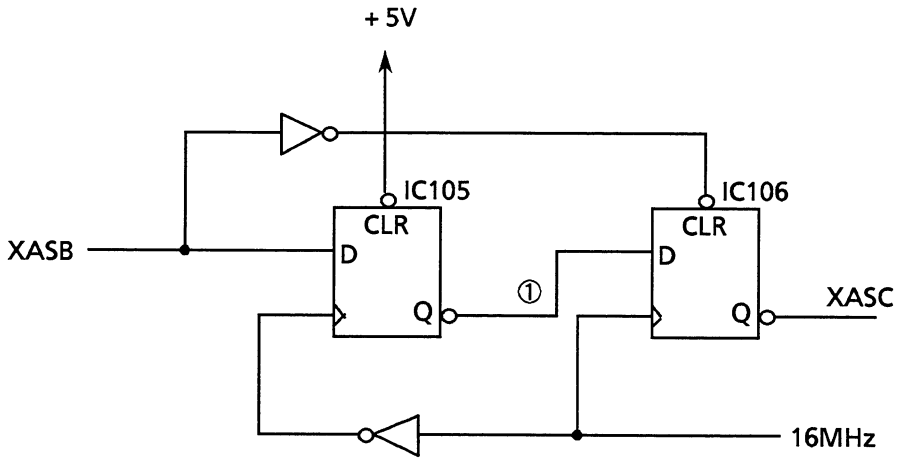
• Data Bus

IC101 and 102 control the input and output of the data according to the commands set by the decoder circuit.

• Address Bus

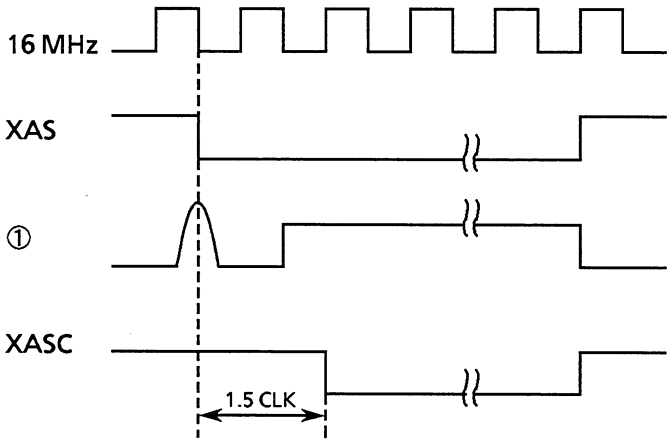
IC103 and 104 is the address bus buffer for waveform data and character data, A1 ~ A16. The address bus A17 ~ A23 go directly to the decoder circuit.

• Control Signal (XAS, XUDS, XLDS, and R/XW)



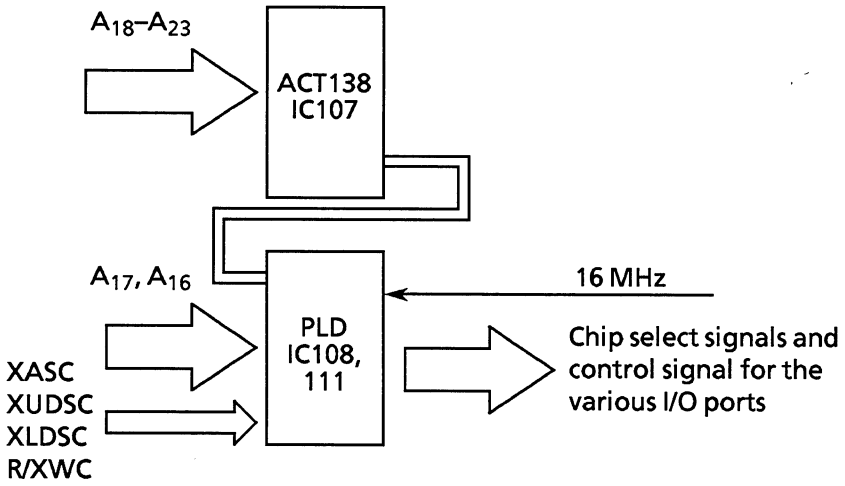
This circuit latches the 16MHz internal clock. The address strobe (XASC) is delayed by 1.5 clock to avoid the metastable condition. The XAS is used to reset the address strobe signal.

The timing chart below shows how the XASC signal is delayed by 1.5 clock.



• Decoder

The IC107, 108 and 111 decodes the address bus A17 ~ A23, and generates the chip select signal and controls signals for the various I/O ports.



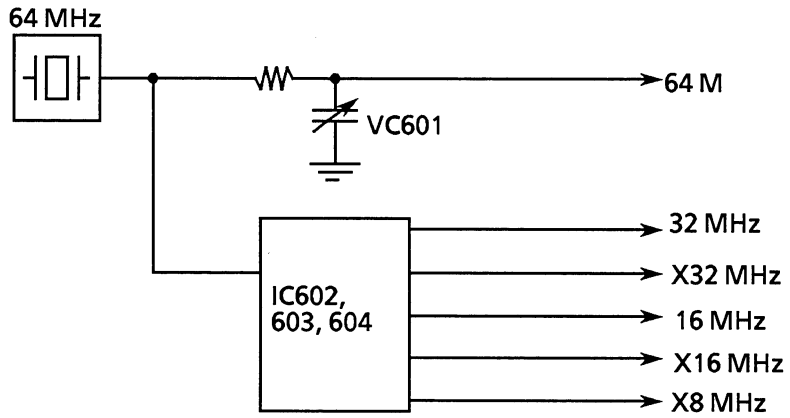
• Data Acknowledge and Interrupt

This circuit informs the CPU when the waveform RAM, ACRTC, CHARA RAM, COLOR PALETTE, AND I/O PORT are accessed. The acknowledge signals passed through a a wired OR circuit (IC109) and outputted as XDTACK signal.

The IC705 separates the interrupt signal from the ACRTC and ACW into the XINT40 and XINT50 signals and outputs them to the CPU.

◆ Timing Generator Circuit

This circuit generates from the 16 MHz system clock the following timing:
* 32 MHz for the waveform display circuit and the graphic display circuit.
* X32 MHz for the waveform display circuit and the graphic display circuit.
* 16 MHz for the waveform display circuit and the character display circuit.
* X16 MHz for the waveform display circuit and the character display circuit.
* X8 MHz for the ARCTC



The VC601 is used for adjusting the latching timing for the waveform, character, and graphic video signals.

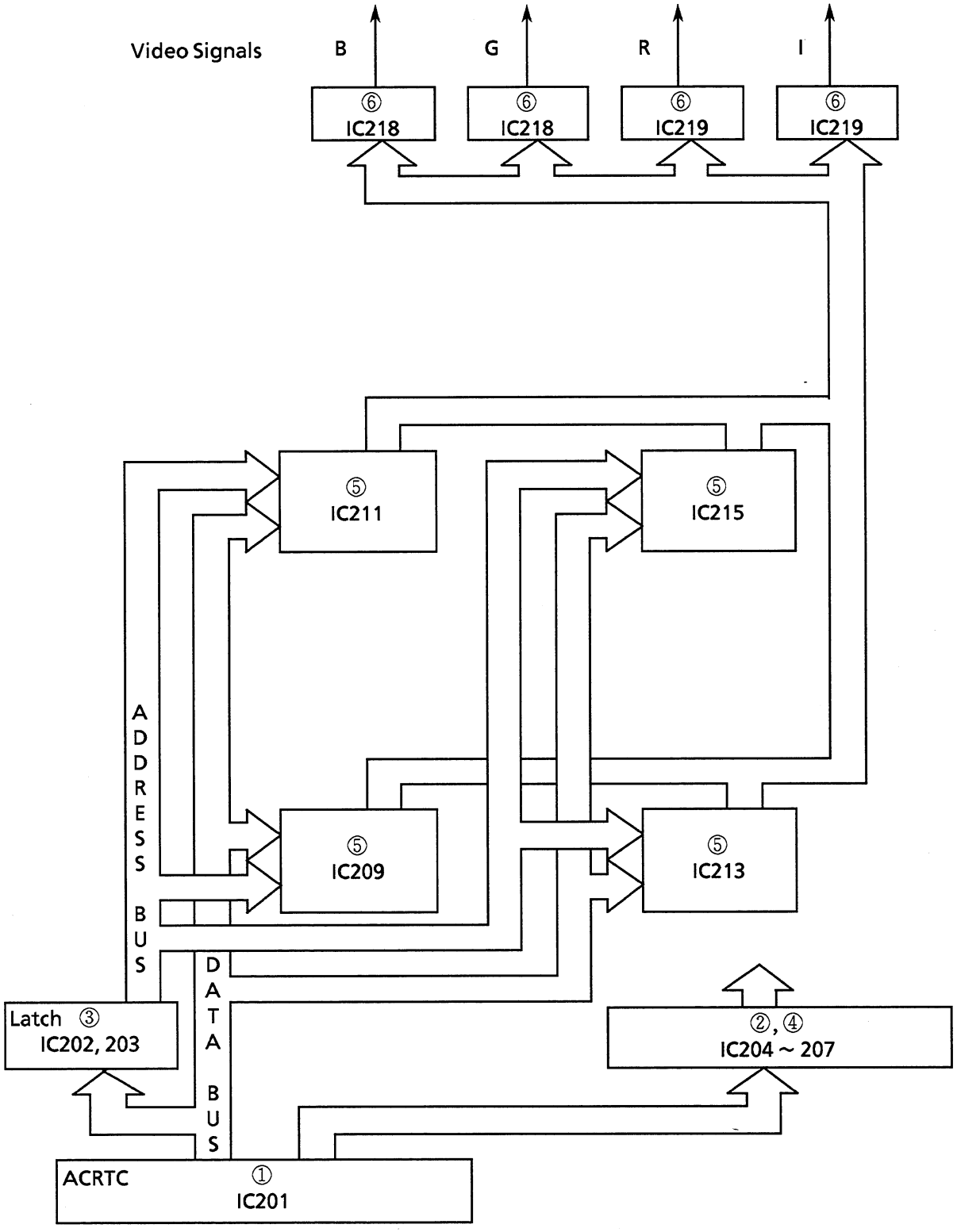
◆ Graphic Display Circuit

This circuit is controlled by the HD63484 ACRTC (Advanced CRT Controller). This controller generates the various timings needed by the CRT unit. It also allows the CPU to access the bitmap memory. The bitmap consist of eight 1M bit multi-port video RAM.

The display screen is made up of 1024 dots on the horizontal plane and 800 lines on the vertical plane.

The bitmap memory consist of 4 planes, that is, I, R, G, and B. This provides a possibility of 16 colors.

• Graphic Display Block Description



1) ACRTC (IC201)
This circuit is control by the CPU. It generates the timing signals for the CRT. It also sends the graphic images to the frame buffer.

2) Multi-port video DRAM Control Circuit (IC204 ~ 207)
This circuit controls the interface between the ACRTC and the multi-port video DRAM, by providing the timing signals, XCAS and XRAS, and the multi-port DRAM read and write signal.

3) Address Latch and Multiplexer (IC202 and 203)
This unit modifies the address or data signals from the ACRTC for the multi-port video DRAM.

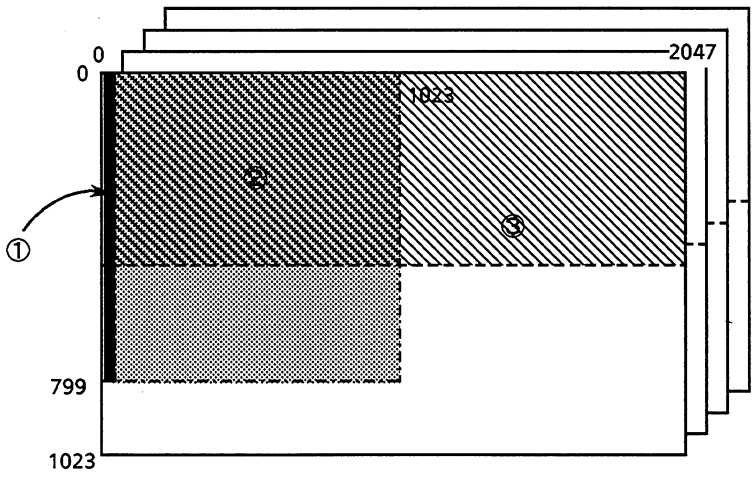
4) SAM Port Control IC218
This IC218 controls the data input and output of the multi-port video DRAMs.

5) Graphic RAM
There are eight 2M bit multi-port video DRAM (IC209, 211, 213, 215). The 4 planes on these multi-port video DRAMs make it possible to display up to 16 colors.

6) Shift Register
The 4 bit shift register latches the parallel data from the SAM port of the multi-port DRAM and converts them into serial data.

• Graphic RAM Memory Area

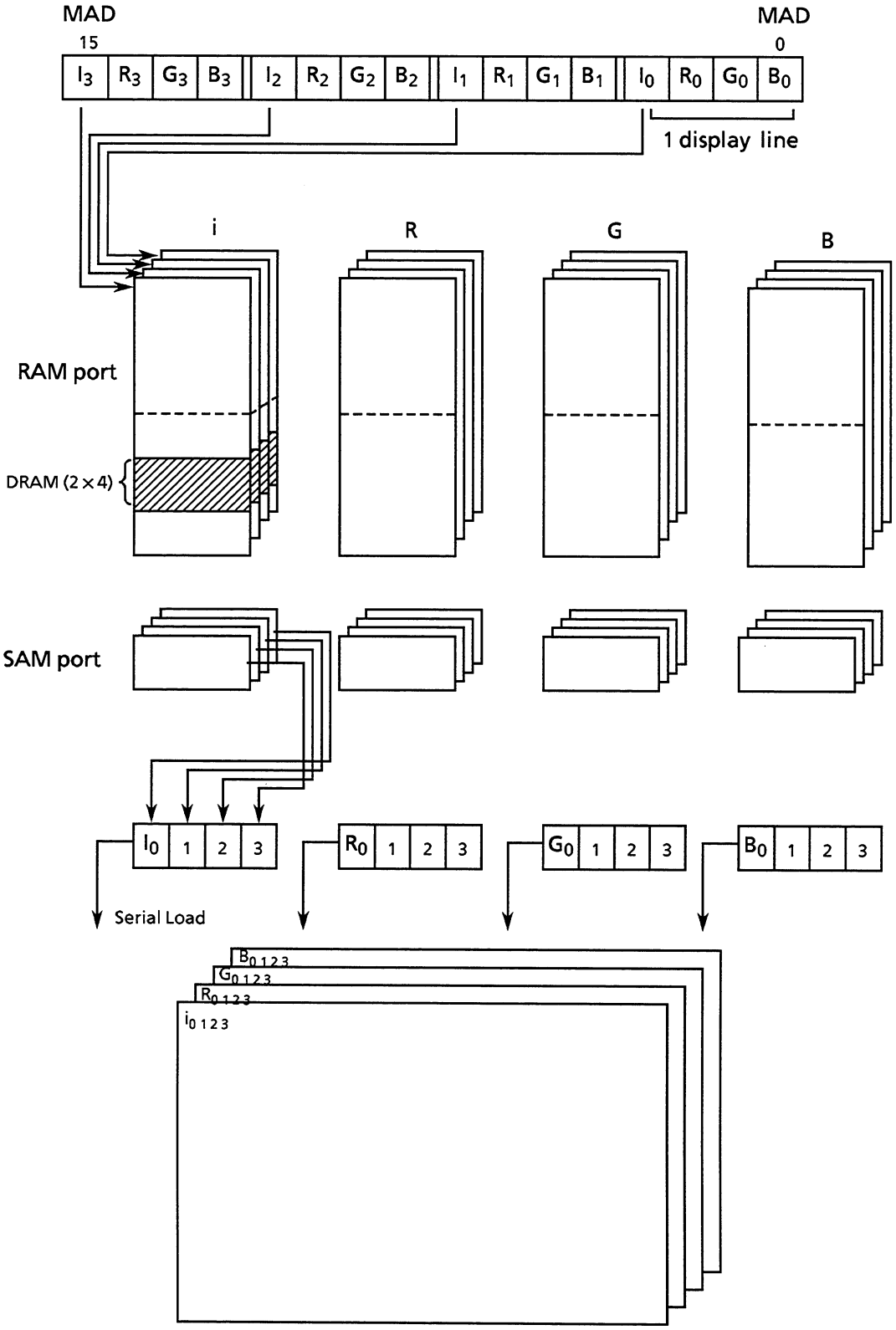
The graphic RAM is based on a multi-port DRAM, where in 1 memory cycle it can read out 2048 data. This is more than it actually needed: the actual memory area of the graphic RAM that is used is shown below.



① Memory area for ACRTC setting information
② Actual memory area used
③ The graphic RAM memory area.

• Color Processing

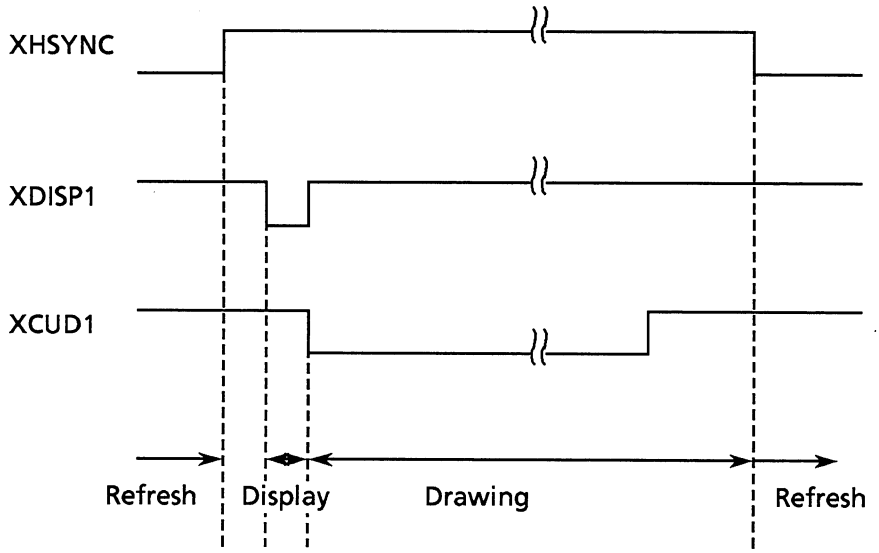
The graphic RAM reads the 16 bit data from the ACRTC. However, the main circuit consists of 4 bit per scanning line. The illustration below shows the composition of a one word data.



• Drawing and Displaying

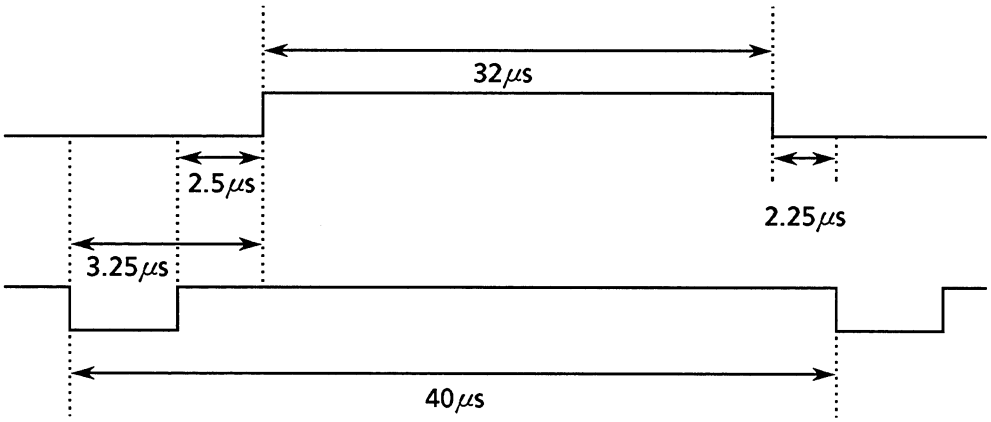
The timings used for drawing on the memory area and reading the drawn data for display are controlled by software settings. In one memory cycle, graphic data are written into the memory and the drawn data in the memory are read out simultaneously. The IC204 and 205 supply the control signals, XRAS, XCAS, XOE, and XWE.

• Drawing and Displaying Timing Chart

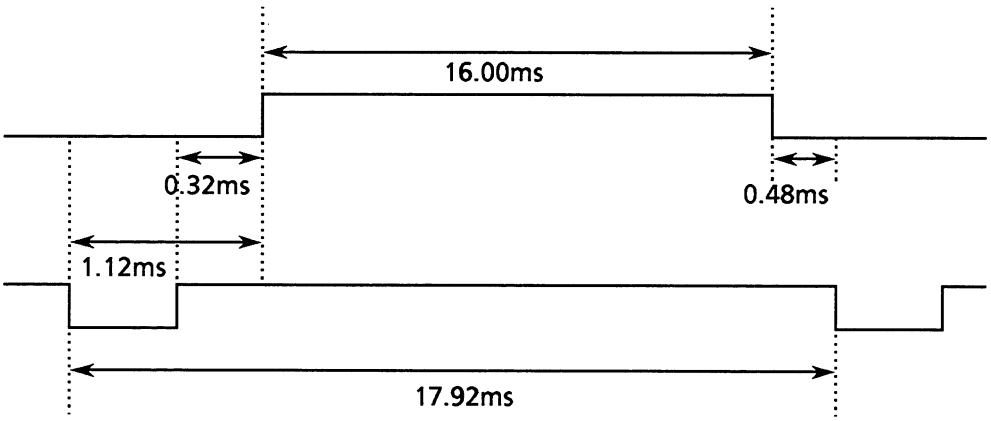


• Graphic Display Timing

* Horizontal Synchronizing Period

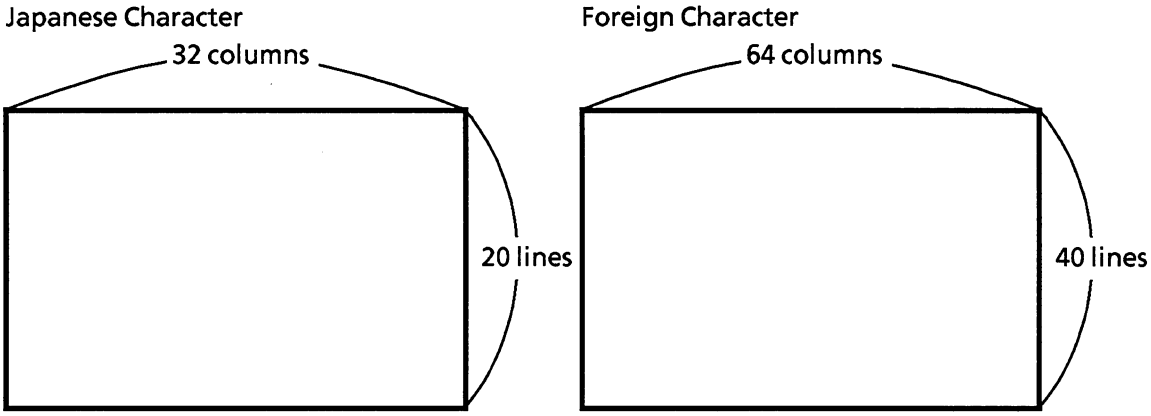


* Vertical Synchronizing Period



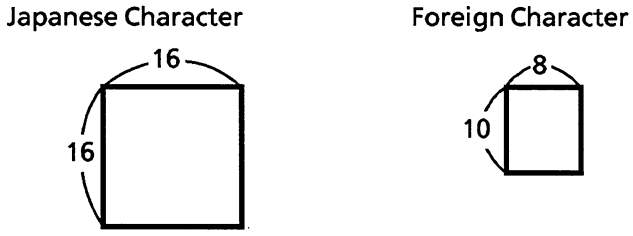
◆ Character Display Circuit

To understand the design of this circuit, a brief description of the construction of the character in the screen display is required. The character display screen for both the foreign character ROM and Japanese character ROM are shown below.



• 1 Character (Dot) Data

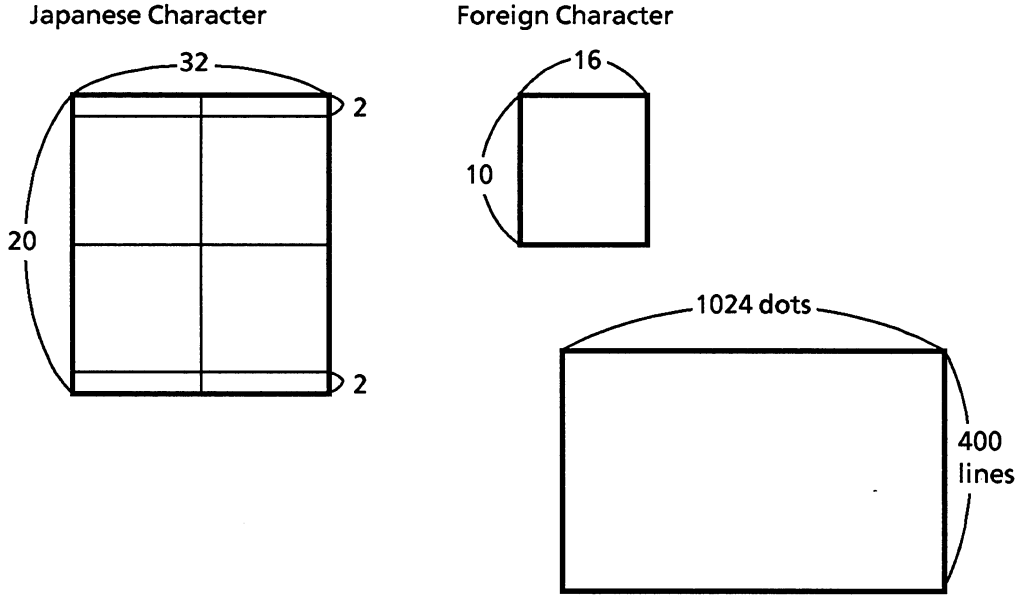
1 character (dot) data occupies 1 column and 1 line unit space on the screen.
The character (dot) data of the Japanese character (16 × 16 dots) and the foreign character (8 × 10 dots) are different. The illustration below shows the configuration of the two types of character.



In the interlace scanning method used in this system, the character data is scanned twice on the screen. This causes the character to double in sized along the vertical plane. To cancel out this elongation effect along the vertical plane, the character data is double read along the horizontal plane. This means the 1 character (dot) data doubles the number of its horizontal dots but the number of its vertical dots stay the same.

Next,the displayed Japanese character (dot) data is modified to fit 4 displayed foreign character (dot) data. Hence 1 displayed Japanese character (dot) data contains 32 × 20 dots, and consequently the display screen now contains 1024 × 400 dots. The smallest unit of character (dot) data consist of 8 × 10 dots.

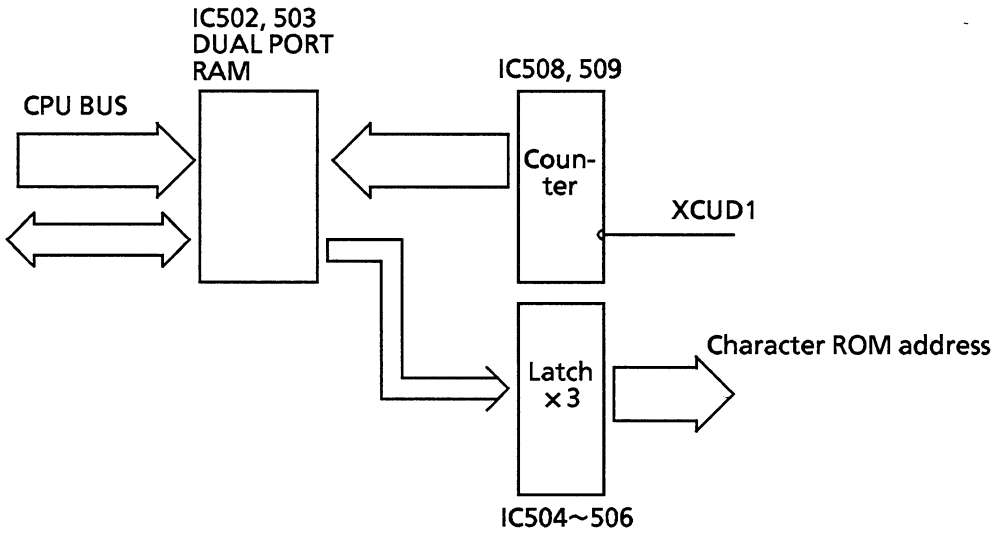
Displayed Japanese Character (Dot) Modification



The 8 × 10 dots character (dot) data is related to one code data in the character ROM. One code data contains 24 bits (3 Bytes) of information – 2 × 8 bits of character code for the character ROM and 8 bits of attribute data of the character code.

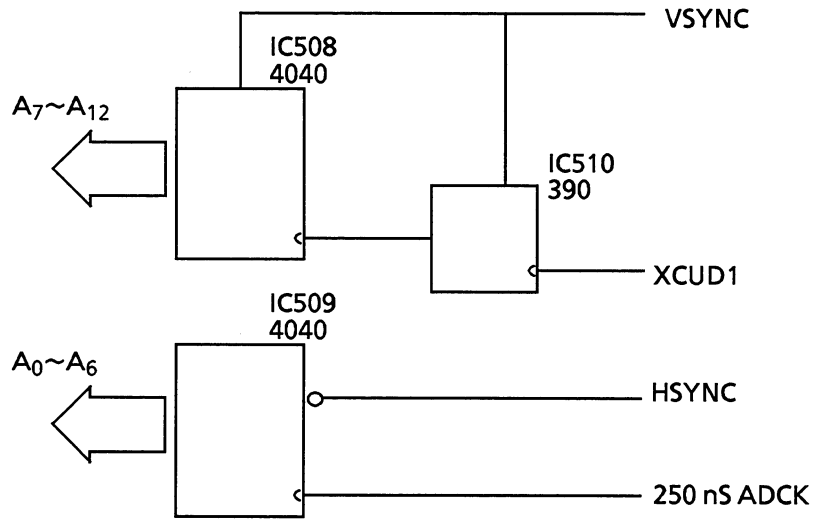
The horizontal 16 bits are read out together, hence 1 cycle takes about 500 nsec. In the cycle, the data are double read – one for the character code and one for the attribute code.

• Character ROM



The counters IC508 and 509 generate an address for display on the display unit.
The address specifies a character code on the Character ROM. The character code and its attribute code are outputted to the character ROM IC511.

• **Character Code Address Generator**

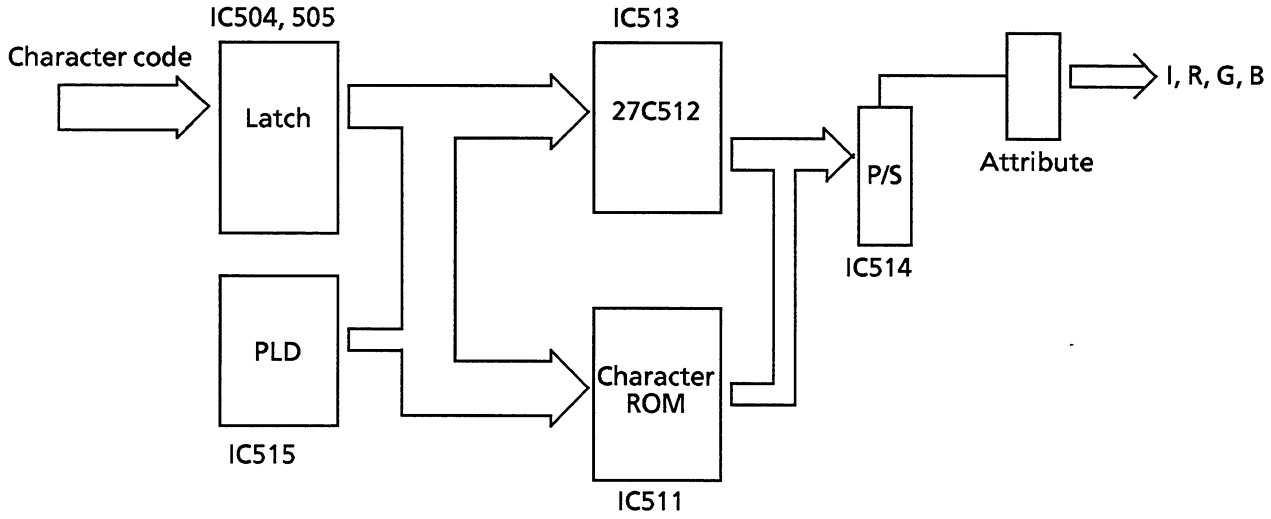


The character code addresses A0 ~ A6 are read out every 250 nsec. For every 128 times the data are read out, the XHSYNC signal reset the circuit.

The character code addresses A7 ~ A12 are read out according to display timing 1 (XCUD1). For every ten times the data are read out, the VHSYNC signal reset the circuit.

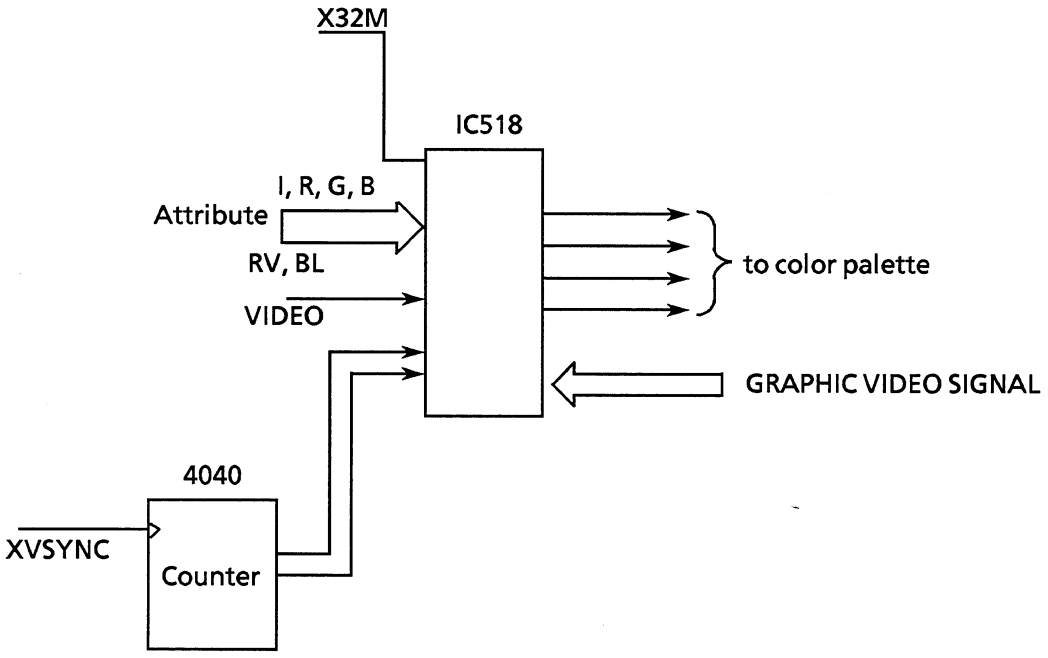
• Character ROM

The character ROM reads out the character video signals according to the address given by the character code address. The character video signals are converted into 8 bit serial data before being sent to the character attribute circuit.



• Character Attribute

The IC518 converts the video signals (character and graphic) according to their attribute signals. The converted video signals now not only consist of the information for the video image, but also, its color.



◆ Waveform Display Circuit

The functions of this waveform display circuit:

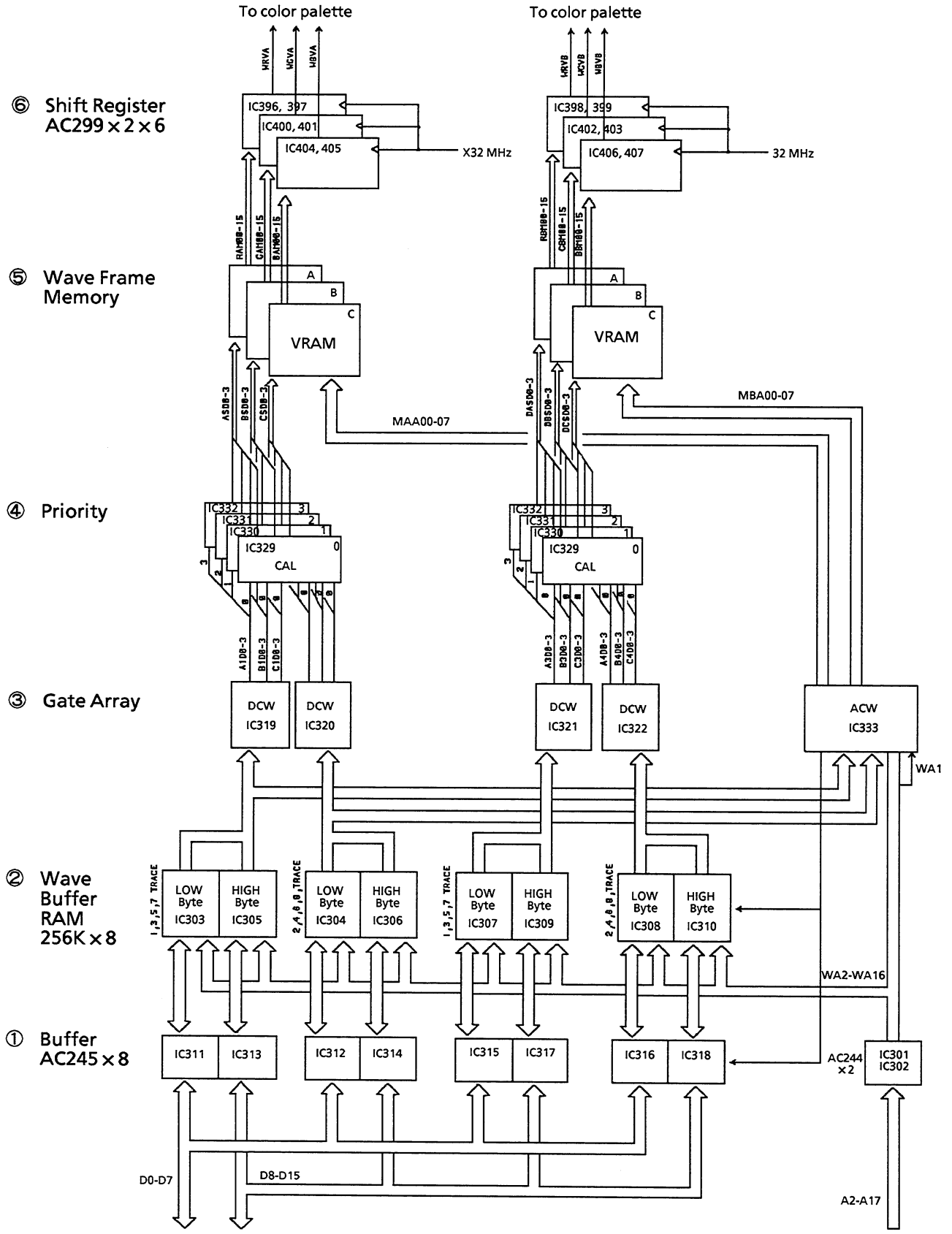
1) To display up to 8 colored waveform traces.
2) To make the waveform trace sweep across the screen.
3) To freeze the waveform trace on the screen.
4) To switch on/off the waveform trace/s on the screen.
5) To allow changeable assignment of colors to the waveform traces.

2K Word (16 bits) of waveform information is required to draw one waveform trace. This 2K Word waveform information is read out from the CPU. The frame gate array in this display unit gates the one frame waveform data into 3 bitmap memory according to the timing provided by the ACRTC.

The 2048 dots × 800 lines screen is divided into the even field and the odd field for waveform display.

The slave video controller (ACW) only controls the processing on the waveform display circuit under the direction of the master video controller (ACRTC).

• Waveform Display Block Diagram



The waveform display circuit consists of the following units:

1) Buffer
This is a two way communication buffer. However, when the data in the WAVE RAM is read out to the gate array, the buffer inhibit the bus line to and from the CPU.

2) WAVE RAM (Waveform Buffer RAM)
The 8 WAVE RAMs are grouped in blocks of two. Two blocks of WAVE RAMs are grouped for the waveform traces 1, 3, 5, and 7. The remaining two blocks of WAVE RAMs are grouped for waveform traces 2, 4, 6, and 8. In this design, the resulting video signals from these two grouped blocks are superimposed on each other with a half clock timing difference. The horizontal resolution is doubled by this half clock timing difference during superimposing.

3) ACW and DCW
The ACW (slave video controller) has two functions:
* Controls the bitmap memory with the timing received from the ACRTC of the graphic display unit.
* Controls the communication bus lines for the CPU and the gate array DCW.

The gate Array DCW
One gate array DCW served 4 waveform traces data.

4) Priority Level Circuit
When two or more waveforms are superimposed on one another there is a tendency for the colors of the waveforms to mix and form another color. This circuit prevents this effect from happening by adding a priority level code onto the waveform data.

5) Bitmap Memory
These are two 3 plane bitmap memory. The priority level coded serial waveform data are inputted into the bitmap memory dual port RAM through the SAM ports. The bitmap memory dual port RAM reads out the parallel data according to the control signals from the ACW.

6) Shift Register
The waveform display resolution is twice of that the character or graphic display resolution, however, the illuminating time is halved. On the screen, the character or graphic display appears brighter than the waveform display. To counter this effect, the brightness signal to the waveform display unit is doubled.

◆ WAVE RAM (Waveform Buffer RAM)

The function of the WAVE RAM (IC303 ~ 310) is to improve the horizontal resolution of the 6 to 8 waveform traces display.

The waveform data read out from the WAVE RAM served two function:
a) used as a command signal by ACW.
b) used as a data signal by gate array DCW.

The IC301 and 302 controls the waveform RAM address bus lines WA1 ~ WA16 according to the command of the CPU. However, when the gate array access them, the IC301 and 302 are inhibited by the

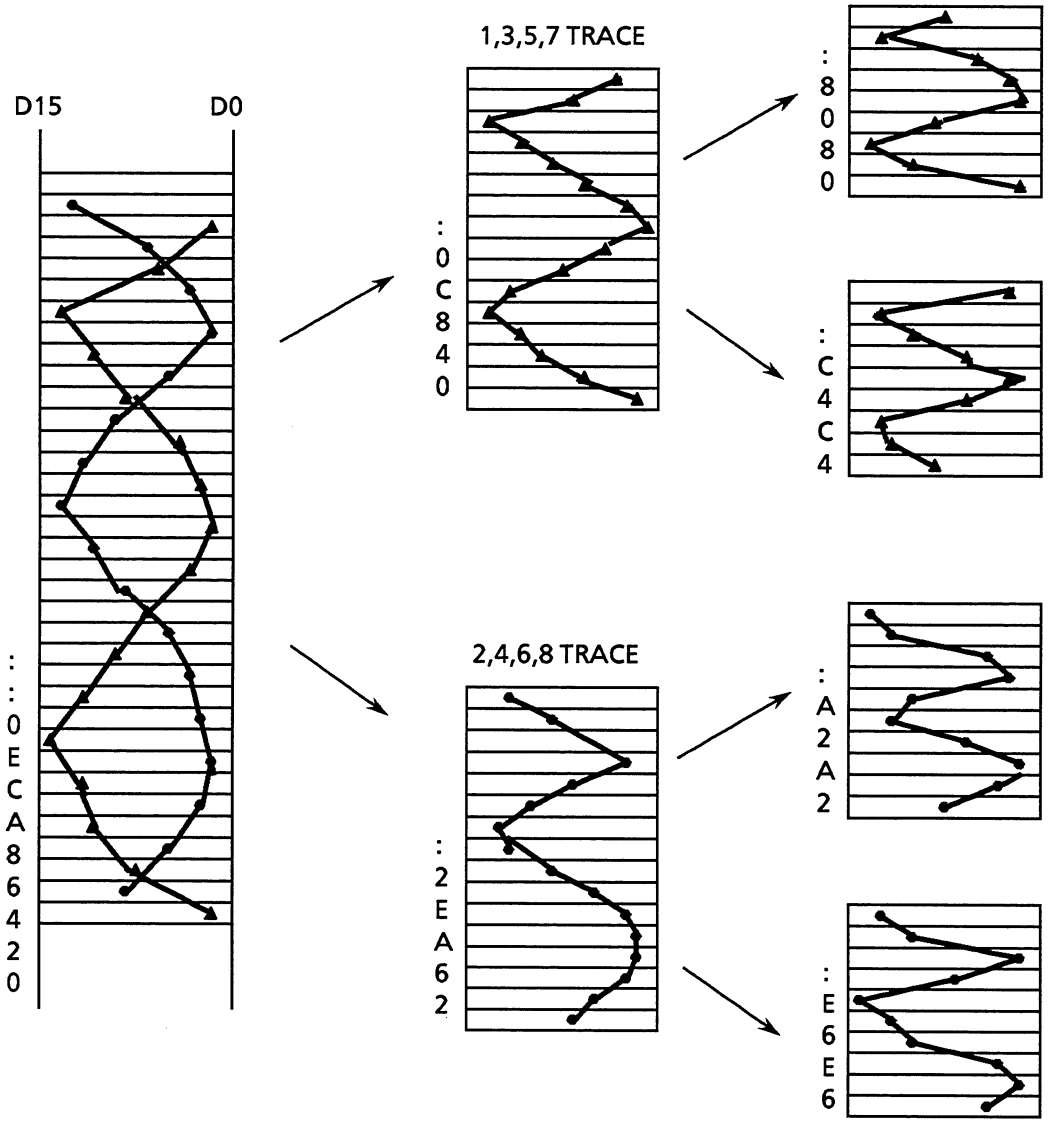
The IC301 and 302 controls the waveform RAM address bus lines WA1 ~ WA16 between the internal bus and the CPU bus according to the command given by the CPU. However, when the ACW access the waveform RAM address lines, the communication bus lines between the internal bus and the CPU bus are inhibited. The BCONT (bus control) signal from the ACW inhibit the above communication. When both the CPU and ACW access the waveform RAM address bus lines together, the ACW delays its waveform data acknowledge signal (XGDTACK) to the CPU. This causes the CPU to hold the address and allow the ACW to finish accessing the waveform RAM bus address lines.

The CPU address line A2 directs the ACW to separate the 4 blocks of two WAVE RAM into two groups of two blocks each. The IC337 and 338 further separates the two blocks of WAVE RAM according to the CPU address line A1 and A2.

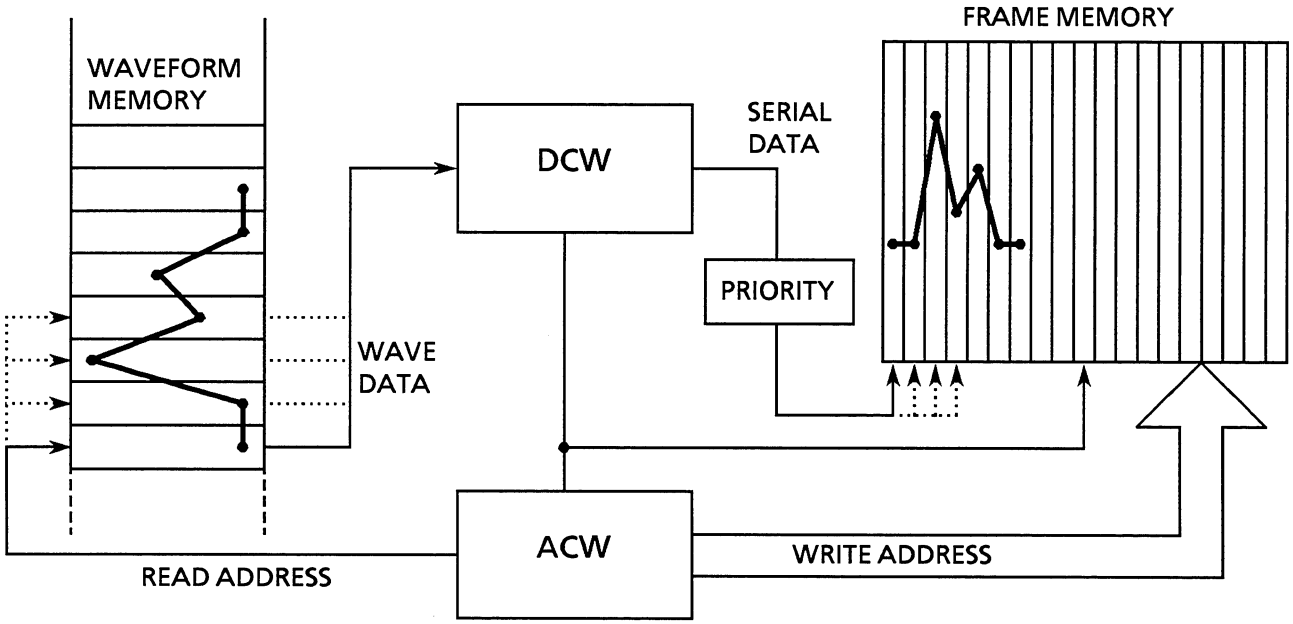
The table below shows the composition of the waveform RAM bitmap memory.

A2, A1	D15	D0	
0, 0	IC303	IC305	1, 3, 5, 7 trace
0,1	IC304	IC306	2, 4, 6, 8 trace
1, 0	IC307	IC309	1, 3, 5, 7 trace
1, 1	IC308	IC310	2, 4, 6, 8 trace
0, 0	IC303	IC305	.
0, 1	IC304	IC306	.
	.	.	.
	.	.	.
	.	.	.
			.

The illustration below shows how the 8 waveform traces are separated.



◆ **Waveform Processing Circuit**



The function of this circuit is to draw the waveform trace on the frame memory with the interpolated waveform data it received from the DCWs (IC319 ~ 322).

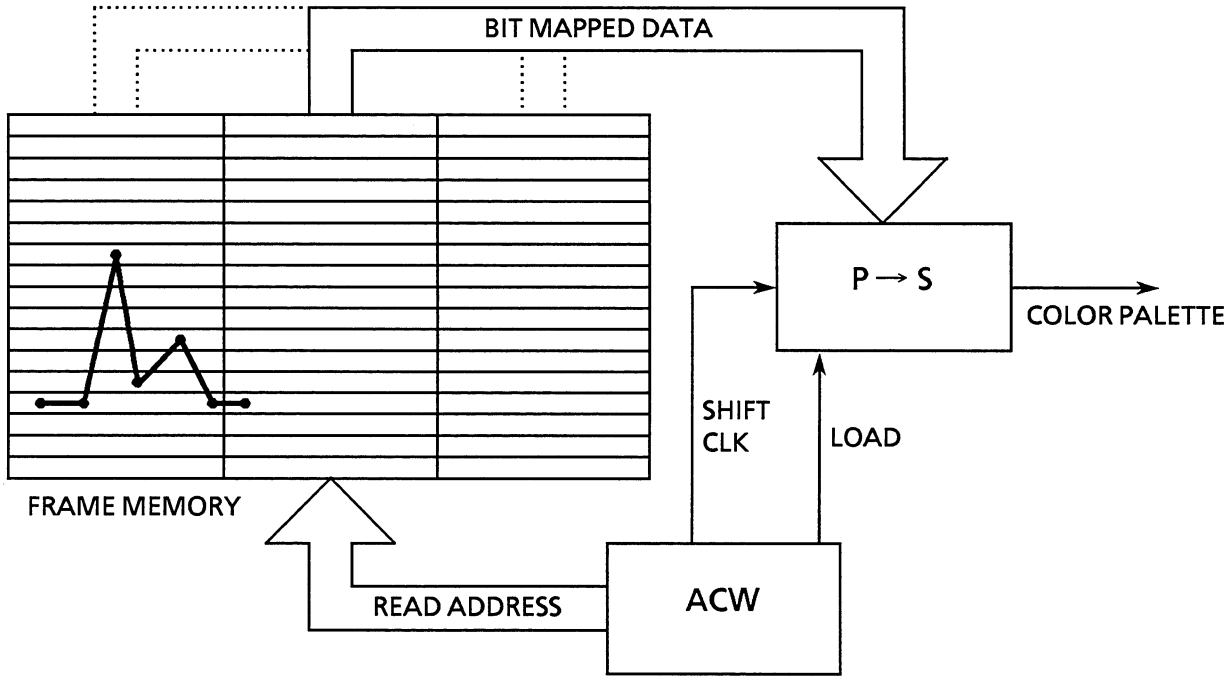
When the DSLD port of the ACW is negated, the ACW reads out the address to the buffer RAMs, IC303 ~ 306. The buffer RAMs then load out the waveform data and the DCW latch this waveform data. The latching timing LCK is provided by the ACW. Before the DSLD port of the ACW is negated again to to load the next batch of waveform data into the DCWs, the DCWs interpolates the waveform data by shifting the waveform data. The shifting timing, SCLK, is again provided by ACW. These shifted data, A1SD0 ~ 3, ...C4SD0 ~ 3, are then outputted to the priority circuit.

At a later stage the shifted data are color palette coded. Up to 7 different colors (represented by bits 0,0,1 to 1,1,1) can be coded onto the shifted data.
These color code can give each individual waveform trace a different color.
However, when these different colored waveform traces overlap each other, a color other than those of the overlapping waveform traces occurs. For example, when a green (0,0,1) waveform trace overlaps a red (0,1,0) waveform trace, the overlapping point will have a different color code (0,1,1). To prevent this from occurring, the priority code is first added to the shifted data.

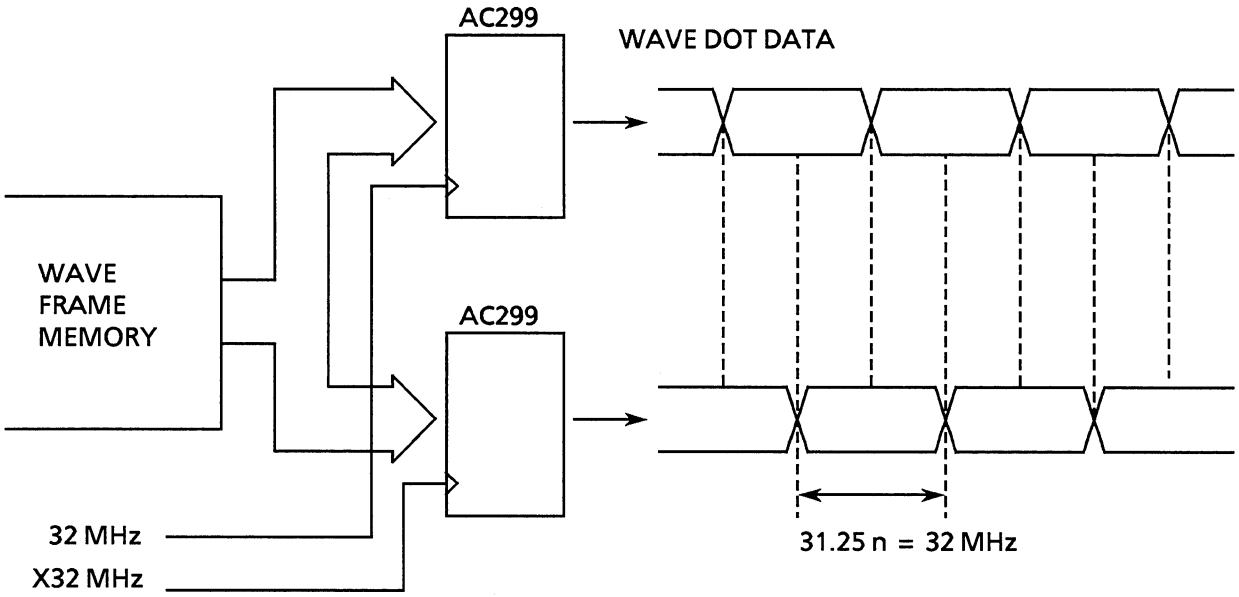
The priority level coded serial data such as ASD0 ~ 3 (shifted data) are strobe into the frame memory (IC348 ~ 395) via their serial I/O ports by the Serial Access Strobe (SAS 0,1). The ACW frame memory access timing is synchronized by the ACW 2MHz output clock. The ACW changes the access address to the WAVE RAM and frame memory with every XSLD timing signal. This process is continuously repeated.

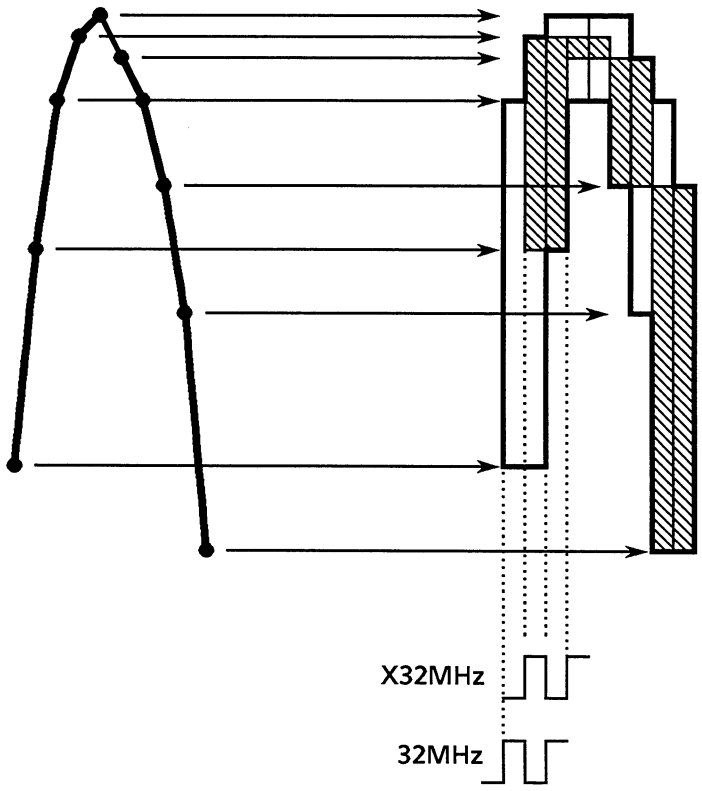
The XHSYNC signal clears the address counter in the ACW. The ACW displays the waveform trace on the CRT when it received the display command signal (XDSP1) from the ACRTC.

◆ **Waveform Display circuit**



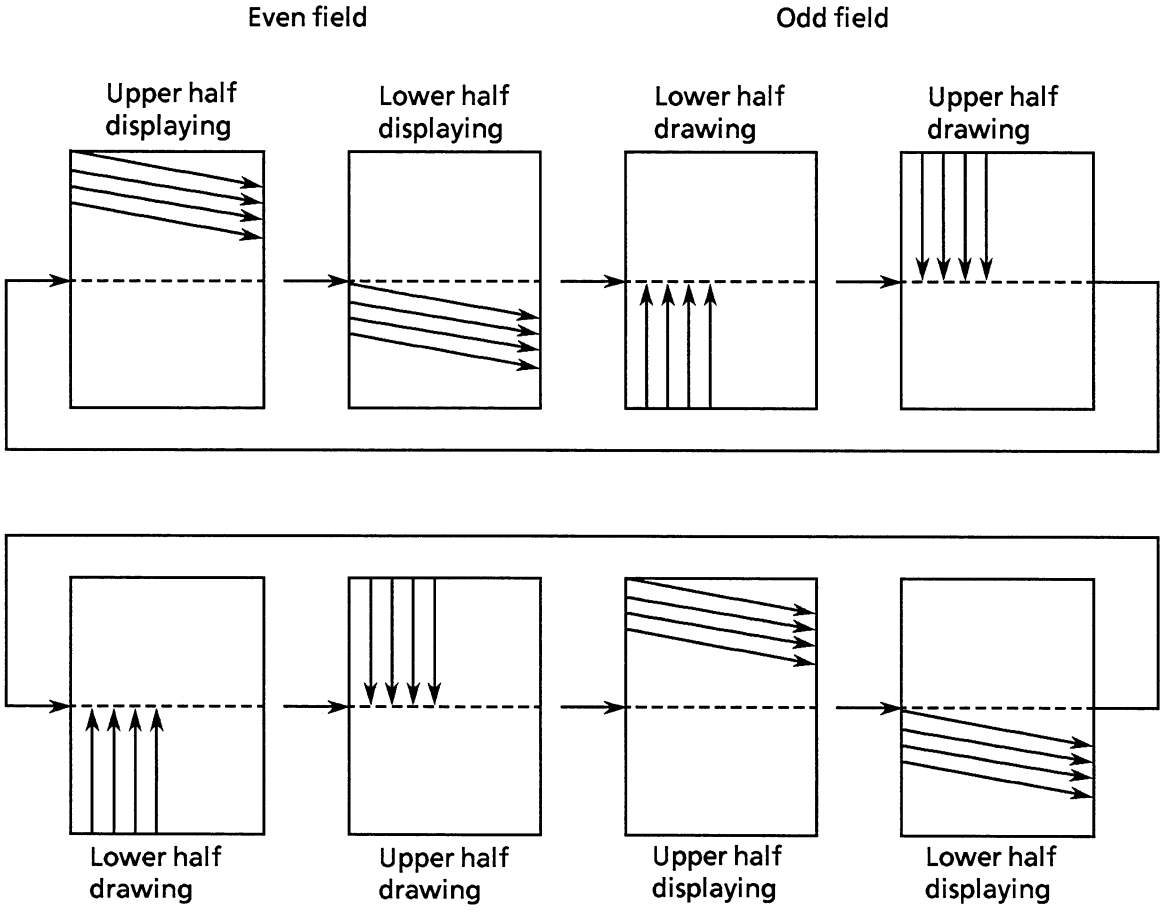
The IC396 ~ 407 latch the 16 bit parallel data from the frame memory and convert them into serial video data. The serial video data is loaded out under two timings: The 32MHz clock and X32MHz clock. The difference between the two clocks is 0.5 clock. This is to provide the display waveform trace with a high display resolution.

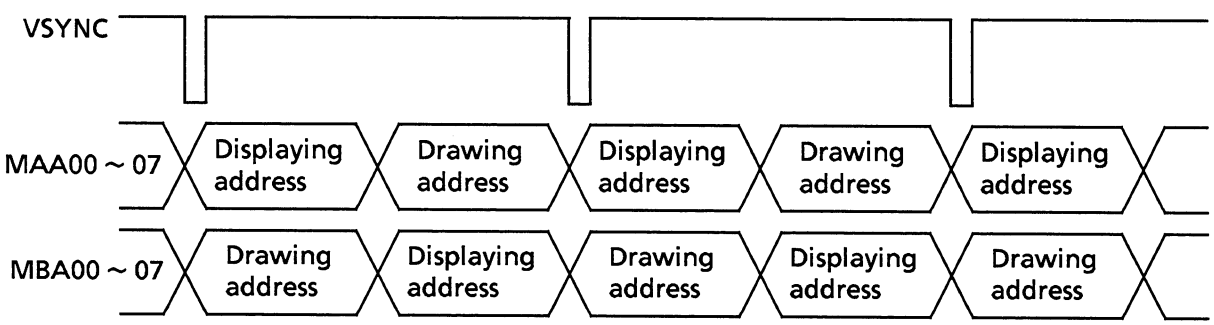




Waveform is not fixed graphic since it changes continuously. To display this continuously changing waveform, the frame memory has to simultaneously draw and display the waveform. To solve this problem, the frame memory is separated into an upper part and a lower part. The upper part of the frame memory draws the waveform and the lower part displays the waveform in the first half of its timing cycle. In the second half of the timing cycle, the upper part displays the waveform that the frame memory had drawn during the first half of the timing cycle, and the lower part draws the next waveform to replace the displayed waveform in first half of the timing cycle.

The illustration below shows the switching of the upper address (MAA00 ~ 07) and the lower address (MBA00 ~ 07).

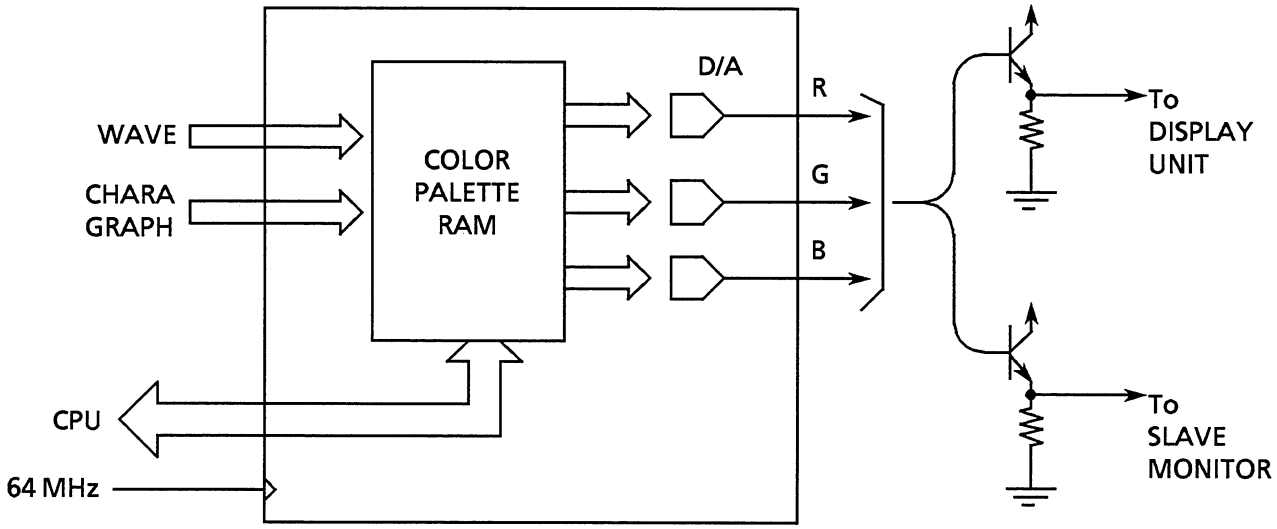




◆ Color Palette Circuit

This color palette circuit adds the color palette code to the waveform, graphic, and character video signal. The D/A convertor converts the digital video RGB signals into analog RGB signals and outputs them to the CRT unit.

This circuit can simultaneously display up to 7 colors for waveform display and up to 15 different colors for character and graphic display.



Color palette IC701

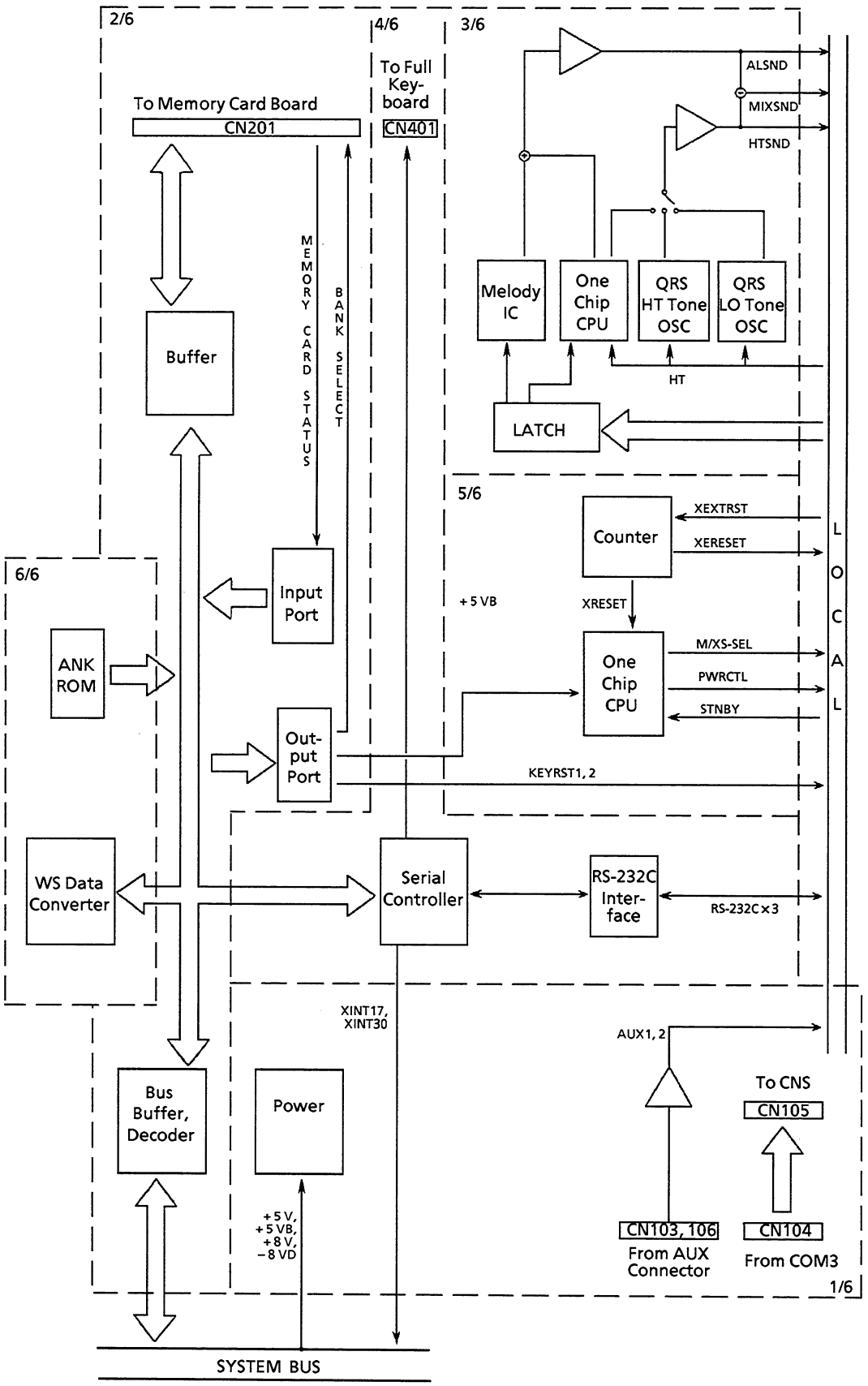
3-2-4 I/O Board, UP-0797

◆ General

The I/O board is the main interface unit with the external units, such as, the display unit and the keypad.

The functions of this board is:
* to interface with the display unit.
* to interface with the keypad.
* to read or write the memory card.
* to control the power supply.
* to generates the alarm sound and the QRS sound signals from the sound signal received from the CPU board.
* to serve as the input and output ports for the central monitors and the signal exchanger.
* to receive and amplify the waveform signals from the auxiliary (external) unit.
* to enable the screen display to be hardcopied by the recorder

Block Diagram



The I/O board consists of the following circuits:

• Bus Buffer and Decoder Circuit
This circuit consists of the system bus and the decoder for the bus control signals from the CPU.

• Memory Card Interface Circuit
This circuit reads/writes the data onto the selected bank in the memory card.

• Serial Communication Circuit
IC404 and 408 control the serial communication with keypad, display unit, and the full-key board.

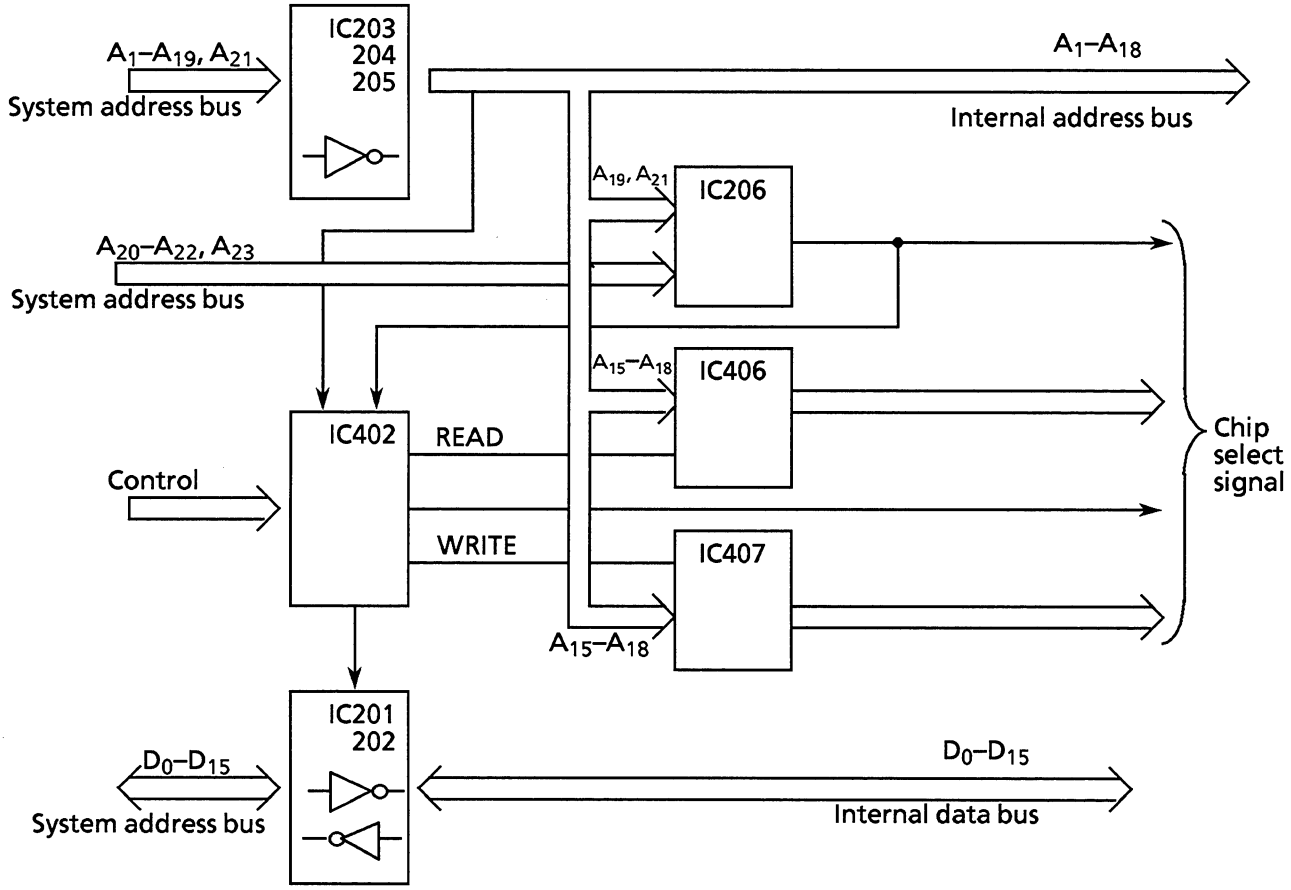
• Power Supply Control Circuit
This circuit controls the power supply according to the instruction set by the CPU on the CPU board, or the keypad.

• Sound Generator circuit
This circuit generates the alarm sound and the QRS sound.

• Auxiliary Amplification Circuit
This circuit amplifies the signals from the front panel auxiliary unit input connector (AUX) , and the rear panel auxiliary unit input connector.

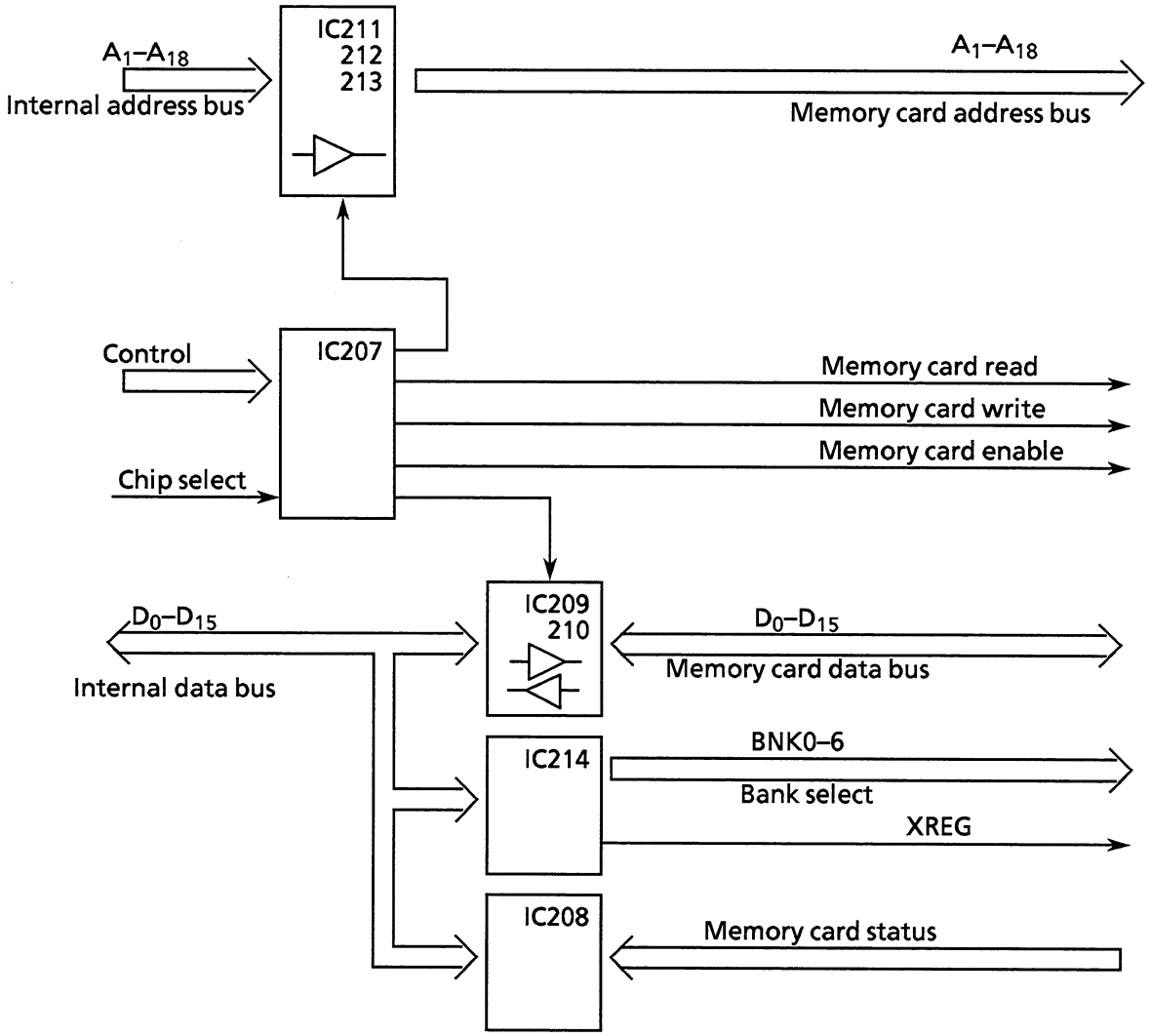
• Hardcopying Processing Circuit
This circuit converts the screen data into recording data for the recorder.

◆ **Bus Buffer and Decoder Circuit**



The buffers IC203 ~ 205 receive the address information from the system address bus and drive it to the internal bus. The bidirectional buffers IC201 ~ 202 receive and transmit the data from/to system data bus to/from internal data bus. IC402 receive the control signals (READ, WRITE, and DTACKB) from the CPU on the CPU board and in turn direct the bidirectional bus to transmit or the receive.
It also directs the decoders/multiplexers IC406 ~ 407 to access the bus.
The decoders/multiplexers decode the address data and outputs the chip selection signals to ROM IC509 ~510.

◆ **Memory Card Interface Circuit**



The buffers IC211 ~ 213 receive the address information from the internal address bus and drive it to the memory card address bus. The buffers' latching timing is provided by IC207. IC207 also provides the latching timings and control signals (READ, WRITE, MEMORY CARD ENABLE, and DTACKB for the bidirectional bus transceivers IC209 ~ 210 to receive/transmit data to/from the internal data bus from/to the memory card data bus.

IC208 reads and interprets the status of the memory card. The table shows the signals received from the memory card board and their interpretation messages appearing on the display.

XCD1, XCD2 either or both are "HIGH" ——— MEMORY CARD NOT INSERTED

BVD1, BVD2 either or both are "LOW" ——— LOW BATTERY

WP is "HIGH" ——————————— WRITE PROTECT ERROR

IC214 selects the memory banks BNK0 ~ 6 in the memory card as directed by the control signal XMCPORTW from the IC407.

The memory card has two kinds of memory, namely, common memory and attribute memory. The selection of one these memories depends on the status of signal XREG.

XREG	Memory Selection
High	Common memory
Low	Attribute memory

◆ Serial Communication Circuit

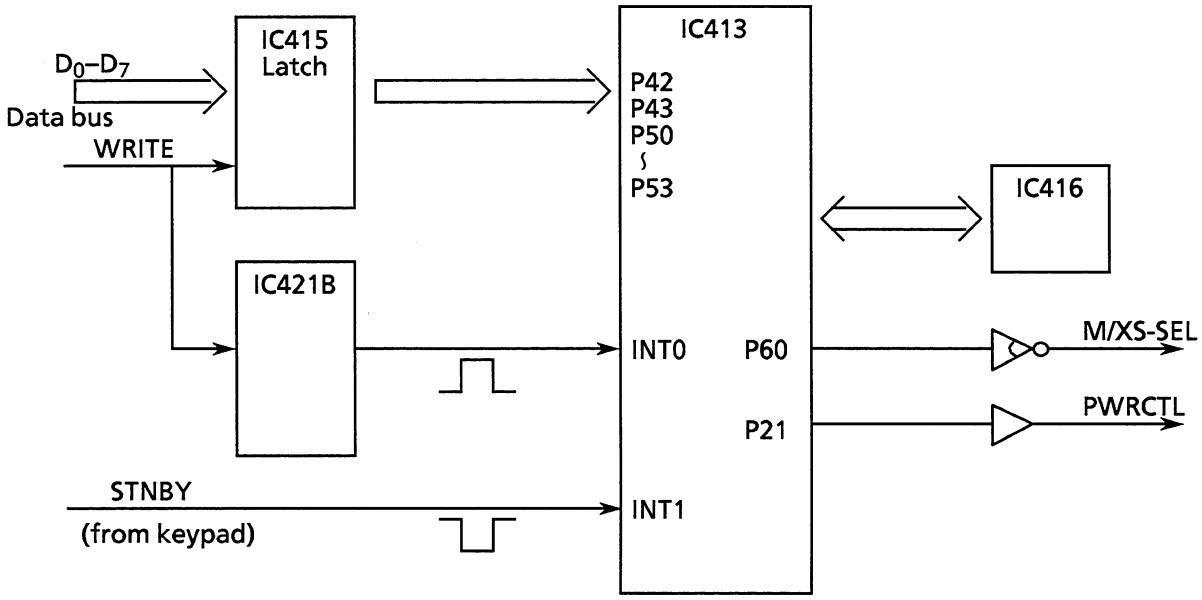
IC404 and 408 control the serial communication circuit. Each port in the two ICs communicates with different unit. The table below shows the port and the unit the port is communicating with.

IC404	Port A Port B	Full-key board Display unit
IC408	Port A Port B	Keypad when connected to the display unit Keypad when connected to the main unit

Communication with the display unit and keypad is by the RS-232C communication.

◆ Power Supply Control Circuit

• Function



This circuit controls the power supply of the bedside monitor main unit when POWER ON/OFF key on the keypad is pressed. The POWER ON/OFF key on the keypad switches the power supply unit either to its standby mode, or its operating mode. In the standby mode, the power supply unit only supplies the +5VB. Almost all the operating functions on the main unit shut down. The I/O board and the keypad are operational as they run on the +5 VB power supply.

IC413 controls this circuit. The status of the PWRCTL terminal of the IC413 sets the power supply unit to its operating mode or standby mode. The table below shows the status of the PWRCTL terminal and its power supply unit setting.

PWRCTL	Power supply
High	Standby
Low/Open	Fully operational

• Keypad Power ON/OFF

Prerequisite condition: The bedside monitor main unit is operating and waveforms are displayed on the display unit.

1) To set the bedside monitor main unit on standby, press the POWER ON/OFF key:
   i) The keypad senses that the Power ON/OFF key is pressed.
   ii) The keypad sends out the command signal to CPU board's CPU.
   iii) The CPU board's CPU receives the command signal and immediately sets the display unit's power supply off.
   iv) The CPU board's CPU then sends the command signal to IC413. This signal sets the monitor main unit power supply unit to its standby mode.
   v) IC413 of the I/O board receives the command signal via ports P42 and P43. This immediately sets IC413 PWRCTL terminal (P21) to HIGH.
   vi) The bedside monitor's power supply unit enters its standby mode.

2) To set the bedside monitor main unit back to its full operational mode, press the POWER ON/OFF key again:
   i) The keypad senses that the Power ON/OFF key is pressed.
   ii) The keypad sends out the command signal to IC413 of the I/O board.
   iii) IC413 of the I/O board receives the command signal via its INT1 terminal, and this consequently sets its PWRCTL terminal LOW/OPEN.
   iv) The bedside monitor main unit's power supply unit returns to full operational mode.
   v) The CPU of the CPU board undergoes reset procedure, and finally switches the display unit's power supply unit on.

• Bedside Monitor Main Unit Master/Slave Mode Function

The bedside monitor main unit, when connected to the display unit, can operate in either the master mode (display unit in the slave mode), or the slave mode (display unit in the master mode). The IC413 sets the operating mode of the bedside monitor main unit by reading the data in its ports P50 ~ P53. The IC413 then asserts or negates the selection signal M/XS-SEL. In normal operation, the bedside monitor main unit operates in the slave mode.

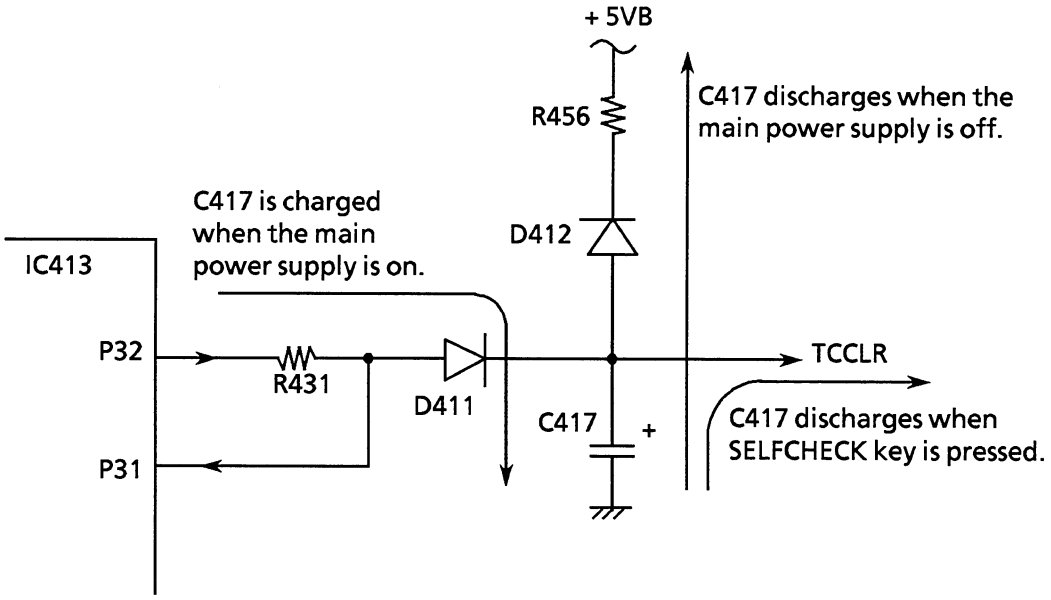
• Power Down Protection Control

This is to prevent IC413 from reading any data inputted into its INT0 terminal when when the + 5V supply is LOW.

• Reset

During normal operation, when the main power switch is accidentally switched off, or a sudden temporary loss of power occurrs, the operating settings of the bedside monitor may be lost. These operating settings are the power supply status (standby mode or full operational mode) and the operating status of the main unit (master mode or slave mode). Therefore, when the main power supply is reconnected, the bedside monitor is

reset.The bedside monitor may now operate on the operating settings different from those before the power failure.
To prevent this from affecting the bedside monitor, the IC416 reads the operating settings of IC413 and stores them in its memory. When the power supply is reconnected, the IC413 now reads the memory of IC416 for the operating settings. This is only effective as long as the temporary + 5VB power supply from capacitor C417 is available.



P31 = H ····· Instantaneous → operating settings maintained
P31 = L ····· Main power supply ON → Power supply ON

• Main Power Supply On

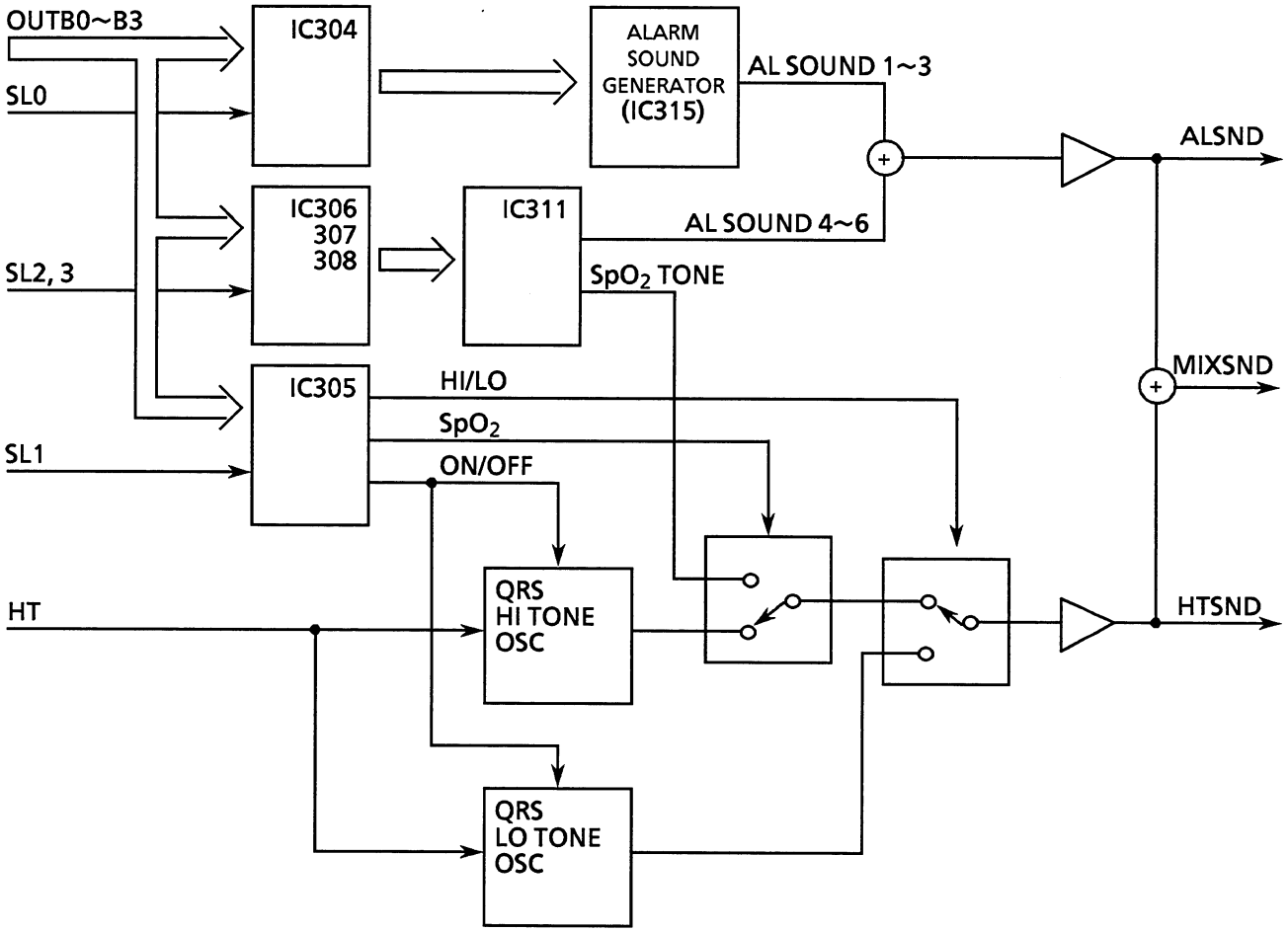
To differentiate the reset operation after a temporary power failure from that of initially switching the main power supply on, IC413's port P31 status is read. When this port is HIGH, the memory in IC416 is read during resetting procedures. However, when the port is LOW, the memory in IC416 is disregarded during resetting procedures.

In the SELFCHECK mode, both the IC413 and capacitor are cleared and reset.

NOTE

The resupply of power back to the bedside monitor is different from that of the function of the POWER ON/OFF key of the keypad.

◆ **Sound Generator Circuit**



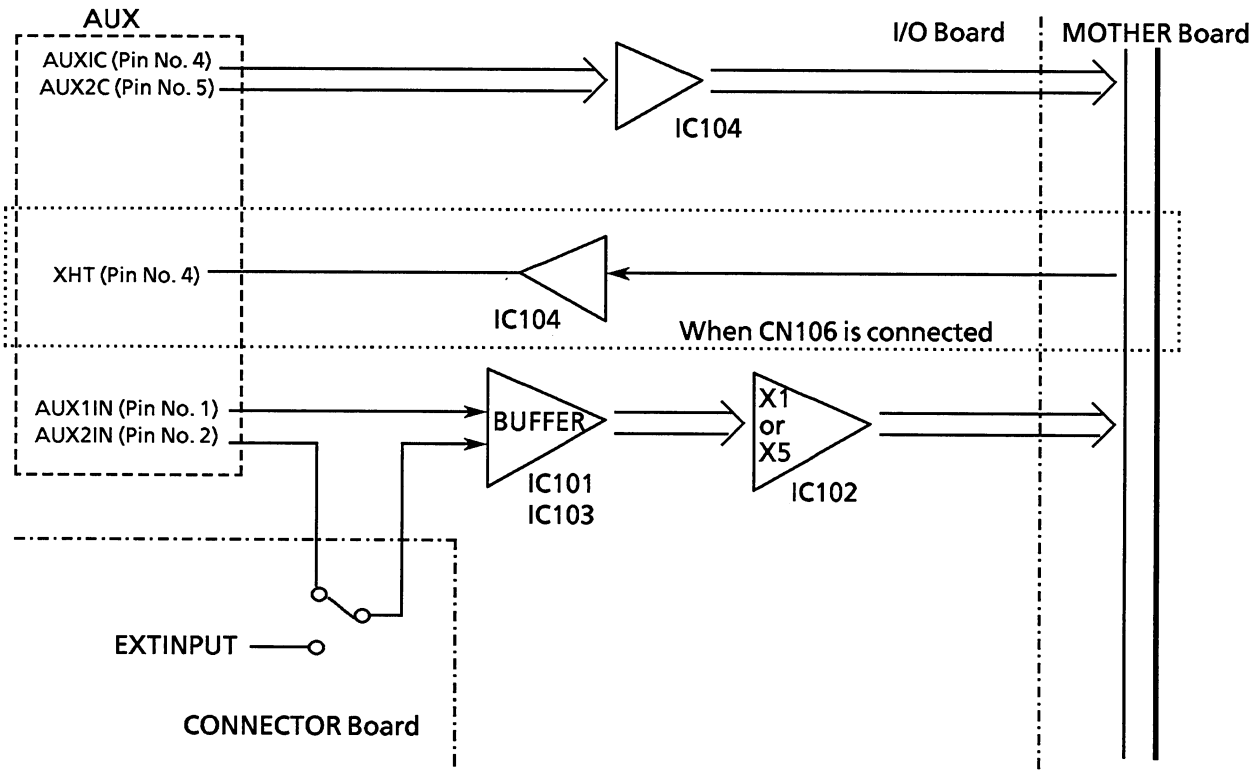
The key controller IC176 of the CPU board supplies the control signals (OUTB0 ~ 3 and SL0 ~ 3) to this sound generator circuit. The table below shows the output port of the key controller IC176 of the CPU board.

Sound Generator Output Signal

SL	OUT	Description	
SL0	B0	Continuous alarm	1: ON 0: OFF
	B1 B2	Alarm Sound 1~3	$\binom{0}{0}$: "piropiro" sound $\binom{0}{1}$: "pinpon" sound $\binom{1}{1}$: "pon" sound
	B3	Alarm sounds once	1: ON 0: OFF
SL1	B0	QRS SYNC sound pitch	1: high pitch 0: low pitch
	B1	QRS SYNC sound ON/OFF	1: ON 0: OFF
	B2	SpO_2 tone	1: normal sound 0: SpO_2 tone
	B3	Not used	
SL2	B0	IC311 reset	0: reset
	B1 B2	Alarm sound 4~5	$\binom{0}{0}$: high pitch "pipipi" sound $\binom{1}{0}$: middle pitch "pipi" sound $\binom{0}{1}$: low pitch "pipi" sound $\binom{1}{1}$: OFF
	B3	SpO_2 tone highest level bit	
SL3	B0	SpO_2 tone lowest level bit	From the 5 bits data 25 different pitches are generated.
	B1	SpO_2 tone second level bit	
	B2	SpO_2 tone third level bit	(1,1,1,1,1) highest pitch
	B3	SpO_2 tone fourth level bit	(0,0,1,1,1) lowest pitch

These control signals are latched by IC304 ~ 308 in the sound generator circuit. In this sound generator circuit, IC315 and 311 generate the alarm sound signal, ALSND. When the SpO_2 tone function is selected, the IC311 outputs the SpO_2 value to the QRS high tone generator circuit. Here, the resulting QRS high tone pitch varies with the value of the SpO_2.

◆ **Auxiliary Amplification Circuit**



The main function of this board is to amplify the external unit input signals.
The settings of jumpers J101 and 102 determine the amplifications factor (X1 or X5) of IC102.

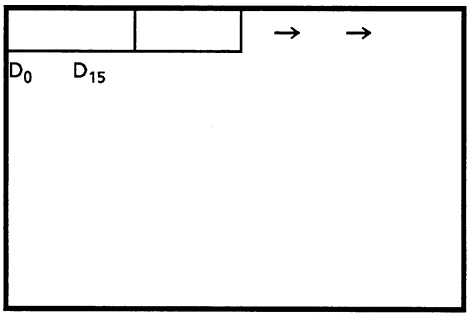
The bedside monitor can receive the external unit input via its two auxiliary inputs (AUX) – one located at the front panel of the main unit and the other located at rear panel of the main unit. The auxiliary input in the front panel is given the priority over the one of the rear panel. This means, if the two auxiliary inputs are used simultaneously, the main unit receive the auxiliary input signal connected to its front panel only. The selection device in the CONNECTOR board selects the auxiliary input signal from the front panel when its auxiliary input signal connector of the front panel is connected.

The auxiliary unit is connected to the I/O board through either the I/O board's STANDARD connector CN103, or HTOUT connector CN106. In standard application, the STANDARD connector CN103 is used. The main unit receive the various alarm signals (depending on the auxiliary unit, $ETCO_2$ alarm or SpO_2 alarm) via the AUX1C pin (pin No.4) of auxiliary connector.
For external unit that requires the QRS synchronizing signal (HTOUT), the HTOUT connector CN106 is used. The pin No.4 of the auxiliary connector now carries the output signal (HTOUT) to the external unit.

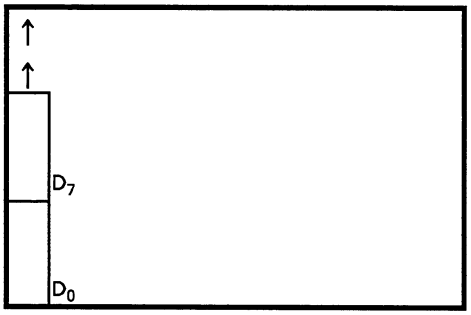
◆ Hardcopying Processing Circuit

The function of this circuit is to allow the recorder to hardcopy the display on the screen of the display unit. To do this the format of the screen data needs to be converted so that the recorder can print the information.

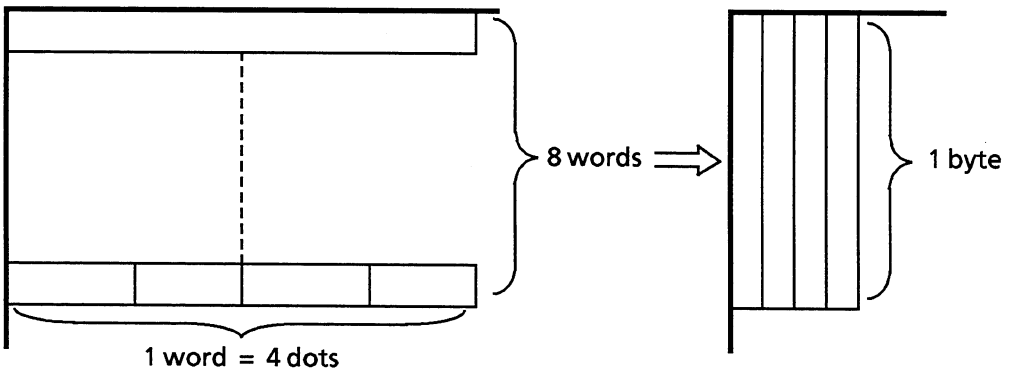
The screen data is arranged from left to right and from top to bottom as shown in the illustration below.



The hardcopy data to the recorder is arranged from bottom to top and from left to right as shown in the illustration below.



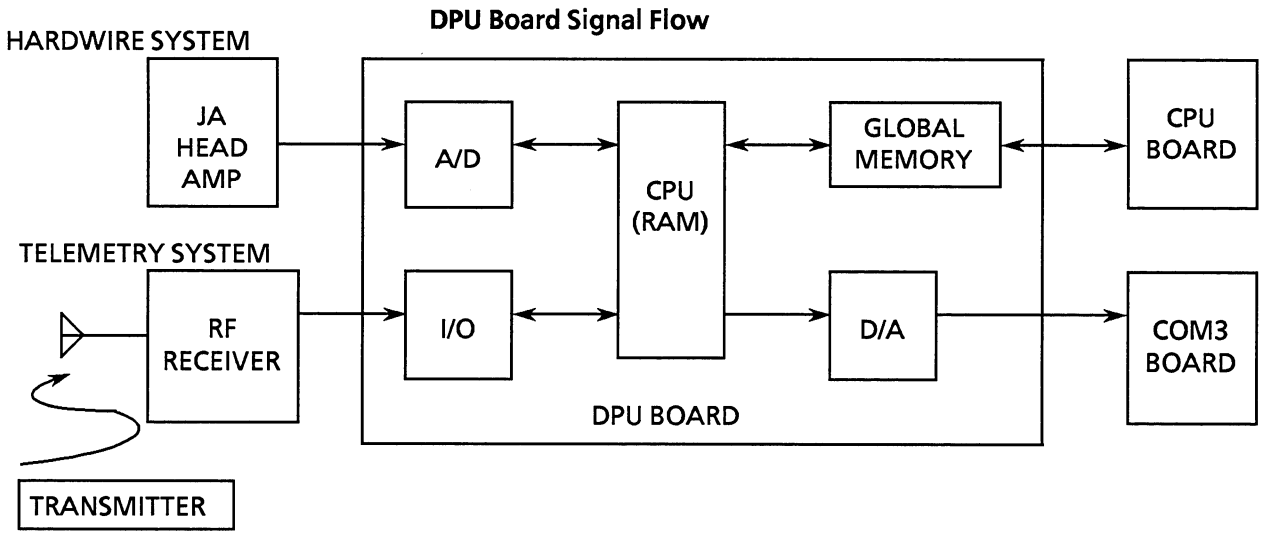
The screen 4 bit data (R, G, B, and I) is converted to 4 bit recorder data.
This 4 bit recorder data represents 1 printing dot. Hence, 1 WORD of screen is converted into 4 dots of printing information. The shift registers IC505 ~ 508 input the 1 WORD screen data 8 times before they output 4 BYTE of vertical arranged printing data.



For printing the characters displayed on the screen, the addresses of the characters are read by ANKROMs IC509 and 510. Since the character data for the screen is doubled to increase the character width, this process is replicated in this circuit. Here, IC511 and 512 are used so that the vertical printing character data read out from the ANKROMs is doubled. The horizontal printing character data is doubled through software program to balance out the final printing.

3-2-5 DPU Board, UP-0670

◆ **General**



The Data Processing Unit (DPU) board processes vital signs data, from the hardwired input box or telemetry transmitter, with the slave Micro Processing Unit (MPU) [68HC000] which is controlled by the master MPU on the CPU board (UR-3027).

• Hardwired System

The DPU board controls head amplifiers and processes ECG/Respiration analog signals before timesharing or directly timeshares the other analog signals with the 16-ch. Multiplexer (IC705 & 706).

The DPU board converts all the analog signals to digital signals with the 12-bit A/D converter (IC725) through the Gain selector (IC723) [twice gain: blood pressure signals. once gain: the others] and Base-line shifter (IC721).

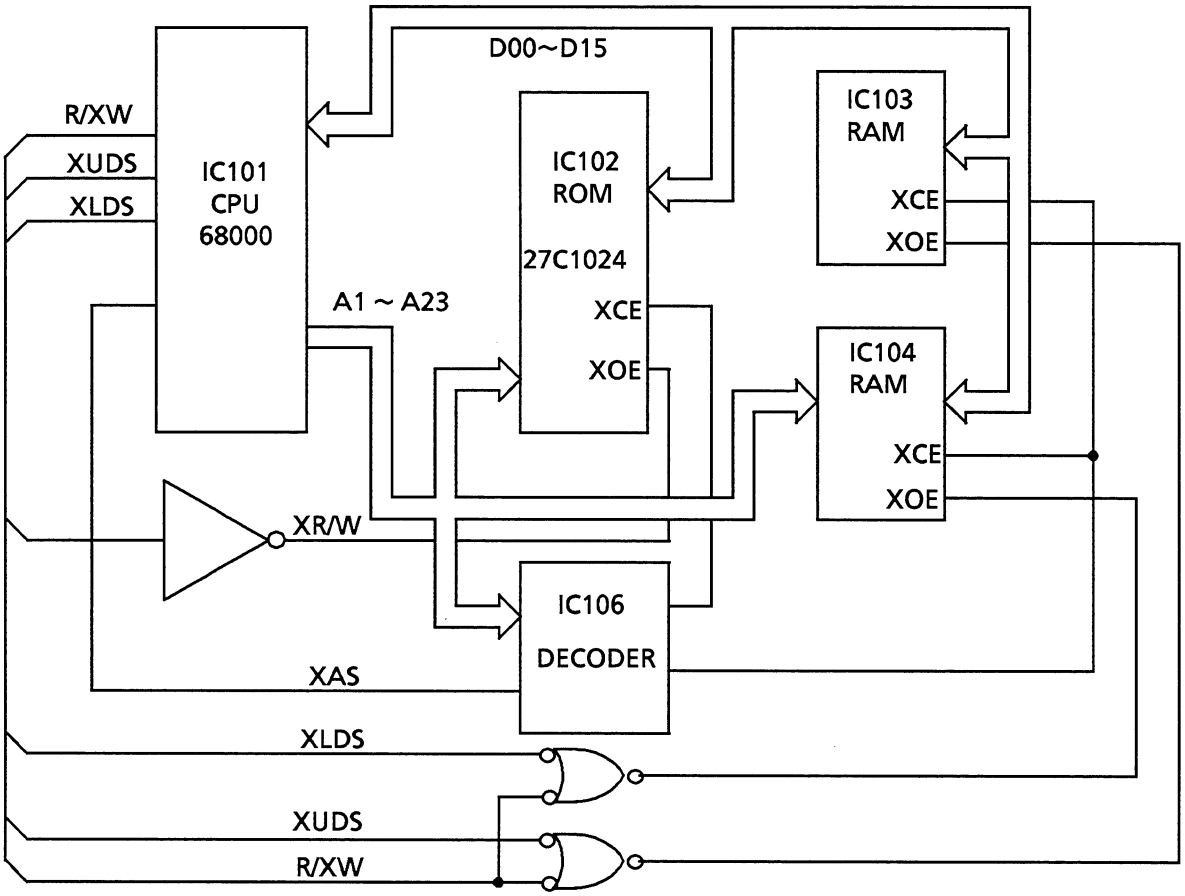
The DPU board primarily formats the digital signals with the slave 16-bit MPU [68HC000] (IC101) and stores the formatted data into the Global memory (IC225 & 226) so that the CPU board reads the data from the global memory at a fixed interval (128 msec.).

• Telemetry System

The analog wave acquired a patient is converted to digital data on a transmitter and sent to the main unit. After reception of the data on RF receiver unit, the data is converted from serial to parallel by gate array IC and then read by 16 bit CPU.

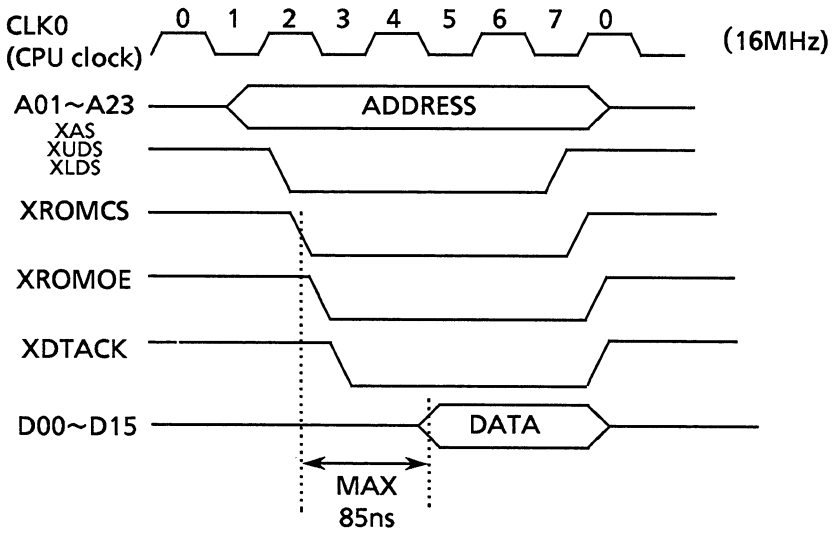
The processing method afterward is the same as the above hardwired system.

◆ **MPU/ROM/RAM Circuit**



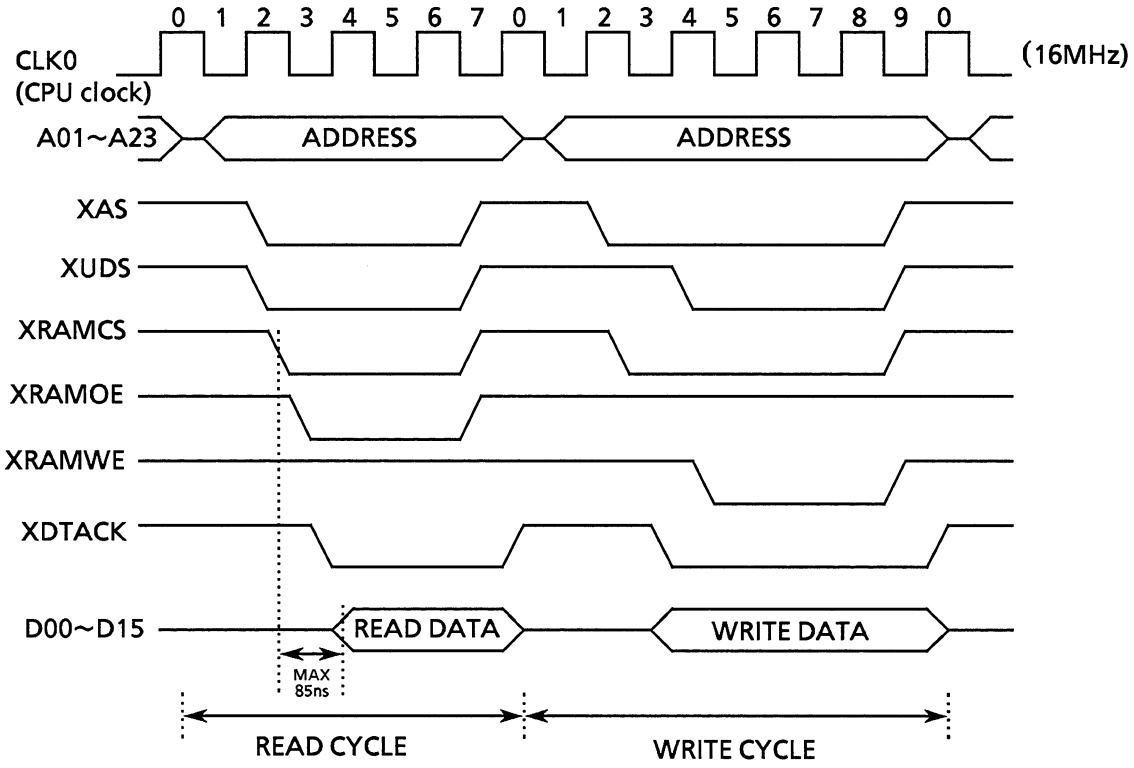
The Micro Processor Unit MPU [68000] (IC101) accesses ROMs (IC102) or RAMs (IC103,104) as follows:

[ROM ACCESS TIMING CHART]



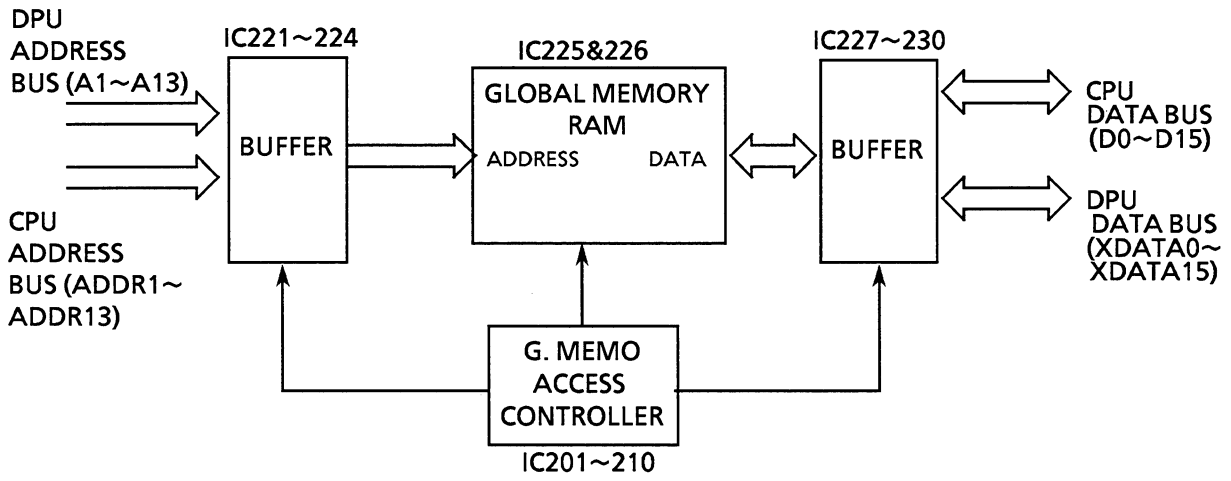
The ROM (IC102) provides 1 Mbit memory and 85 ns access time. The total memory capacity of the ROM is 128 kbytes.

[RAM ACCESS TIMING CHART]



The RAM provides 256 kbit memory and 85 ns access time. The total capacity of the RAMs (IC103,104) is 32 kwords.

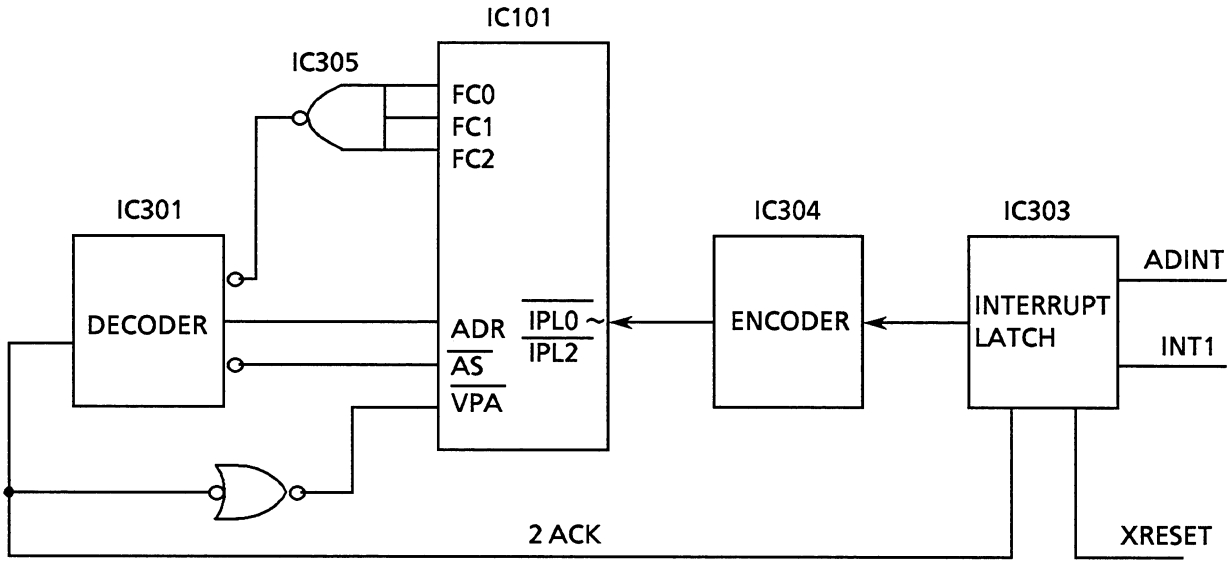
◆ **Global Memory Control Circuit**



XDATA, XADDR: from System Bus
D, A: from CPU Bus of DPU

The above global memory control circuit provides dual access function to the global memory (IC225&226) from the master MPU on the CPU board or the slave MPU on this board for communication between the CPU and DPU board.
The dual access function is controlled by the global memory access controller (IC201~210). The access controller accepts a former access and keeps another one waiting when both accesses are found.
The global memory data is read, modified or written by both MPUs.

◆ **Interrupt Control Circuit**



The above circuit generates an Auto-vectored interrupt to the MPU on this board or a Vectored interrupt to the MPU on the CPU board.

• Auto-vectored Interrupt

The interrupt is processed with a vector generated in the MPU.
The encoder (IC143) requests an interrupt to the MPU (IPL0~2 terminal) when the interrupt request signal, ADINT or INT1 is latched by the interrupt latch (IC303).
The IC1303 latches ADINT or INT1 with a positive-going edge and resets with the initialization signal, XRESET or the individual interrupt acknowledge signal from the decoder (IC301).
The interrupt acknowledge signal from the MPU sets FC0~FC2 High and the same level signals appear on A1~A3 of Address line. They are inputted to the decoder and an interrupt acknowledge signal (ACK) is generated. Simultaneously, the ACK signal is returned to VPA terminal of MPU, which is the Auto-vectored interrupt.

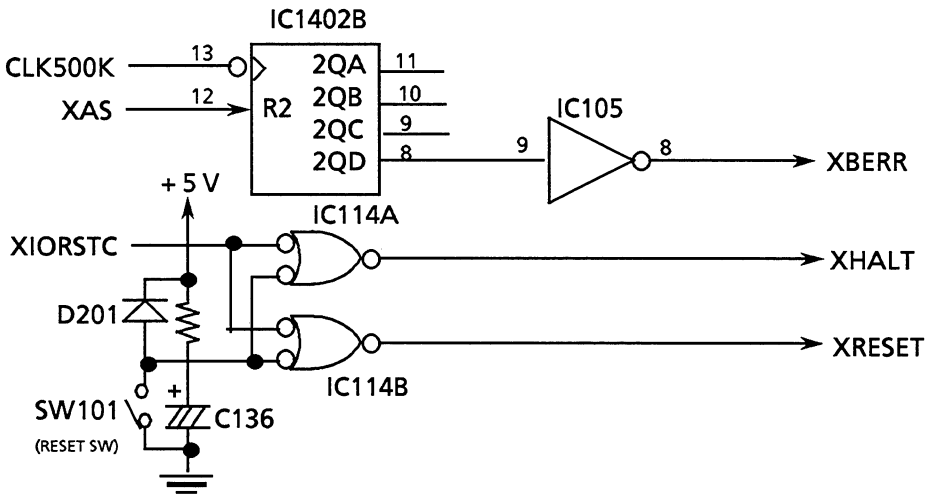
INTERRUPT PRIORITY	Interrupt Request signal	Explanation
7		No use
6		No use
5		No use
4	ADINT	Periodic interrupt for A/D conversion timing (every 2 msec)
3		No use
2		No use
1	INT1	Command interrupt from the MPU on the CPU board (at random)

• Vectored Interrupt

The interrupt signal (INT13) is generated from the MPU on the DPU board to the MPU on the CPU board approximately every 128 msec to indicate a wave data set on the global memory to the MPU (CPU board).

INTERRUPT PRIORITY	Interrupt Request signal	Explanation
INT13	XCPU INT	Periodic Interrupt to CPU from DPU to have wave data (approx 128 msec) set

◆ **Bus Error & Reset Circuit**

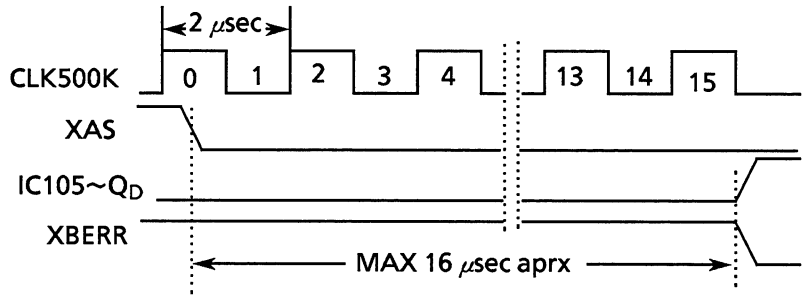


● **Bus Error Detecting circuit**

The detecting circuit informs the MPU (IC101) on this board of any trouble found in the bus cycle during an execution. If Address Strobe signal XAS is not negated on the Counter (IC402B) within 16 μsec due to the following condition, Bus Error XBERR is outputted to the MPU through the IC105.

DTACK signal is not asserted.

VPA signal is not asserted.



● **Reset circuit**

The reset circuit which consists of IC114B,R201 and C201 generates the reset signal XRESET (XHALT) in the following case.

When the reset switch (SW101) is depressed;

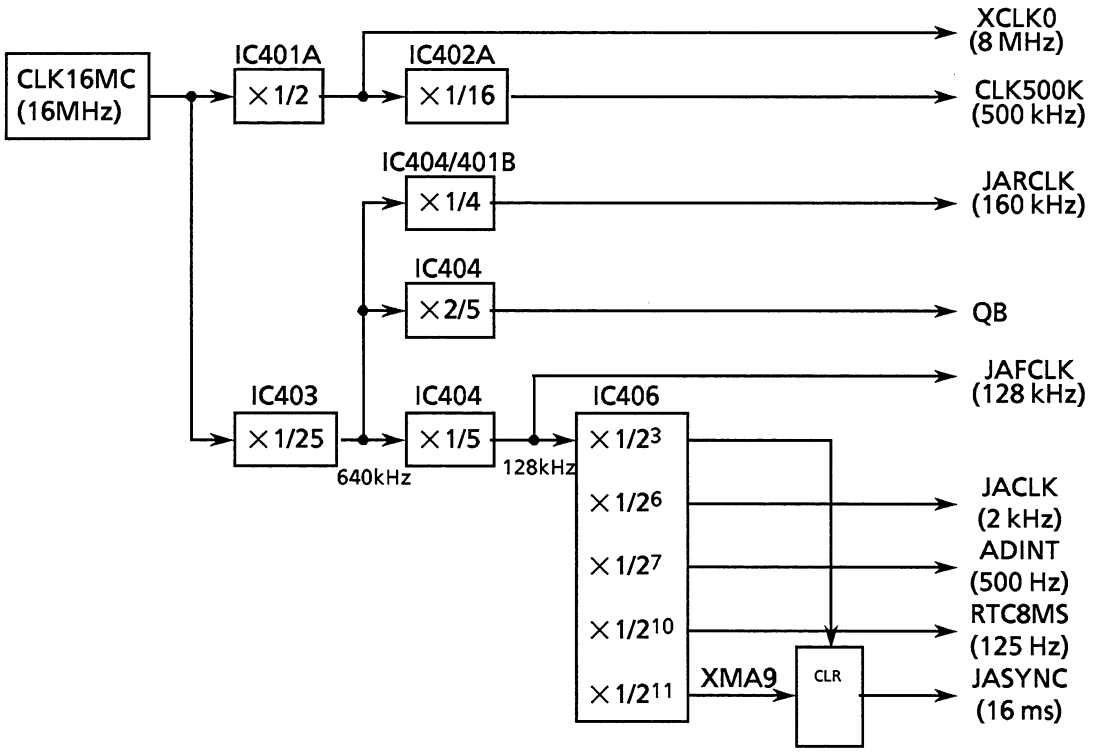
When the power switch is turned on;

When a reset command is executed;

When the reset signal XIORSTC is outputted from the CPU board to this circuit.

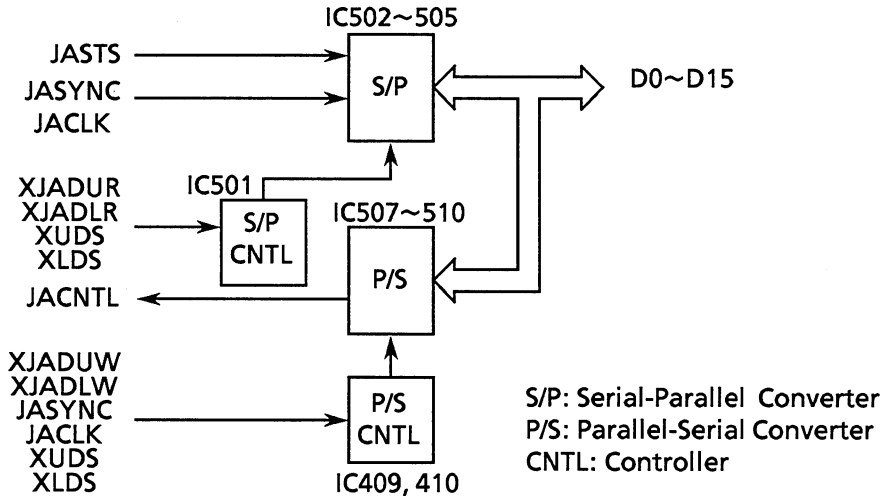
◆ Timing Control Circuit

The timing control circuit generates the following various clocks with the 16MHz system clock from the CPU board.



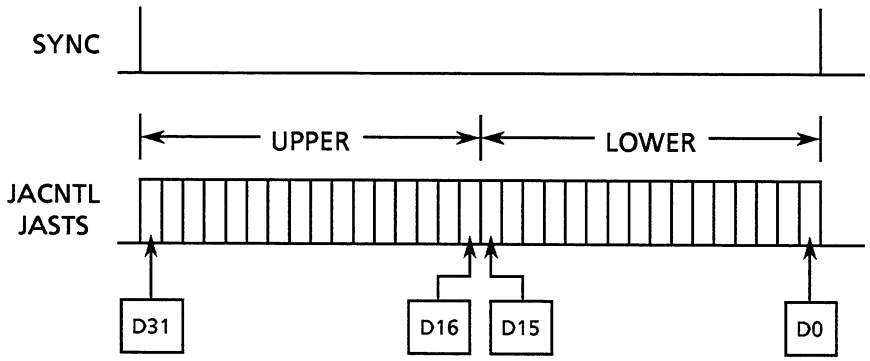
CLOCK	Frequency	Duty	Function
CLK0 XCLK0	8 MHz	50 %	MPU clock on DPU board
CLK500K	500 kHz	50 %	Clock to detect Bus Error or convert A to D, D to A
JARCLK	160 kHz	50 %	Clock to detect respiration waveform at the input box
JAFCLK	128 kHz	40 %	Clock to float the input circuit on each Head Amp board
JACLK	500 μS	50 %	Clock to communicate (DPU - Input box)
ADINT	2 ms	50 %	Timing clock to convert A to D every 1ms
RTC8MS	8 ms	50 %	Timing clock to interrupt to CPU board (ever 8 ms) Timing clock to synchronize wave display between CPU board and CRTC board
JASYNC	16 ms	See next page	Timing clock to synchronize communication (DPU-Input box)

◆ JA Data Control Circuit

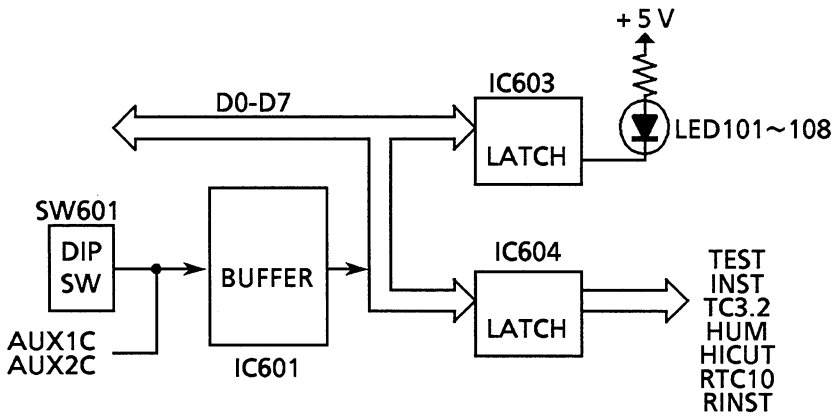


32-bit serial format signals JACNTL and JASTS are transferred between the DPU board and Input box.
The Parallel-serial converter (IC507~510) converts parallel data D0~D15 to the serial format signal JACNTL to control the input box.
The Serial-parallel converter (IC502~505) converts the serial format signal JASTS to parallel data D0~D15. The JASTS signal indicates the status of the input box to the MPU on this board.

JACNTL: to control each head amplifier and LEDs/key sound on the input box
JASTS : to indicate the status of each head amplifier and keys in the input box



◆ **LED/DIP Switch Circuit**



The buffer (IC601) is an input port to indicate the status of the DIP switch (SW102) and external signals AUX1C/AUX2C to the MPU on this board.

The latch (IC603) is an output port to latch data for the LEDs (LED101~108) indication.

The latch (IC604) is an output port to latch control signals for the ECG/RESP Processing circuit on this board.

[IC601]

D0	DIPSW0	OFF {Factory Set}
D1	DIPSW1	↓ (1: OFF. 0: ON)
D2	DIPSW2	
D3	DIPSW3	
D4		{No use}
D5		
D6	AUX1C	(Active-low)
D7	AUX2X	

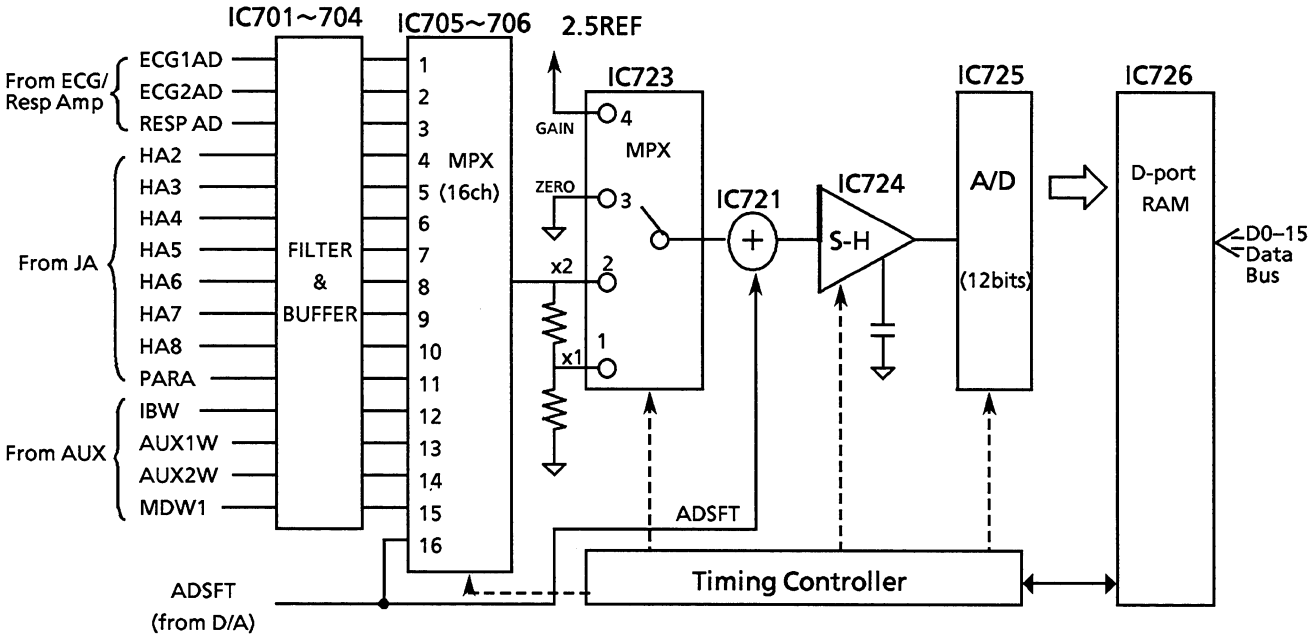
[IC603]

D0	LEDBIT0	(1: No lighting) (0: Lighting)
D1	LEDBIT1	
D2	LEDBIT2	
D3	LEDBIT3	
D4	LEDBIT4	
D5	LEDBIT5	
D6	LEDBIT6	
D7	LEDBIT7	

[IC604]

D0		No use		
D1	TEST	ECG Calibration	(1: Test.	0: Normal)
D2	INST	ECG INST	(1: ON.	0: OFF)
D3	TC3.2	ECG Time Constant	(1: 3.2s.	0: 0.5s)
D4	HUM	ECG Hum Filter	(1: ON.	0: OFF)
D5	HICUT	ECG Low-pass Filter	(1: ON.	0: OFF)
D6	RTC10	RESP Time Constant	(1: 10s.	0: 1.5s)
D7	RINST	RESP INST	(1: ON.	0: OFF)

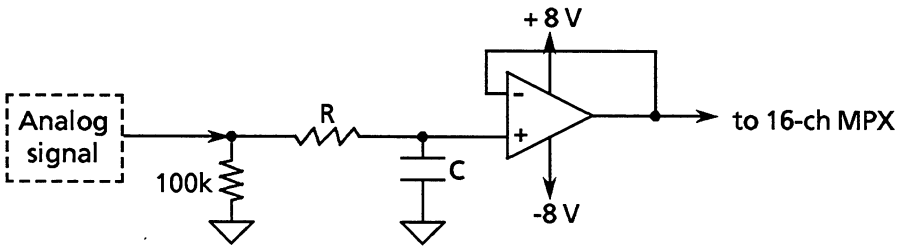
◆ A/D Control Circuit



Analog signals collected from the input box or external equipment are timeshared by the 16-ch. Multiplexer through the Filter & Buffer.
The timeshared signal is sampled and held by the Sample-holder after adding a DC voltage for the base line shift (ADSFT signal from D/A converter) to the signal with the Adder through the Gain selector multiplexer.
The held signal is converted to digital signals by the 12-bit A/D converter and written into Dual-port RAM by AUTO A/D system.

• Filter & Buffer (R014~117, C101~115, IC173~176)

The low-pass filter composed of the resistor and capacitor provides the following cut-off frequency.



RESP signal: 16 Hz
The others: 1.6 kHz

• 16-ch Multiplexer (IC705&706)

CH	SIGNAL	Explanation
1	ECG1AD	↕ Output from ECG/RESP Processing circuit
2	ECG2AD	
3	RESPAD	
4	HA2	↕ Output from Head Amplifier
5	HA3	
6	HA4	
7	HA5	
8	HA6	
9	HA7	↕ Extra
10	HA8	
11	PARA	Parameter recognition signal
12	IBW	Interbed ECG in connecting the other BSM (ICU 7000 series)
13	AUX1W	↕ External input
14	AUX2W	
15	MDW	Delayed ECG from COM3 board
16	ADSFT or RSSI	A/D shift voltage for inspection

• Gain Selector Multiplexer (IC723)

The multiplexer selects gain or generates +2.5 V d.c. or 0V for inspection according to the following table.

CH	Output	Function
4	2.5 V REF	for Gain adjustment
3	0V	for Offset adjustment
2	× 2	for Blood pressure wave (necessary to obtain high resolution)
1	× 1	for Other wave

• Adder (IC721)

The adder provides a base line shift function to convert each timeshared signal to digital signals at the most suitable position. The DC voltage signal for the base line shift ADSFT is generated by a 12-bit D/A converter. The function is mainly used to auto-zero the base line of blood pressure waveforms.

Shift range: within ±5 V

Resolution: by 2.5 mV

• Sample-holder (IC724)

The sample-holder samples and holds each timeshared signal to prevent the voltage level from changing during A/D conversion.

Sampling time: 10 μsec

Error: 0.01 % or less

Capacitor for holding: 1000 pF

• A/D Converter (IC725)

The A/D converter provides the following specifications.

[Model name: AD574]

Resolution: 12 bits

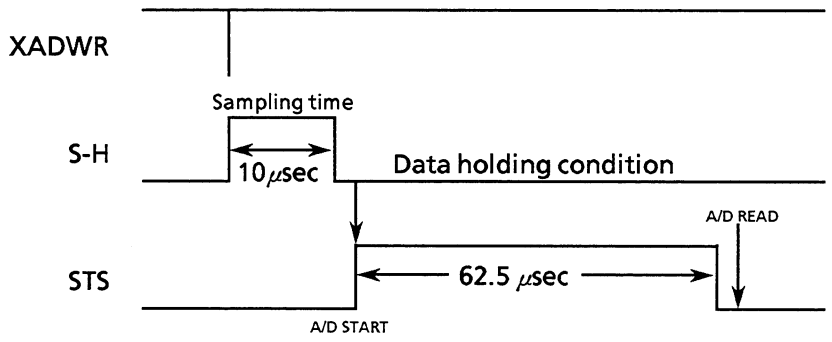
Linearity tolerance: ±1 bit

Input range: ±5.12 V (400 D/V)

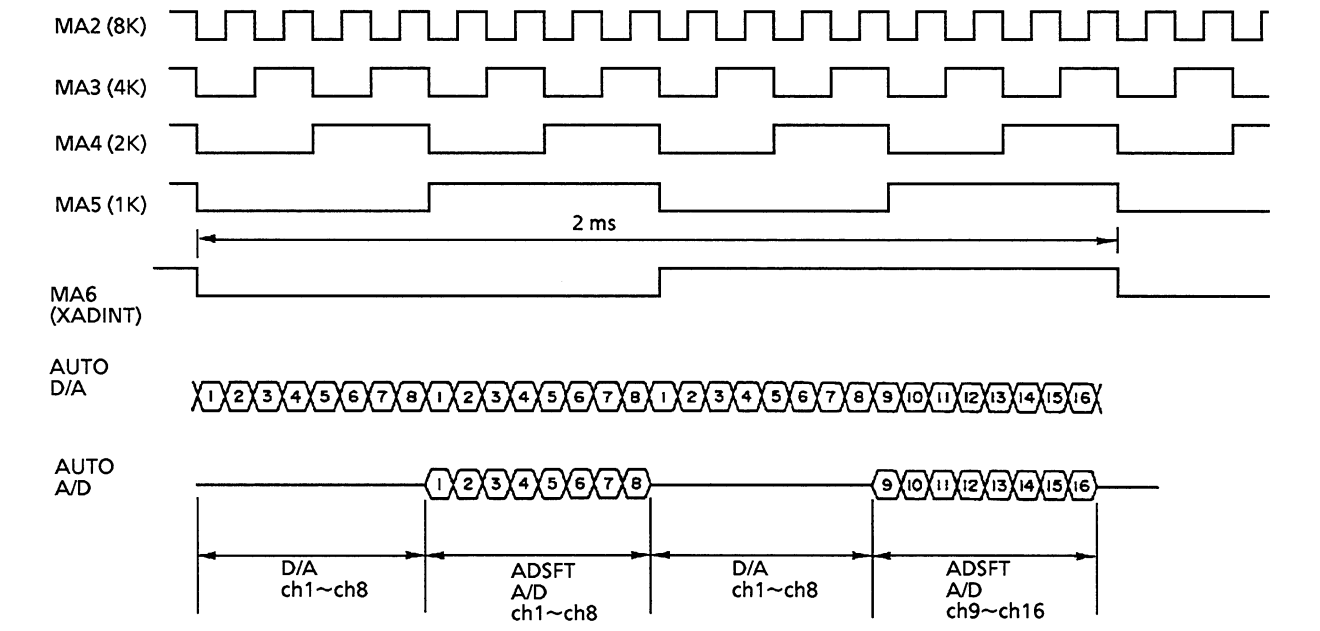
INPUT VOLTAGE	A/D OUTPUT DATA	
+5.12 V	4095 D	FFF H
+5.00 V	4048 D	FD0 H
0.00 V	2048 D	800 H
−5.00 V	48 D	30 H
−5.12 V	0 D	0 H

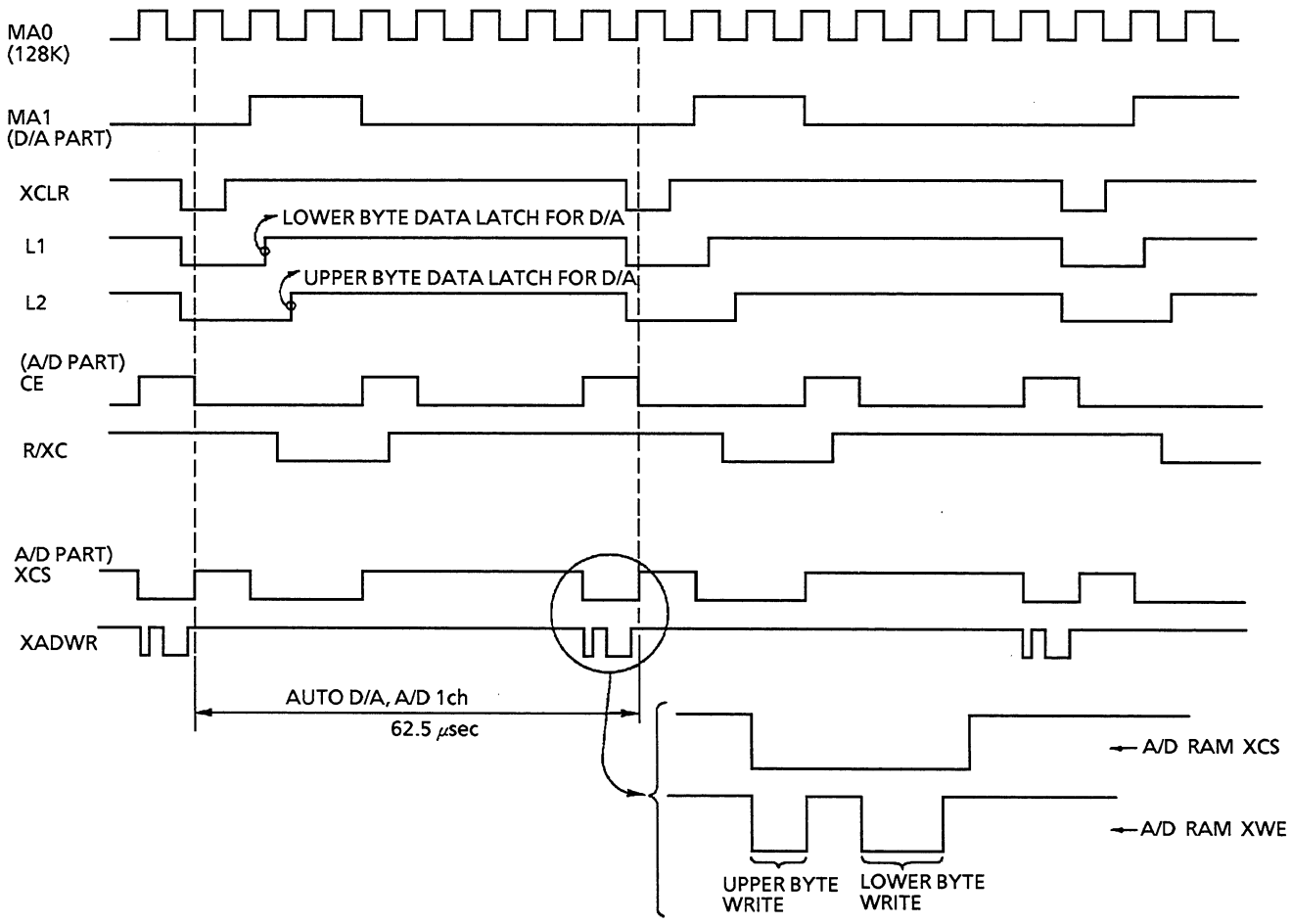
Converting time: 62.5 μsec

[Timing Chart]

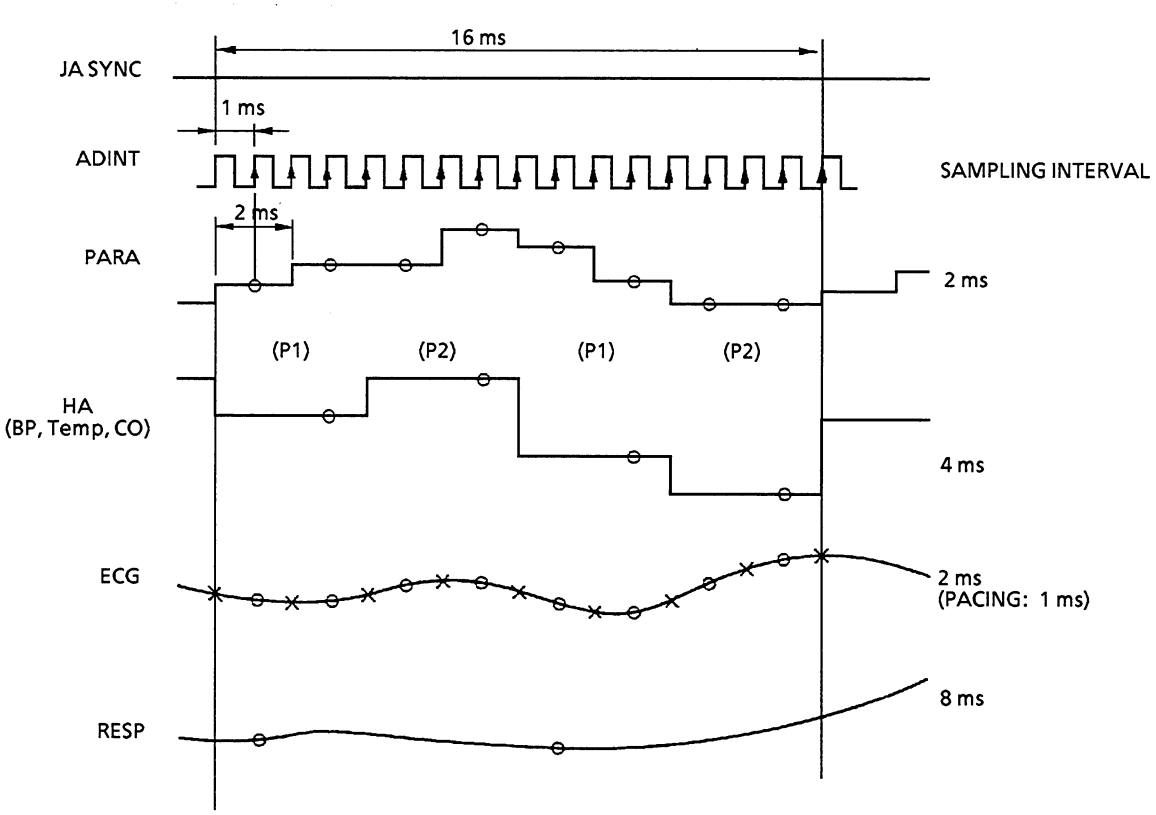


[A/D . D/A Basic timing]: Generated by IC406

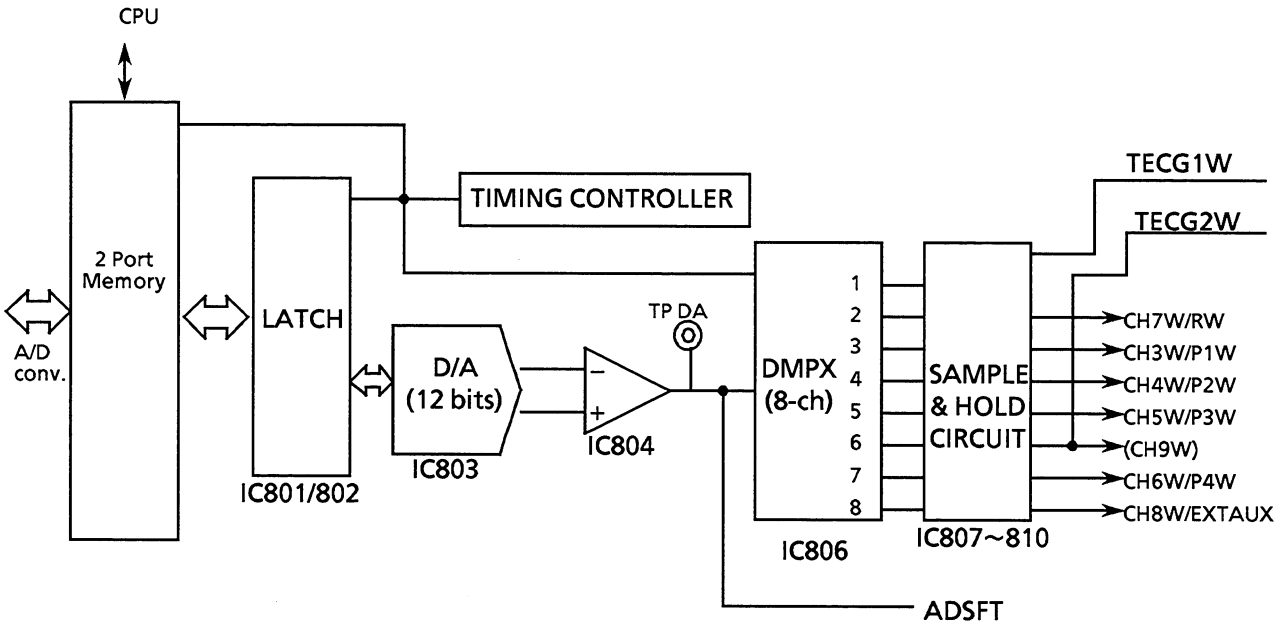




[A/D SAMPLING TIMING CHART]



◆ **D/A Control Circuit**



Data for D/A is converted by the 12-bit D/A converter through the latch (IC801&802).
The D/A converted signals are distributed to each signal line by the 8-ch Demultiplexer.
Channel 1 & 6 output TECG1W & 2W, and the other channels output each waveform, Respiration, Blood pressure or External input waveform.
The D/A signal is outputted synchronized with A/D conversion timing.
Each waveform signal except the Respiration wave is outputted approximately every 1msec.

- **D/A converter (IC803)**

The D/A converter provides the following specifications.

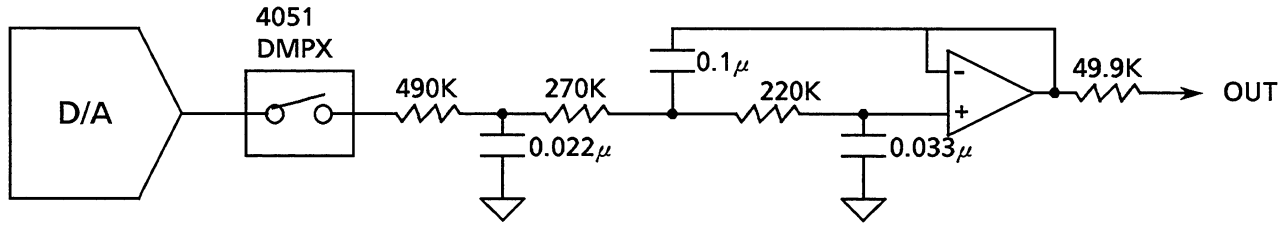
[Model name: HA-17012PB]
Resolution: 12 bits
Linearity tolerance: ±0.05 %FS (±2 bits)
Output range: ±5.12 V (1 V/400 D)
Settling time: 250 nsec

D/A INPUT DATA		D/A OUTPUT VOLTAGE
4095 D	FFF H	+5.12 V
4048 D	FD0 H	+5.00 V
2048 D	800 H	0.00 V
48 D	30 H	−5.00 V
0 D	0 H	−5.12 V

● **8-ch. Demultiplexer (IC806)**

CH	SIGNAL	Explanation
1	TECG1W	Telemetry ECG wave
2	CH7W/RW	Analog output to CNS
3	CH3W/P1W	
4	CH4W/P2W	
5	CH5W/P3W	
6	(CH9W)	
7	CH6W/P4W	
8	CH8W/EXTAUX	

● **D/A sample and hold circuit**



Sampling time: 62.5 μsec
Sampling interval: 1 msec
Holding frequency characteristic: 62.5 Hz at minimum (ECG),
31.25 Hz at minimum (0thers)
Held voltage gap after 4msec: approx. 2 mV at maximum
Output range: ±5 V
Output offset voltage: ±37 mV at maximum (ECG1)
±11 mV at maximum (ECG2)
±5 mV at maximum (CH3~CH8)

◆ ECG/RESP Processing Circuit

• ECG Processing circuit

The ECG processing circuit consists of the following components.

Calibration voltage generator (15 mV to 1 V on CRT)
Pacing pulse limiter ..... (1)
Time constant selector (0.5 sec or 3.2 sec)
Instantaneous short circuit in ECG lead selection
Auto-instantaneous short circuit ..... (2)
Hum filter (50/60 Hz: common use)
Low-pass filter

Each ECG processing circuit in the dual ECG lead is the same.
When the hum filter is on in the monitor mode, the ECG processing circuit functions by hardware to directly pass the ECG signal to the A/D converter, not through the low-pass filter, since pacing pulse detection by software needs ECG data including high frequency component.

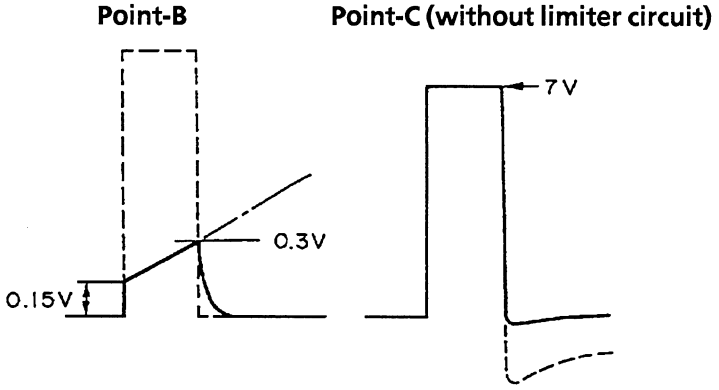
NOTE

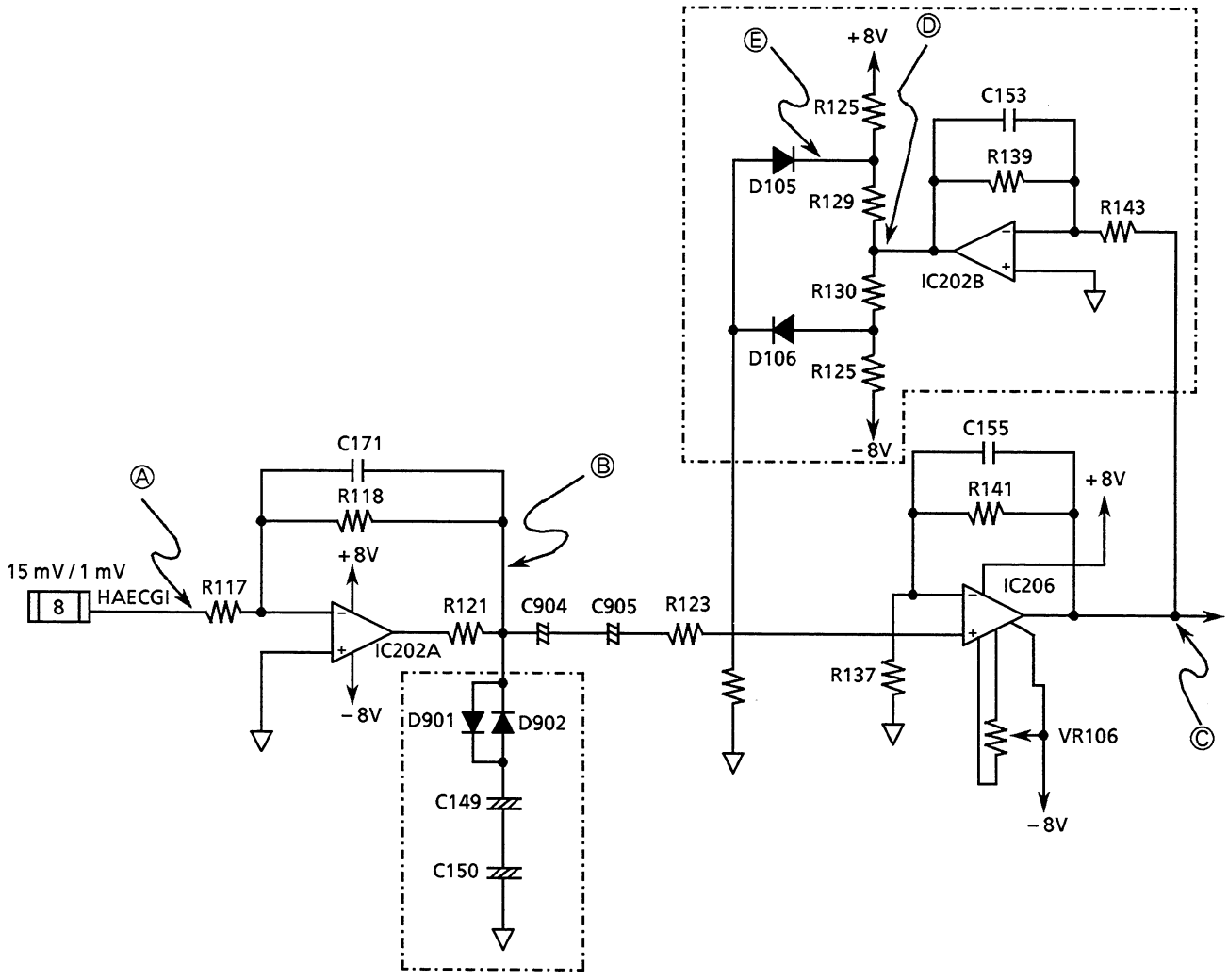
QRS detector and Pacing pulse detector which had been processed by hardware are processed by software.

1) Pacing-pulse Limiter circuit

A large amplitude signal such as a pacing pulse is limited at point-B by having either a schottky diode, D901 or D902 on while a small amplitude signal such as ECG (15 mV at the point-B to 1mV at the ECG Head Amp input) keeps both diodes D901 and D902 off (high impedance).

If the limiter circuit is removed, the large amplitude signal through the capacitors (C904/905) will make the base line shift as shown in the following figure, and the ECG wave next to every pacing pulse will not be stable on the CRT.



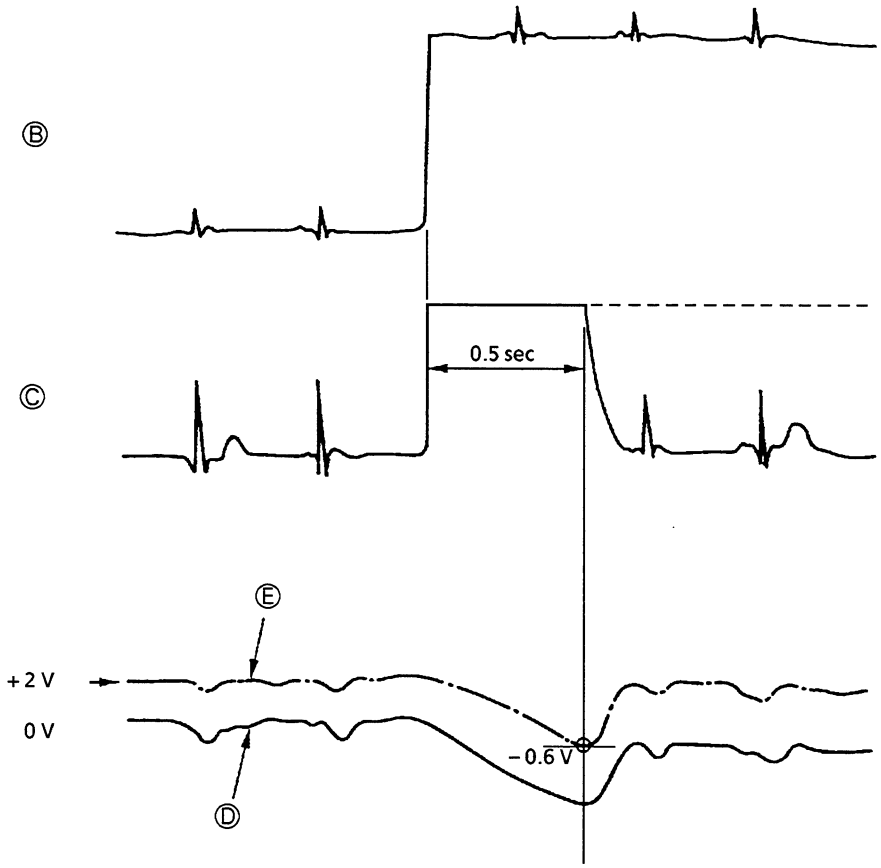


2) Auto-instantaneous short circuit

This circuit instantaneously discharges the charged coupling capacitor (C904/905) caused by a rapid large change of an offset voltage before the ECG Head Amp input.

When the base line shifts largely upward (toward positive) at point-C due to the offset voltage change as shown in the following figure, the base line gradually shifts from the initial setting, +2 V level toward the negative at point-E while shifting toward the negative at point-D gradually. After the 0.5 seconds from the offset voltage change, the charged capacitor (904/905) is discharged through the diode (D903) since D903 comes on. Therefore, the base line is recovered to approximately 0 V level.

When the base line largely shifts downward(toward negative) at point-C, the base line gradually shifts from the initial setting −2 V level toward the positive at point-E while shifting toward the positive at point-D gradually. After 0.5 seconds, the C904/905 is discharged through the diode (D904) since D904 comes on. Therefore, the base line is recovered to approximately 0 V level.

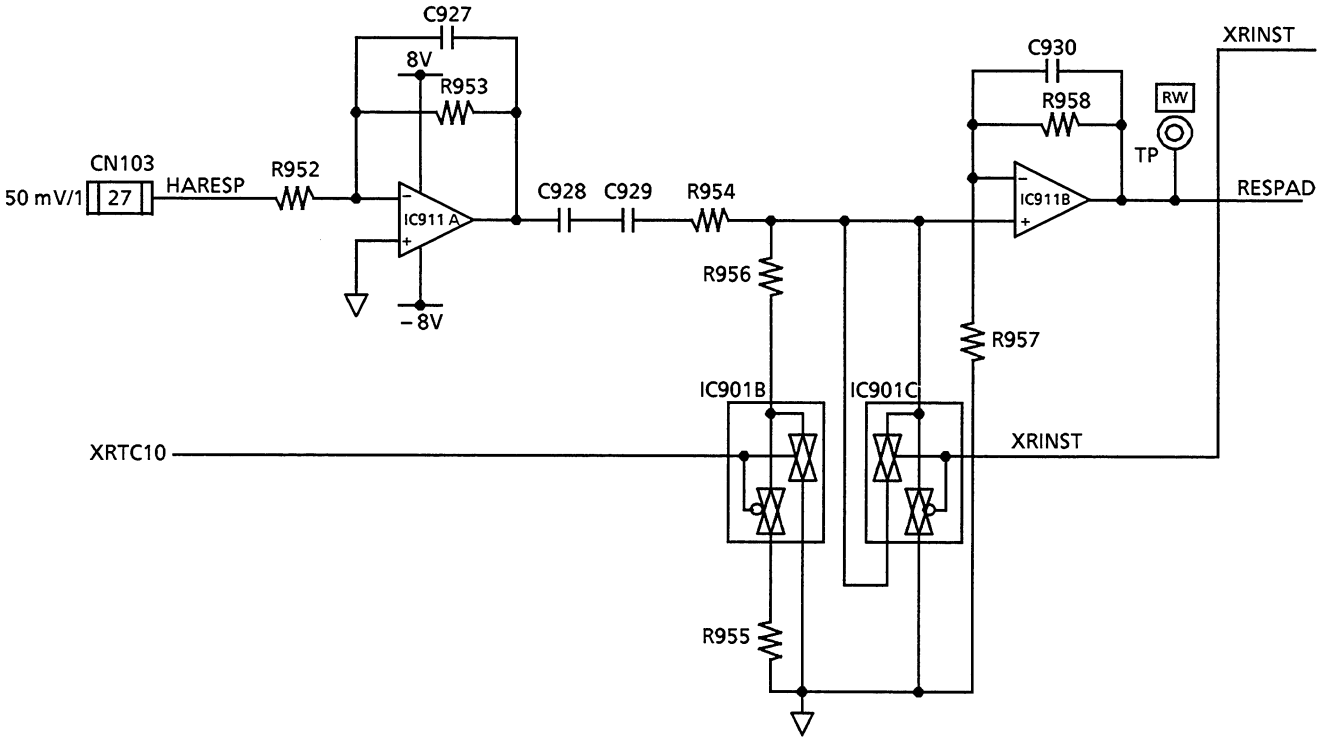


• Respiration-wave Processing circuit

The circuit consists of the following components.

20 time-inverted Amplifier (IC911A/B)
1.5/10 seconds Time constant Selector (IC901B)
Instantaneous Short circuit (IC901C)

When a respiration wave signal HARESP is deflected to the saturation level, the base line is recovered to approximately 0 V level by software.



◆ JA Interface & Power Supply Circuit

This circuit generates control signals (CNTL, SYNC, FCLK, RCLK), status signal (STS) and power source for the input box .

The circuit composed of resistors (R971~974, R001, R002, DA921, DA922) is a protection circuit.

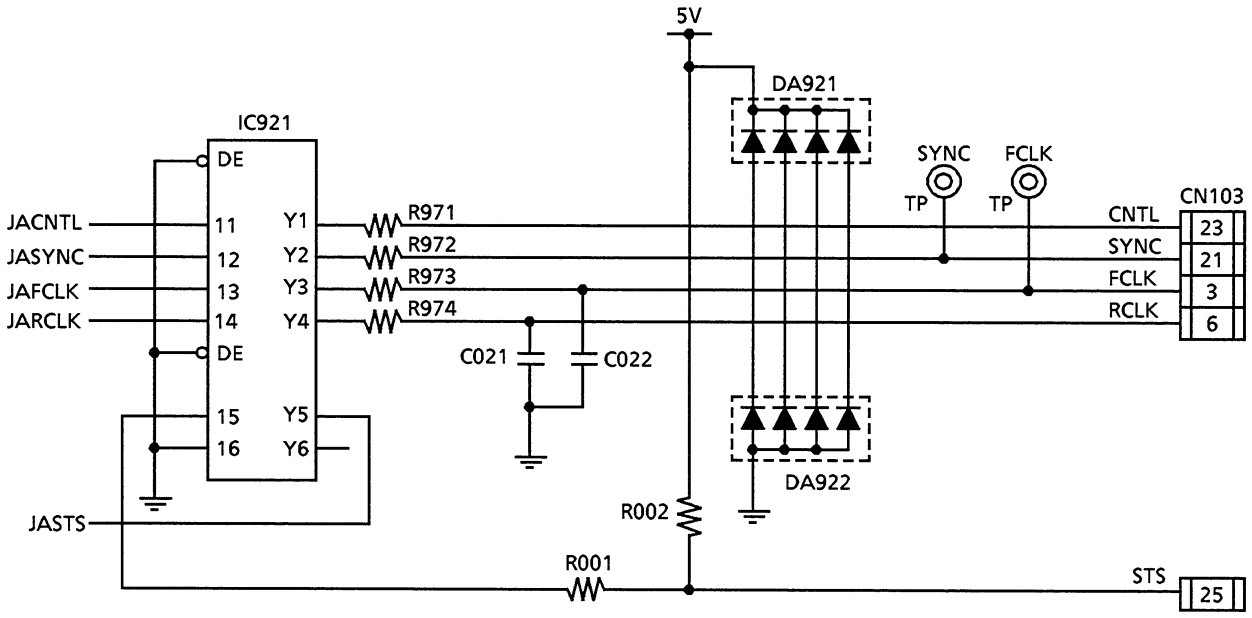
The buffer (IC213) functions to the control and status signals.

The capacitor (C132/133) is a low-pass filter component to allow the ringing on the clock pulses (FCLK,

RCLK) to be ignored.

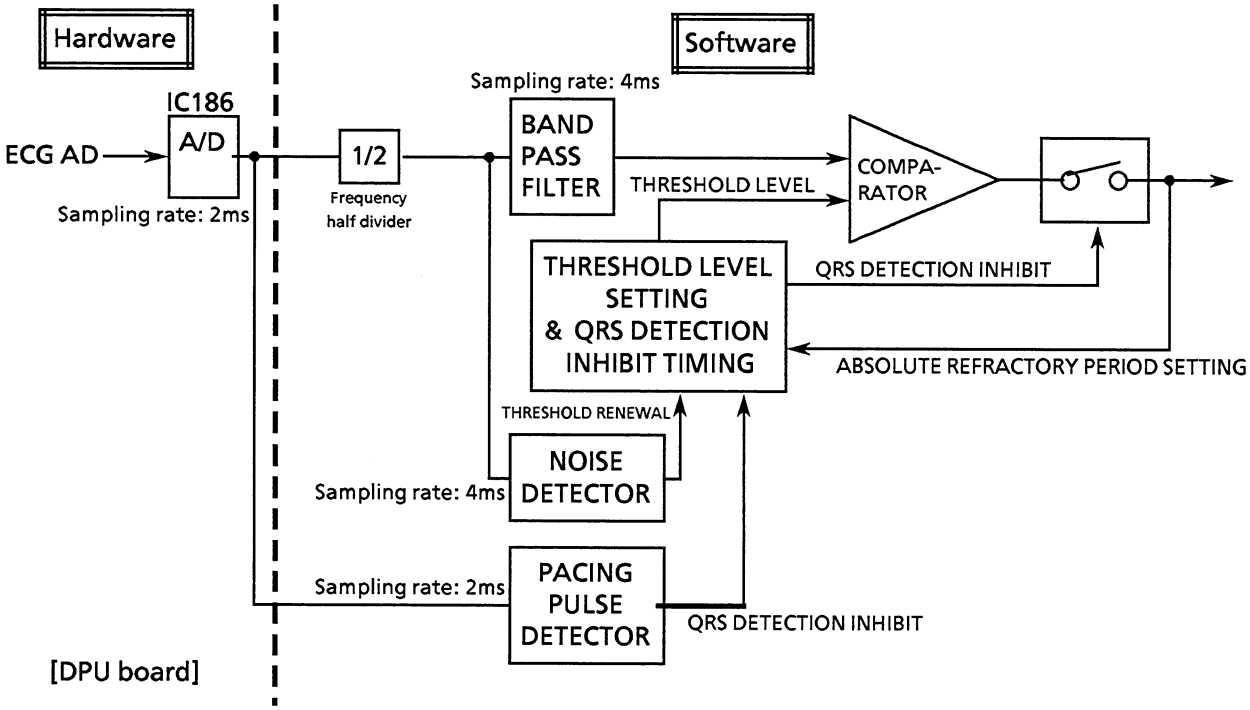
The power source supples the input box with ±8 V and +21 V.

The ground terminals, E1(for ±8 V) and EH/EHC/ER(for +21 V), are shorted to the analog signal ground AGND (for ±15 V, A/D and D/A converter power source).



◆ Software Data Process [Hardwire system]

(1) ECG Data process



● Definition

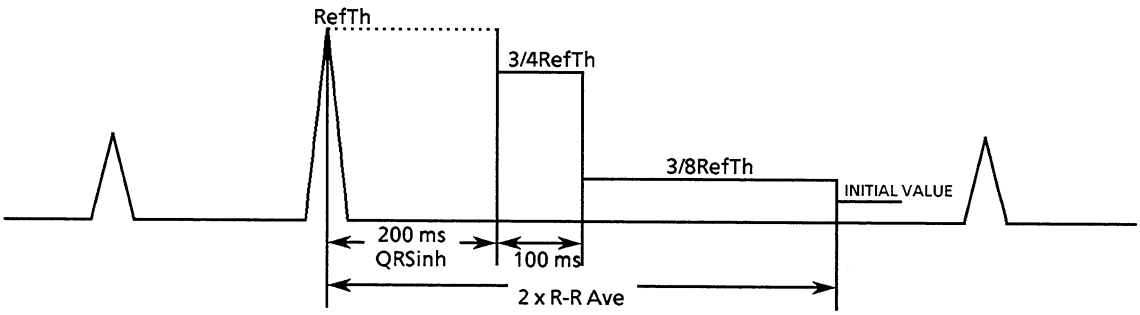
Sampling data through QRS band pass filter is defined as Reference Threshold level "RefTh" when a QRS is detected.

Another QRS detection is inhibited for 200 msec after detecting a QRS. The 200msec is defined as the Absolute Refractory period, "QRSinh".

The threshold level is changed according to the elapse time so as to detect the next QRS after the 200msec.

The threshold level data is defined as "HighTh".

Averaged R-R interval out of 4 beats is defined as "R-R Ave".



• Threshold level renewal

When the next QRS is not detected, the threshold level is changed as follows:

During QRSinh: Data inhibit

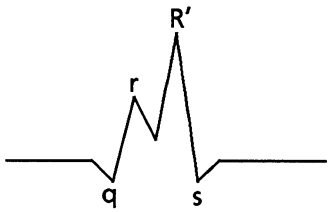
For 100msec after QRSinh: 3/4 RefTh

From the time after the 100msec to 2 x R-R Ave: 3/8 RefTh

From 2 x R-RAve to 2sec after detecting the last QRS: Initial value

When sampling data through the band-pass filter is larger than RefTh during the same QRSinh, the RefTh data is renewed with the sampling data to be the threshold level for the next QRS.

[EXAMPLE QRS]



• QRS Band-pass filter

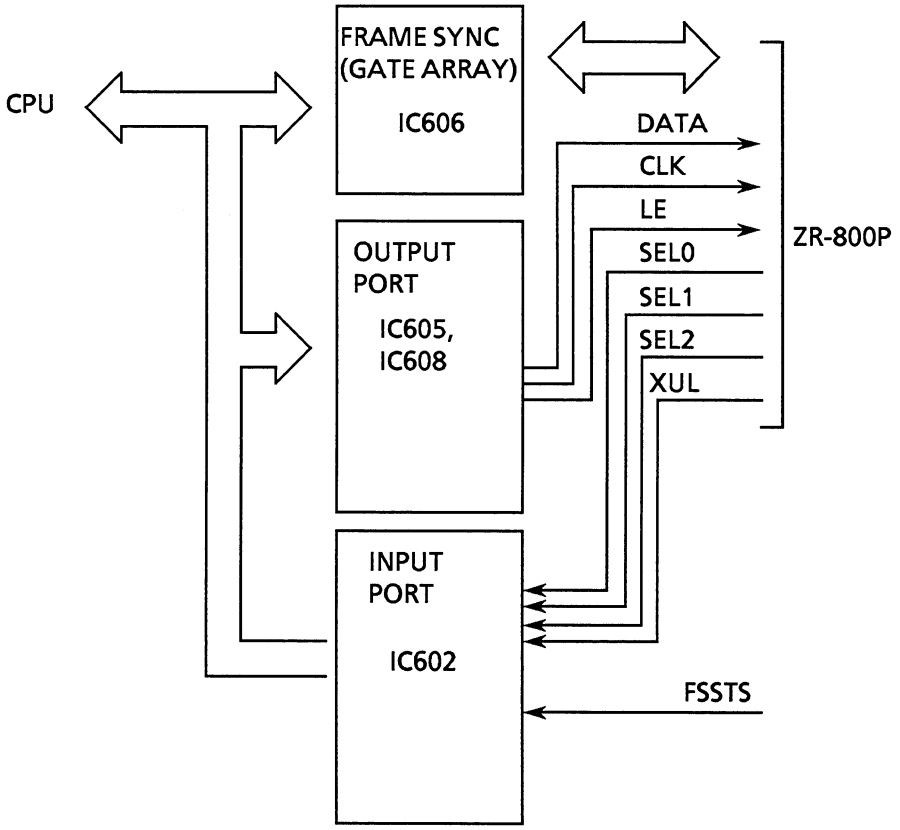
The band-pass filter consists of a low-pass filter and high-pass filter. The frequency characteristic is 8 to 20 Hz.

• QRS Detection

When 2 units of continuous sampling data or more through the filter exceeds HighTh during QRS detection enable period, the sampling data is detected and counted as a QRS.

◆ Digital Telemetry Signal Processor

Interface on DPU board for digital telemetry receiver consists of following block diagram.



IC606 receives the serial data from the receiver and converts the data to parallel one. Then it is transferred to CPU.

IC606

Signal symbol	Function	
RD	Input data in serial	Input signal
RT	Synchronization clock for input data in serial	Input signal

IC 605 is an output port latch device and outputs the receiving channel setting data to the CPU .

IC605

Pin	Signal symbol	Function	
D0	DATA	Output data	Output signal
D1	CLK	Clock for output data	Output signal
D2	LE	Latch enable signal	Output signal

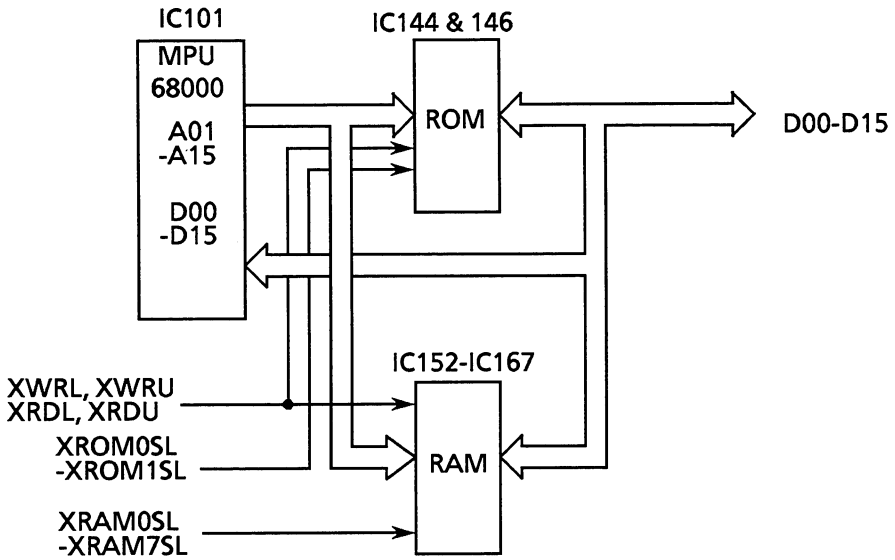
IC602 functions as an input port and inputs the condition information of the receiver to the CPU.

IC602

Pin	Signal symbol	Function	
D0	SEL0	Shows the values of DIG switch in the receiver (ZR-800P)	Input signal
D1	SEL1		Input signal
D2	SEL2		Input signal
D3	XUL		Input signal
D4	FSSTS	Asserts every 8ms	Input signal

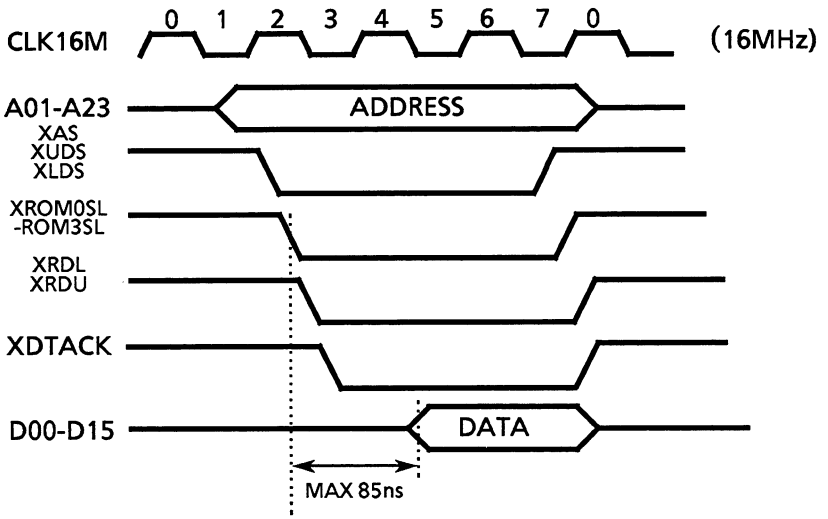
3-2-6 CPU Board, UR-3027

◆ **MPU/ROM/RAM Circuit**



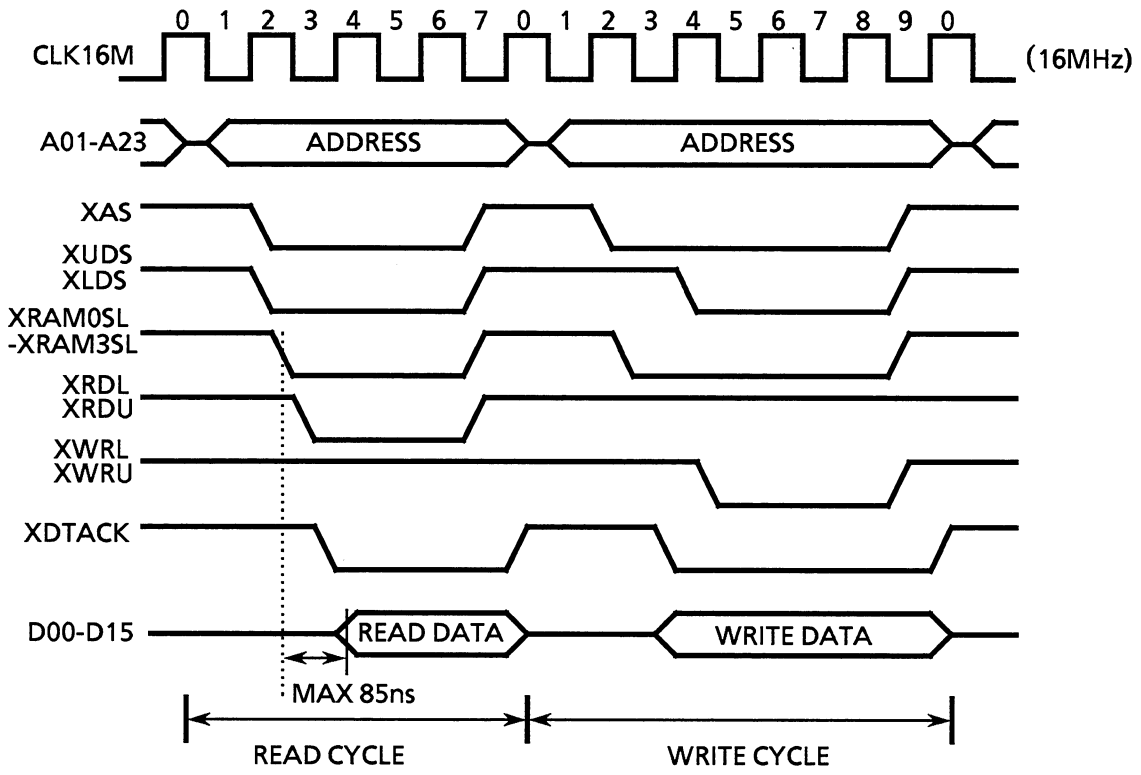
The Micro Processor Unit MPU[68000] (IC101) accesses ROMs (IC144 & 146) or RAMs (IC152-167) as follows:

[ROM ACCESS TIMING CHART]



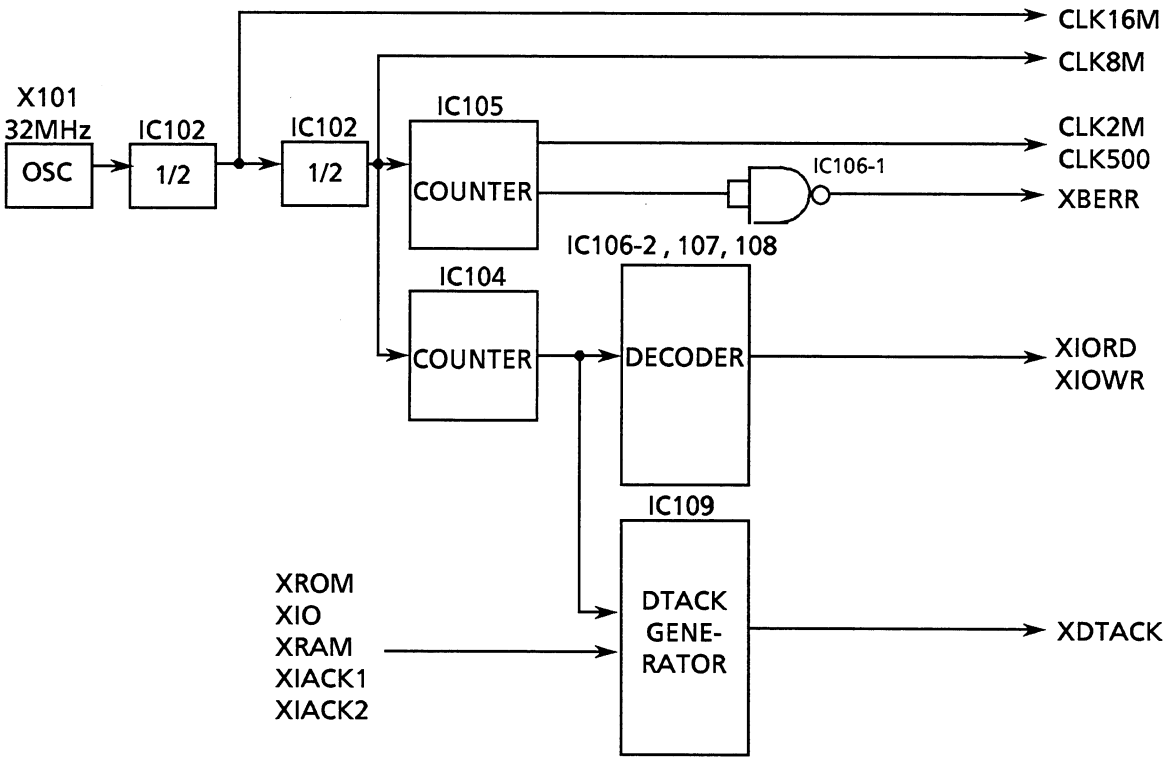
The ROM provides 128kbit memory and 85ns access time. The total memory capacity of the ROMs is 512kwords.

[RAM ACCESS TIMING CHART]



The RAM provides 32kbit memory and 85ns access time.

◆ **Timing Control Circuit**



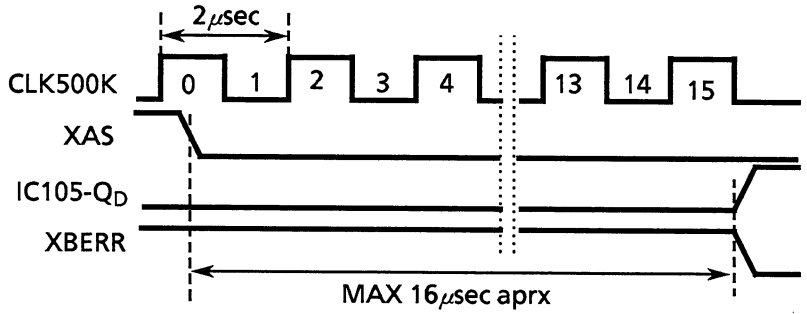
The above circuit generates clock signals, Read/Write Control signals, and Data Transfer Acknowledge signals. Moreover, the circuit provides a Bus Error Detector (IC105,106-1).

• Bus Error Detector

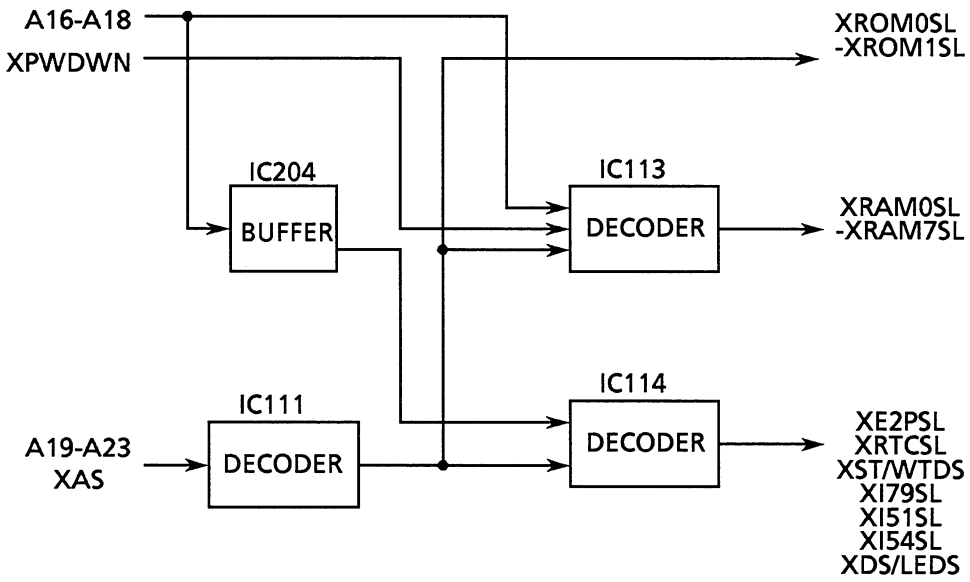
The detector informs the MPU (IC101) on this board of any trouble found in the bus cycle during an execution. If Address Strobe signal XAS is not negated on Counter (IC105-2) within16μsec due to the following condition, Bus Error signal XBERR is outputted to the MPU through the IC106-1.

DTACK signal is not asserted.

VPA signal is not asserted.



◆ **Address Decoding Circuit**

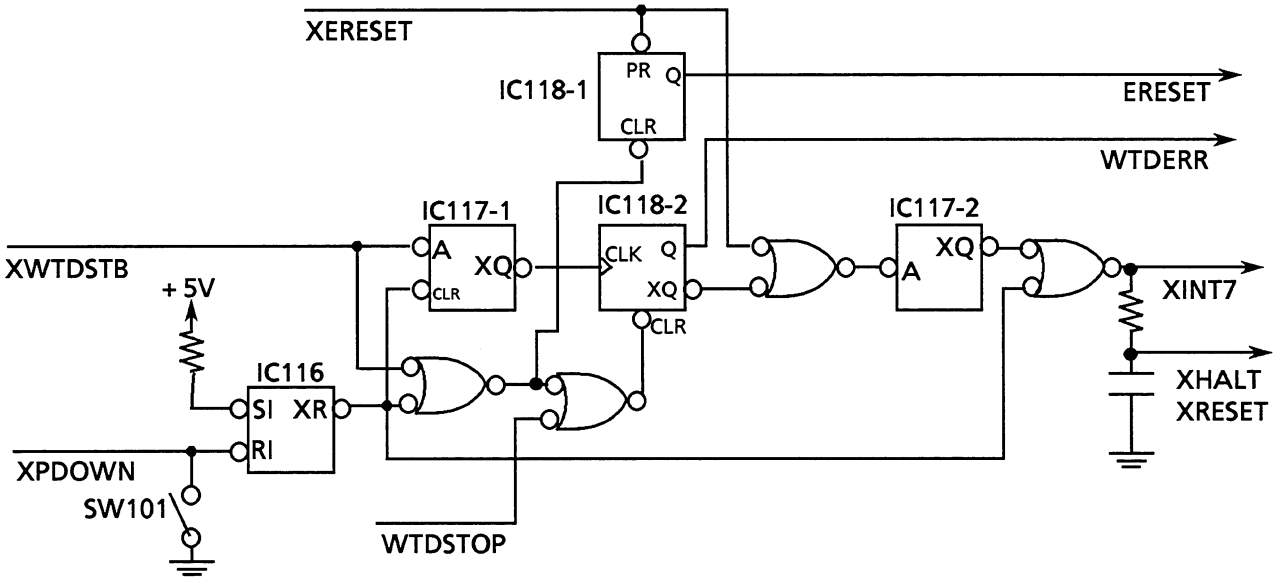


IC111 generates ROM selection signals XROM0SL-3SL.

IC113 generates RAM selection signals XRAM0SL-7SL.

IC114 generates the other I/O chip selection signals.

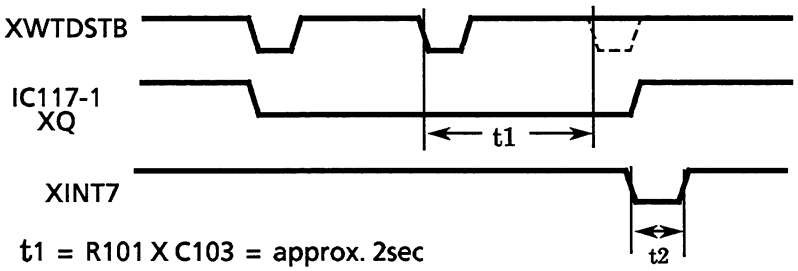
◆ **Reset/Watch Dog Timer/Power Down Detector Circuit**



● **Reset circuit**

When external reset signal XERESET is asserted by pressing the SELF CHECK key on the operation panel, the following signals are generated. The output (Q) on External Reset Status Flip Flop (IC118-1) is set to high, assertion of ERESET signal. Interrupt request signal to MPU (IC101), XINT7 is asserted for 50μsec. Reset signal to MPU (IC101), XRESET (XHALT) is asserted for 50μsec after 10μsec delay from XINT7 assertion.

● **Watch Dog Timer circuit**



t1 = R101 X C103 = approx. 2sec

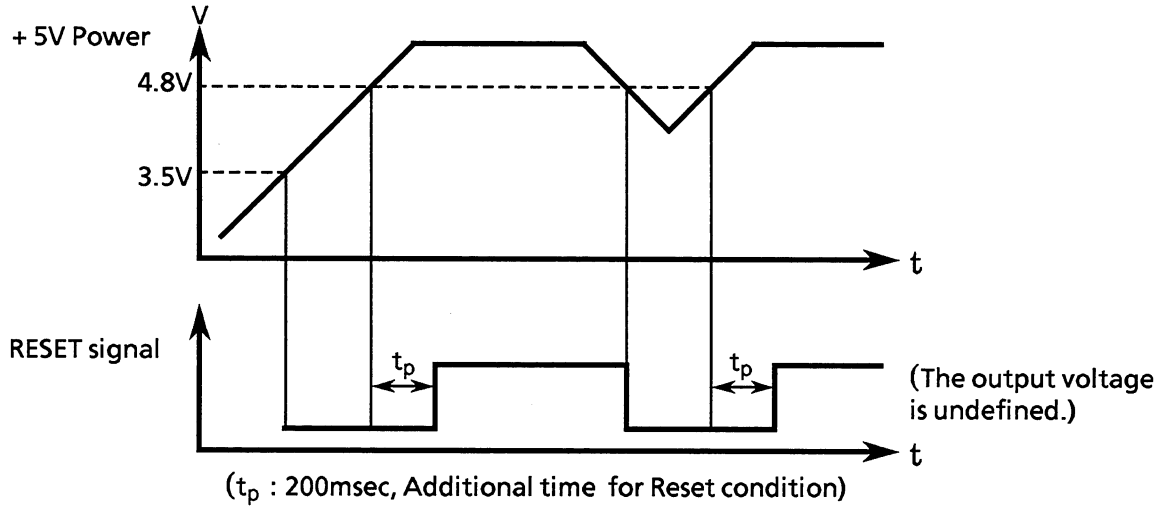
t2 = (RA109-5) X C104 = 47μsec

If MPU (IC101) runs away, this circuit resets the MPU as follows:
Under normal conditions, the output (XQ) on One-shot multi. (IC117-1) keeps low since IC117-1 receives the Watch Dog Strobe signal from MPU XWTDSTB within 2sec. However, under abnormal conditions, XQ on IC117-1 is changed to high since IC117-1 does not receive XWTDSTB signal. The following signals are generated.
The output (Q) on Watch Dog Timer Error Status F/F (IC118-2) is set to high (assertion of WTDERR signal).

XINT7 signal is asserted for 50 μsec.

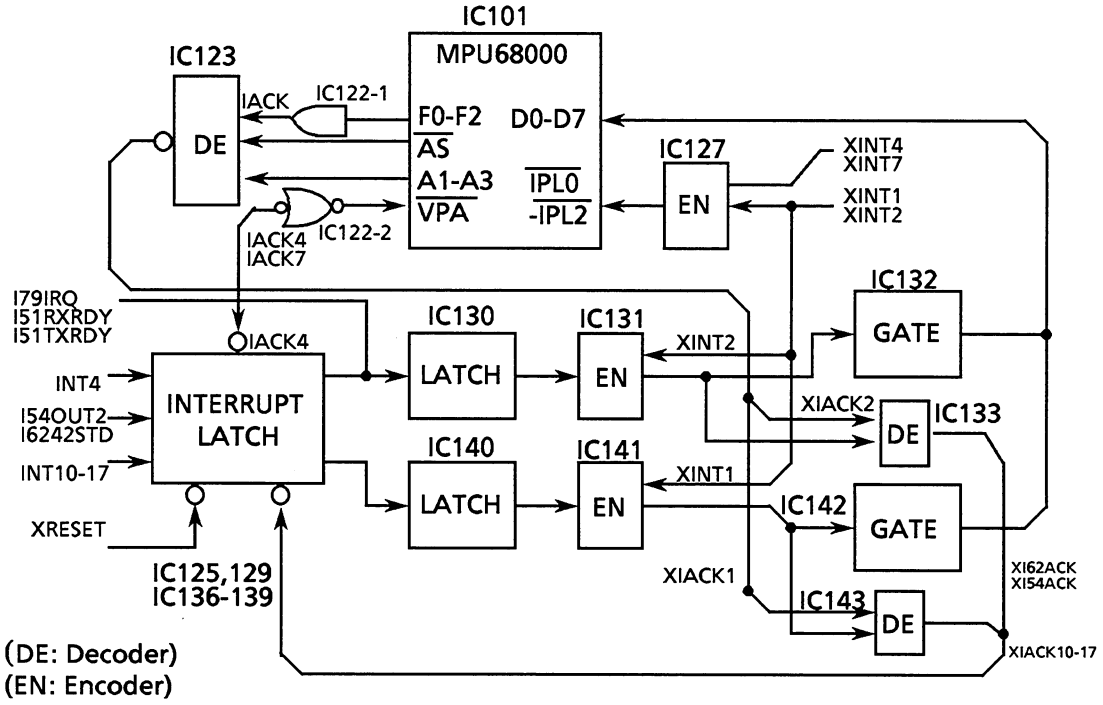
XRESET (XHALT) is asserted for 50 μsec after a 10 μsec delay from XINT7 assertion.

● **Power Down Detecting circuit**



If the +5 V power changes to 4.8 V or less in Power Down signal, the Power Down detector (IC116) generates reset signal (active-low) for IC118-1& 2 until 200msec passes after the +5 V power returns to 4.8V.
When the power is turned on, IC116 keeps reset signal until 200msec passes after the +5V power comes to 4.8V.
In the both cases, INT7 signal is asserted for 50μsec. and XRESET signal is also asserted for 50 μsec after 10 μsec delay from XINT7 assertion.
When the switch (SW101) is turned on, the reset input (RI) on IC116 is set to active-low.

◆ **Interrupt Control Circuit**



The interrupt request signals are divided into Auto-vectored interrupt and Vectored interrupt while being divided into seven levels according to the following table. Level-7 provides the highest priority.

INTERRUPT PRIORITY	VECTOR NUMBER	INTERUPT REQUEST SIGNAL	EXPLANATION	GENERATED IN
7	Auto	XPDOWN WTDERR XERESET	Power down Watch dog External reset	CPU board
6			Not used	
5			Not used	
4	Auto	INT40	CRTC Frame synchronizing (16msec)	CRTC board
3	Auto	INT30	For keypad's 72001	I/O board
2	4D 4C 4B 4A 49	16242STD 154OUT2 151TXRDY 151RXRDY 1791RQ	Real time (1sec) 71054 OUT2 (10msec) RS232CT_XRDY RS232CR_XRDY Key-in	CPU board
1	47 46 43 41	INT17 INT16 INT13 INT11	Interrupt for VD (72001) Interrupt from COM3 Interrupt from DPU Interrupt for WS recording	I/O board COM3 board DPU board COM3 board

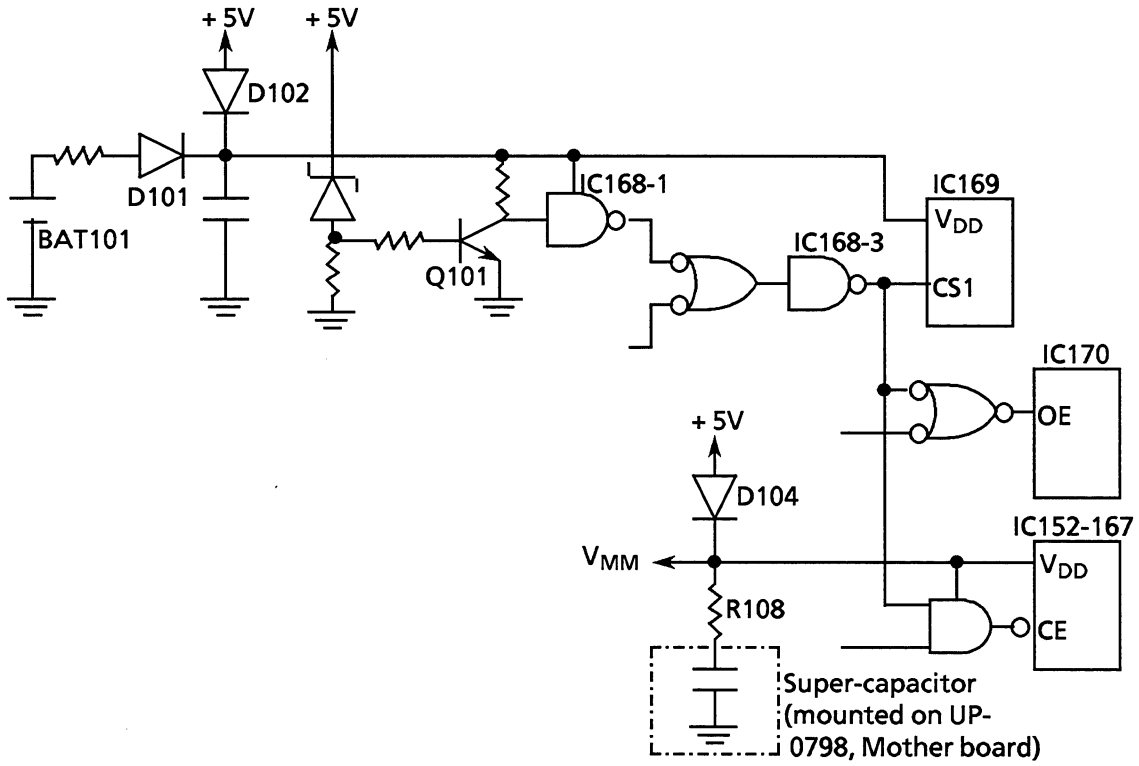
• Auto-vectored Interrupt

The Interrupt is processed by using a vector generated in the MPU. The interrupt request signal INT4 or INT7, is inputted to the Interrupt Control terminals, IPL0-2 on the MPU through Interrupt Latch (IC125) or Priority Encoder (IC127).
The IC125 latches an INT4 signal by triggering the positive-going edge of the signal and resets the output with XRESET or Interrupt Acknowledge signal IACK.
The IC127 generates the interrupt request to the IPL0-2 on the MPU whenever a higher interrupt priority level than before is inputted.
The IC122-1, IC123 and IC122-2 generate Interrupt Acknowledge signals, IACK and XIACK1/2 and Auto-vector recognition signal XVPA.

• Vectored Interrupt

The interrupt is processed by acquiring a vector number from the others by the MPU.
The interrupt level signal, XINT1 or XINT2, is inputted to IPL0-2 on the MPU through the Priority encoder (IC127). An interrupt request signal is changed to vector number signal (D0-7) through IC129/136-139, IC130/140, IC131/141 and Gate (IC132 /142).
The AND (IC122-1) and Decoder (IC123,133/143) generates interrupt acknowledge signals.
The Interrupt latch (IC129,136-139) resets the output by triggering the positive-going edge of the XRESET signal or each interrupt acknowledge signal.
The IC132/142 generates the vector number according to an interrupt request signal and then the vector number is acquired by the MPU.

◆ **Real Time Clock (RTC)/Battery/EEPROM**



• RTC

The real time clock IC (IC169) can be read or written by the MPU from second to year. IC169 provides four data lines, four address lines, three control lines and two lines of chip select signal for communication with the MPU.

IC169 provides real time setting or modification or readout function.

•Battery & Super-capacitor

The lithium battery (BAT101) provides a backup power function to prevent a data break in IC169 due to a power failure. The BAT101 supplies the IC169 through D101 with the +3 V power instead of the +5 V power when the +5 V power is lower than the battery power.

The super-capacitor (C101,102) mounted on the mother board (UP-0798) is always charged by the +5V power. The super-capacitor provides a backup function to prevent a data break in Static RAMs (IC152-167) when power fails. The super-capacitor supplies the Static RAMs through D104 with the charged power instead of the +5 V power when the +5 V power is lower than the charged power.

When the +5 V power starts to drop, the transistor (Q101) reaches cut-off condition and NAND IC (IC168-3) outputs low (0 V) through IC168-1, 2. Therefore, IC169, IC152-167 and IC170 work as follows:

IC169: The write mode is disabled since chip select terminal CS1 is set to Low, negation.

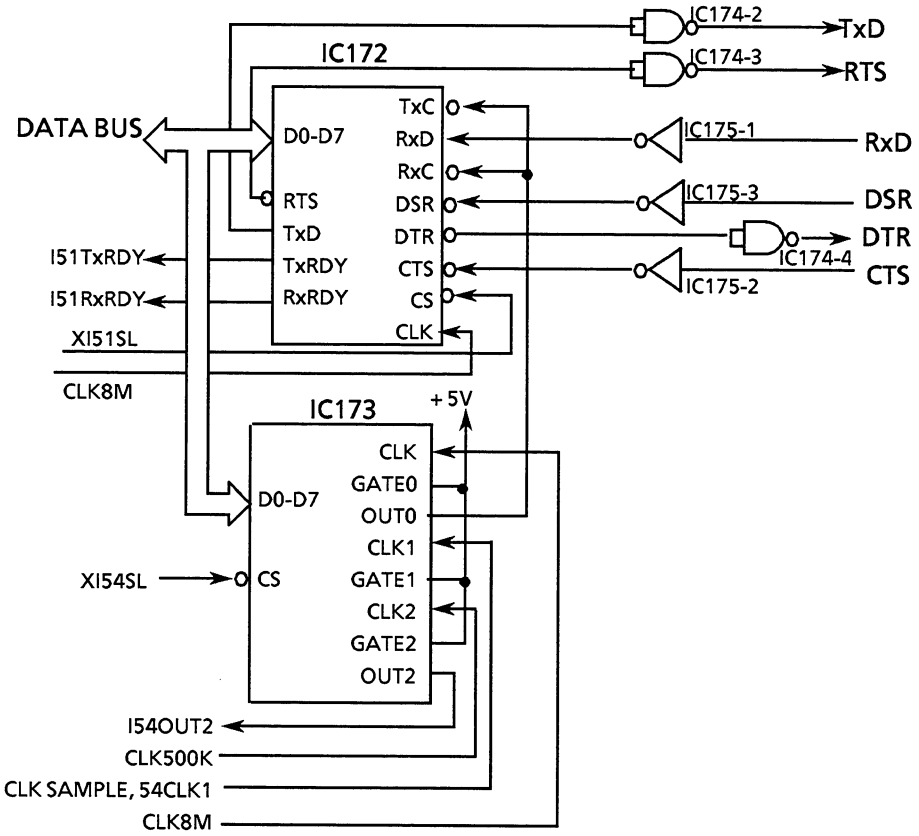
IC152-167: The write mode is disabled since chip enable terminal CE is set to High, negation.

IC170: When the power is within 3.0 V to 4.85 V, the write mode is disabled since output enable terminal OE is set to Low, assertion. When the power is between 0 to 3 V, the write mode is disabled owing to itself.

• EPROM

The Electrically Erasable Programmable ROM (IC170), HN58C65, provides 8kbyte memory capacity and 250nsec access time.

◆ RS232C Control Circuit



• Serial Inter-Face Controller (IC172), µPD71051C

The following items are controlled by software.

Baud rate:	1200, 2400 or 9600 bits/sec
Data length:	7 or 8 bits
Number of Stop bit:	1 or 2 bits
Operation mode:	Synchronizing or Asynchronizing mode
Parity bit:	Even or Odd

*** Transmitting operation**

When a parallel data is inputted at D0-7 on IC172, the data is converted to serial format data. The serial data is transmitted from Transmit Data terminal TxD. When the data transmission is completed, Transmitter Ready terminal TxRDY is set to High so as to interrupt the MPU operation and wait for the next parallel data.

*** Receive operation**

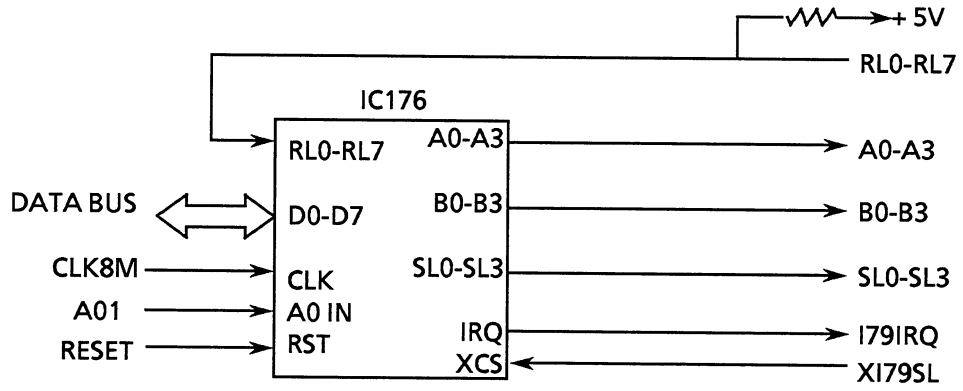
When a serial format data is received at Receive Data terminal RxD, the data is converted to parallel data for the MPU. When the data reception is completed, Receive Ready terminal RxRDY is set to High so as to interrupt MPU operation and request the reception of the parallel data to the MPU.

• Programmable Interval Timer (IC173), µPD71054C

The IC173 consists of three sets of 16-bit counters controlled by software. The IC173 is used for the following purpose.

- to control baud rate for RS232C communication
- to generate periodic interrupt to the MPU (10 msec interval)
- to synchronize data transfer timing with wave display timing on CRTC board (UP-0262) by counting 8 msec interval clock, I54CLK1.

◆ Key/Sound Control Circuit

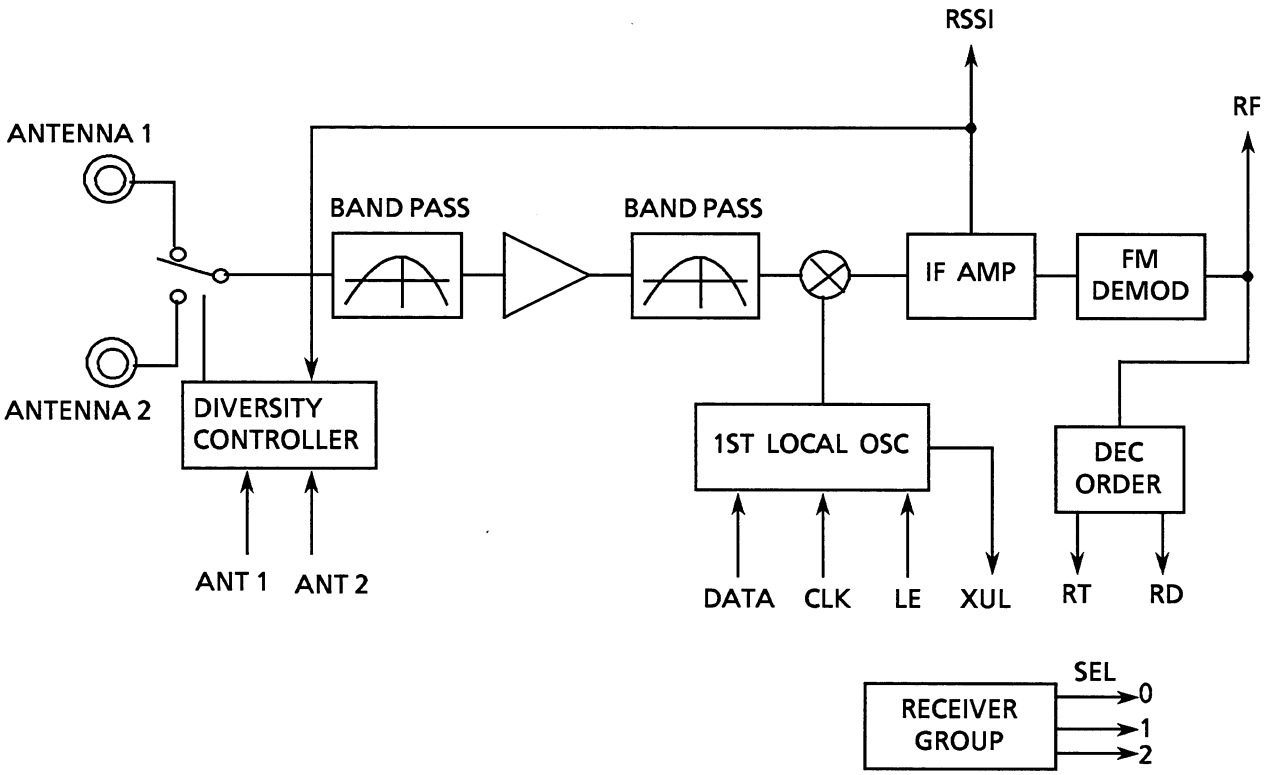


The keyboard /display controller (IC176) 8279 controls I/O board's sound generation circuit.

The operation mode is controlled by software. In BSM-8800, the operation mode is fixed as Decode, Scan and Sensor Matrix mode. SL0 ~ 3 signals are branched to latch B0 ~ 3 on the UP-0797 board.

3-2-7 Receiver, ZR-800P

Block Diagram



◆ Operation of Diversity Antenna

Two antennas (ANT1, ANT2) are provided.
Operation of diversity antenna is determined by 2 bit signals (ANT1, ANT2).
The relation between signal condition and operating status for ANT1/ANT2 are shown in below;

ANT1	ANT2	Operating status
L	L	Diversity
L	H	ANT2 only
H	L	ANT1 only
H	H	Unfixed

L: Poor (low) signal condition
H: Good (high) signal condition

◆ Output of SEL

The output of SEL is 3 bit output same as receiving group of transmitters.
Type of output is open collector type.

Group	Channel	SEL		
		0	1	2
1	7001 – 7201	H	L	L
2	7202 – 7387	L	H	L
3	7388 – 7574	H	H	L
4	7575 – 7785	L	L	H
5	7786 – 7997	H	L	H

◆ Setting of Receiving Channel

3 input lines (DATA, CLK, LE) are used for receiving channel setting.
Timing chart for DATA, CLK. LE are shown in next page.
The chart contains following two information.

(1) Reference clock setting information
The upper part of DATA,CLKA,LE is for setting reference clock of receiver's synthesizer to 12.5 kHz.
This information is always written for any channel.

(2) Receiving frequency setting information
The lower part of DATA,CLKA,LE is for receiving channel setting.
D15~D0 shown in the chart is 16 bit data (=65536 data) for determining receiving channel (I.E., receiving frequency).

Assuming that "f (MHz)" is a desired receiving frequency and "n" is a data for 16bit of D15~D0, following equation can be presented;

$$(f-45) \times \frac{1000}{12.5} = n$$

Example; When "f" = 457.5125 MHz, "n" is calculated as 33001.
33001 is converted to hexia code and expressed in 16bit data by D15~D0.

According to the above equation, rather wide range frequency can be set. However, only the channels on the table of above section 3.11.3 can be set actually for guaranteeing firm receiving condition.
When setting of receiving channel is not possible due to malfunction, "L0" is output on XUL.

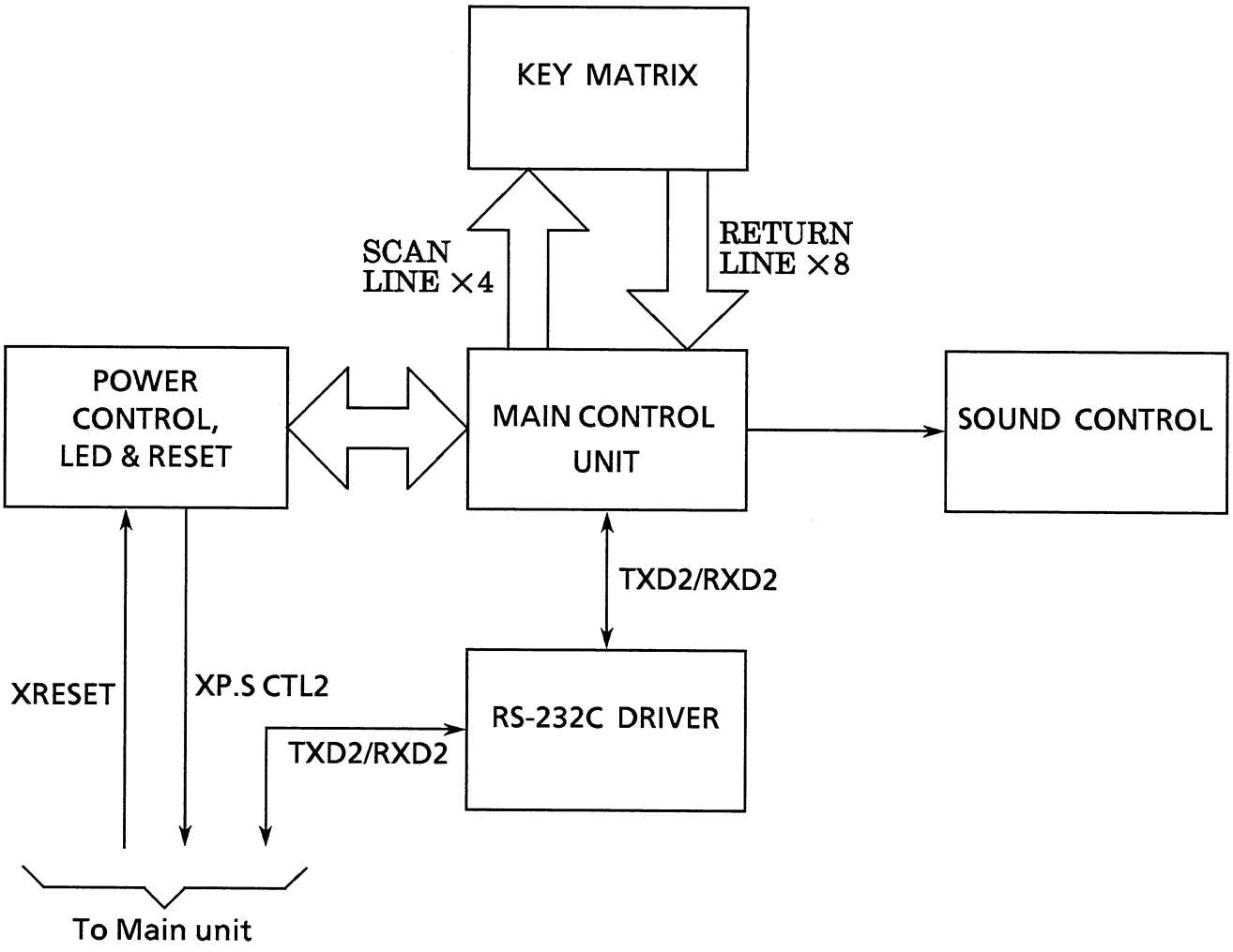
3-2-8 Transmitter

Internal operation of transmitter is not explained because specifications of transmitter can not be guaranteed if the repair is done locally.
Please see Section 6-6 for details.

3-3 Keypad, RY-881PA

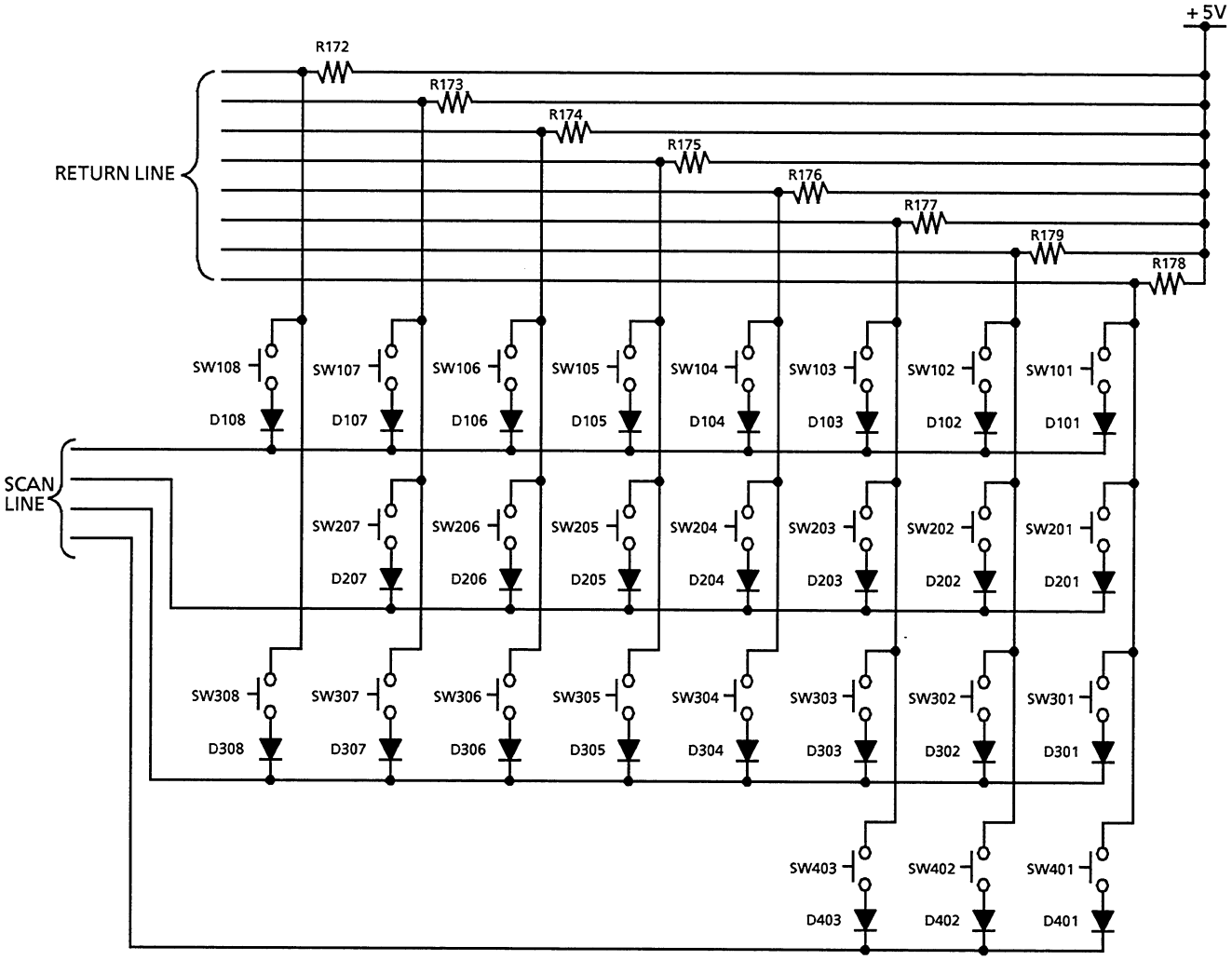
3-3-1 OPERATION RY Board, UR-3025

◆ **Keypad Operation Block Diagram**



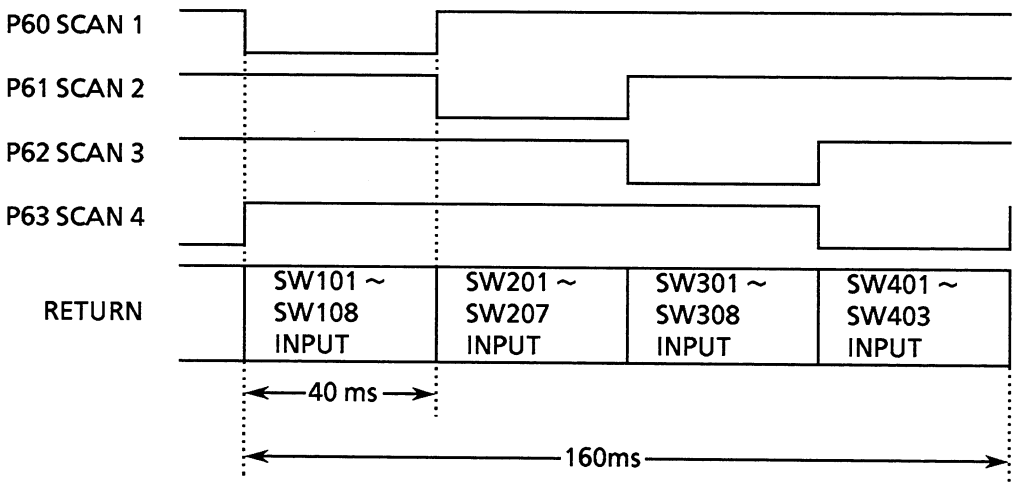
◆ Hardware Composition

The 26 keys on the keypad are arranged in matrix formation. The statuses of these keys are read by 8 return lines.



◆ Key Scanning Timing

The inputs of all the keys on the keypad are time-shared by the timings provided by SCAN1 - 4. These timings are shown below.



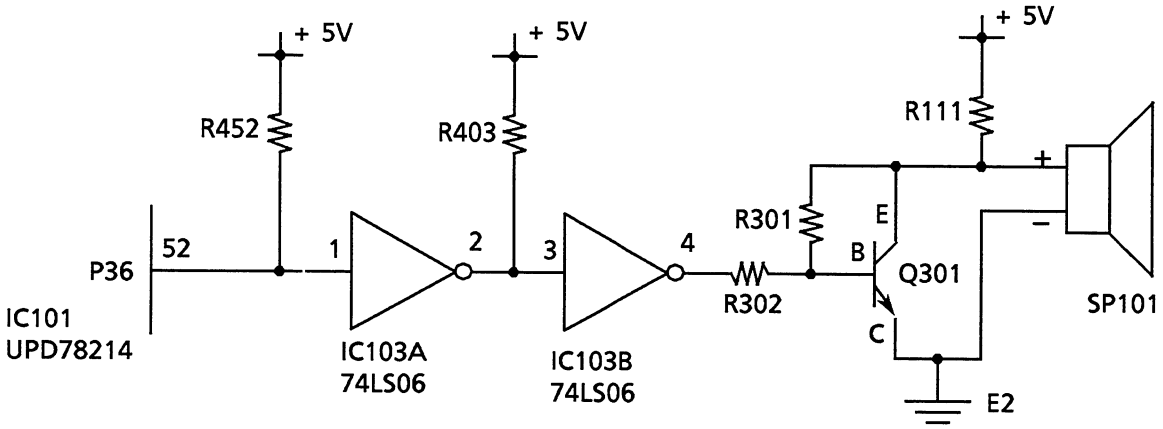
◆ Serial Communication

The serial communication with the bedside monitor main unit is controlled by the bus driver. The serial communication mainly consists of the key code data, and the control signals for the LED and key sound. The specification of this serial communication is :

*RS-232C Communication
* Baud Rate: 4800 or 9600 bps
* Character Length: 8 Bit
* Stop Bit Frequency: 1 Bit
* Operation Mode: ASYNCHRONOUS
* Parity: None

The baud rate depends on the setting of the dip switch SW501. The IC101 begins its transmission when the READY signal is asserted (HIGH).

◆ Sound Control



There are two types of key sound generated by the piezoelectric crystal speaker SP101. The type of key sound generated depends on the control data it received from the bedside monitor main unit via the IC102 and IC101. The frequency and the output time of the key sound type is shown in the table below.

Key sound type	Frequency	Output time
Key sound 1	3.0 kHz	50~60 msec
Key sound 2	2.0~1.4 kHz	3.0~3.6 msec

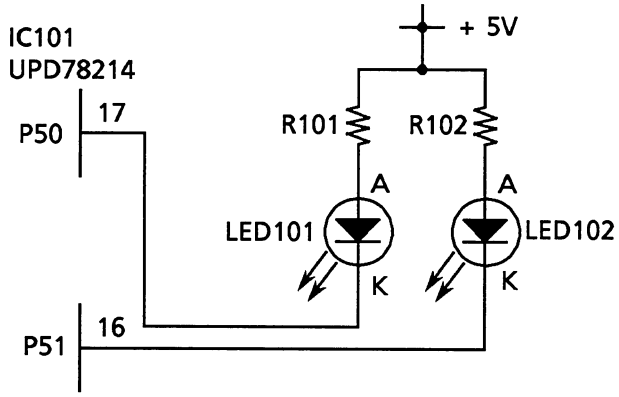
◆ Power Supply Control

The IC101 outputs the power supply control signal pulse, P.S CTL2, via its port P43 when one of the following conditions is observed.

* When the SW101 key is pressed for more than 120 msec.
* When the status of the M/S SEL signal is LOW.

◆ LED Control

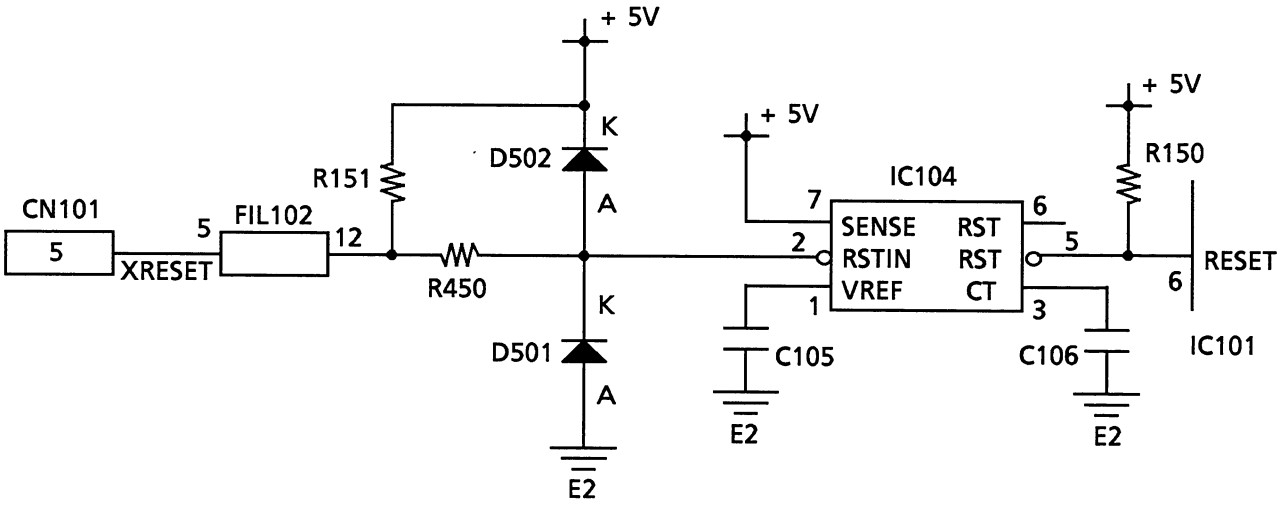
IC101 controls the LED101 and LED102 according to the instruction received from the bedside monitor main unit via IC102. The LED lights up when the connected port of IC101 is LOW and goes off when the port is HIGH.



◆ RESET

IC101 is reset under one of the following conditions :

* When it received the reset signal from pin No.5 of connector CN101 via IC104.
* When the +5 V voltage drops below 4.8 V.



3-4 Head Amplifiers

3-4-1 ECG Head Amp (AC-800P) Board, UP-0272

◆ General

The Hybrid IC (IC007) "ISOLATE" is mounted on not only this ECG head amplifier but also the others. In IC007, the F-CLK Generator supplies the power to the floating circuit, and the Switching Circuit SW1 demodulates the modulated signal from the floating circuit.

The Hybrid IC (IC009 ~ 012) "ECG BUF" buffers the ECG input signal and detects any electrode disconnection.

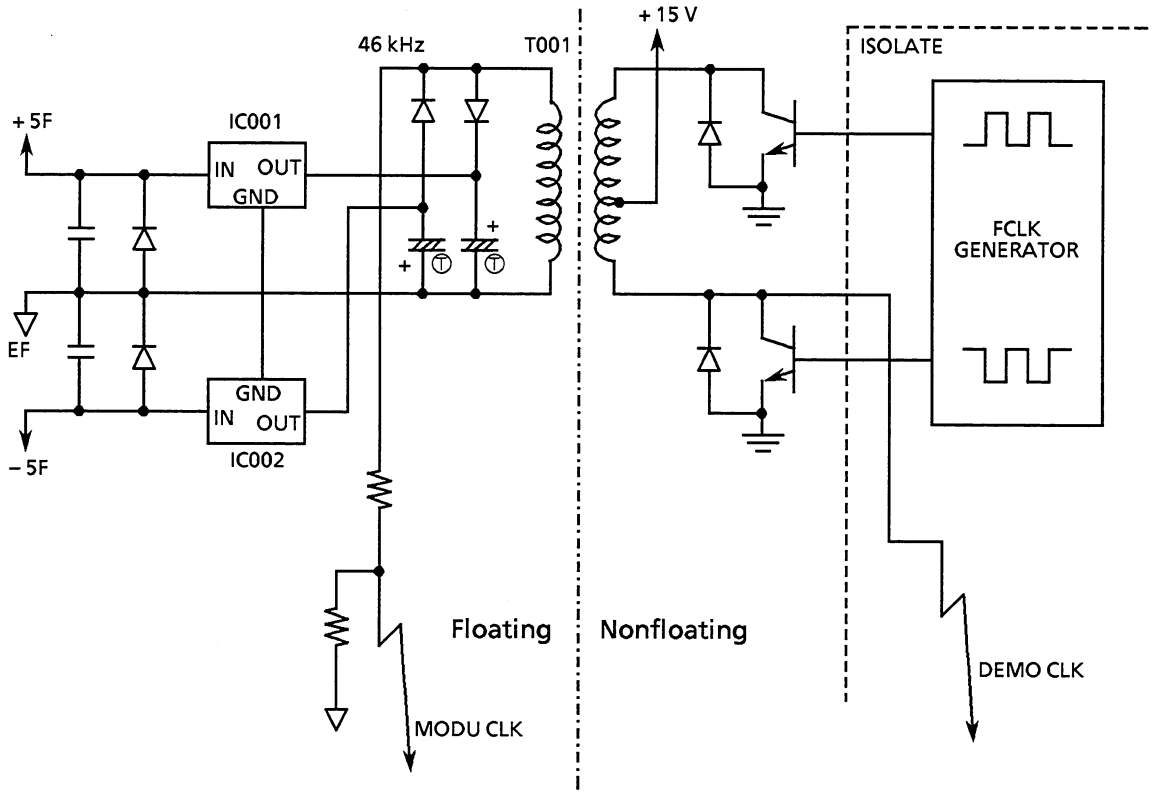
The Hybrid IC (IC008) "ECG SEL" selects an ECG lead. In IC008, the Switching Circuit SW3 modulates the selected ECG signal.

The S-P Converter (IC005) outputs the ECG lead selection signal to the Multiplexer (MPX1) in IC008 and the neutral electrode selection signal (for negative feed back) to the analog switch SW2(IC003B) or IC009 ~ 011.

The Counter (IC006) controls IC005 and the multiplexer (IC004) "MPX2" for time-sharing electrode disconnection signals.

◆ Floating Power Circuit

On the following circuit, the DC-DC converter circuit supplies the power(+5F,EF,−5F) to the floating circuit.
The MODU CLK signal is a 64kHz chopping signal to modulate the time-shared signal so as to transfer the time-shared signal from the floating circuit to the nonfloating circuit.
The DEMO CLK signal is a 64kHz chopping signal to demodulate the chopped signal.
The MODU CLK and DEMO CLK are synchronized with opposite polarity.



NOTE

The floating power circuit for the other Head Amp board is the same as the above circuit.

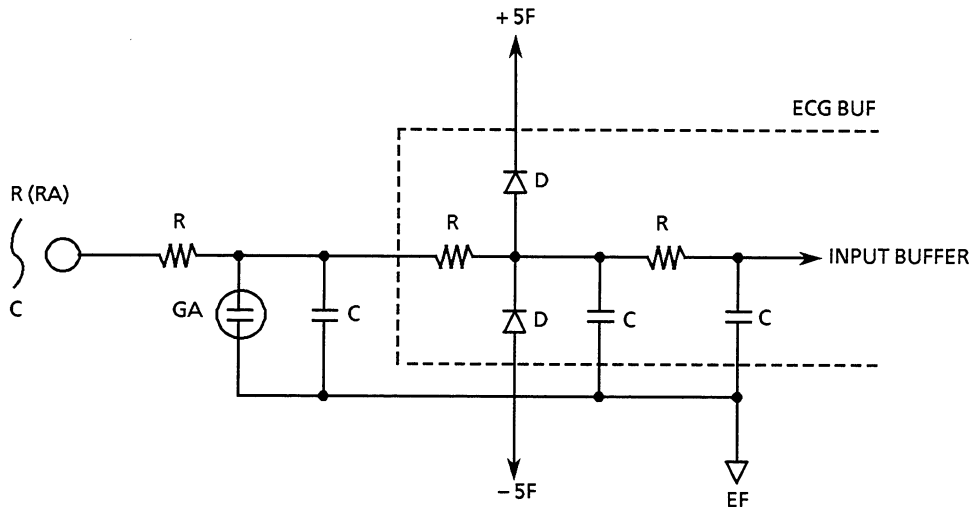
◆ Input Protection Circuit

• Electrosurgery Interference Elimination Filter

On the following circuit, the low-pass filter composed of the 3-stage R-C connection attenuates the high frequency component (100 dB down or more between 300kHz and 5MHz) of Electrosurgery Interference. The low-pass filter is intended to monitor ECG, to protect the input circuit and to reduce heat in case of simultaneous use of an electrosurgery unit.

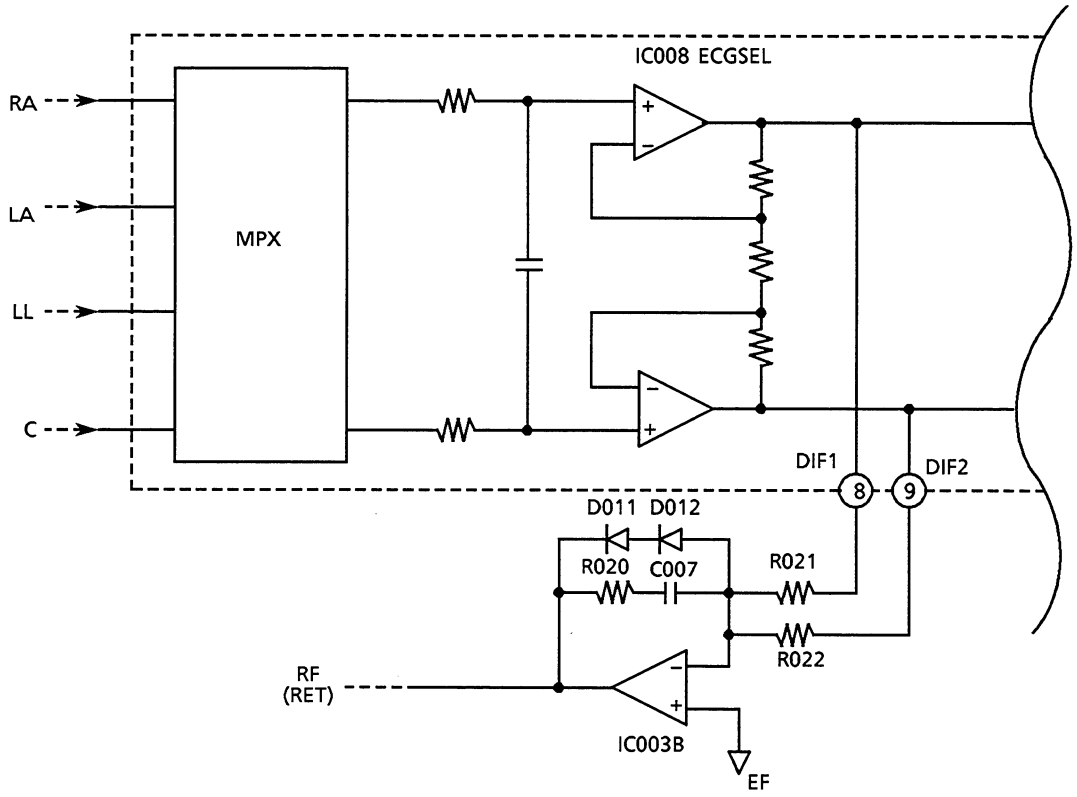
• Defibrillator Discharge Protector

On the following circuit, the series-connected resistors limit the discharge current to protect the input circuit against an excessive-voltage input signal, and the gas arrestor and diodes limit the discharge voltage when a discharge is started with a defibrillator.



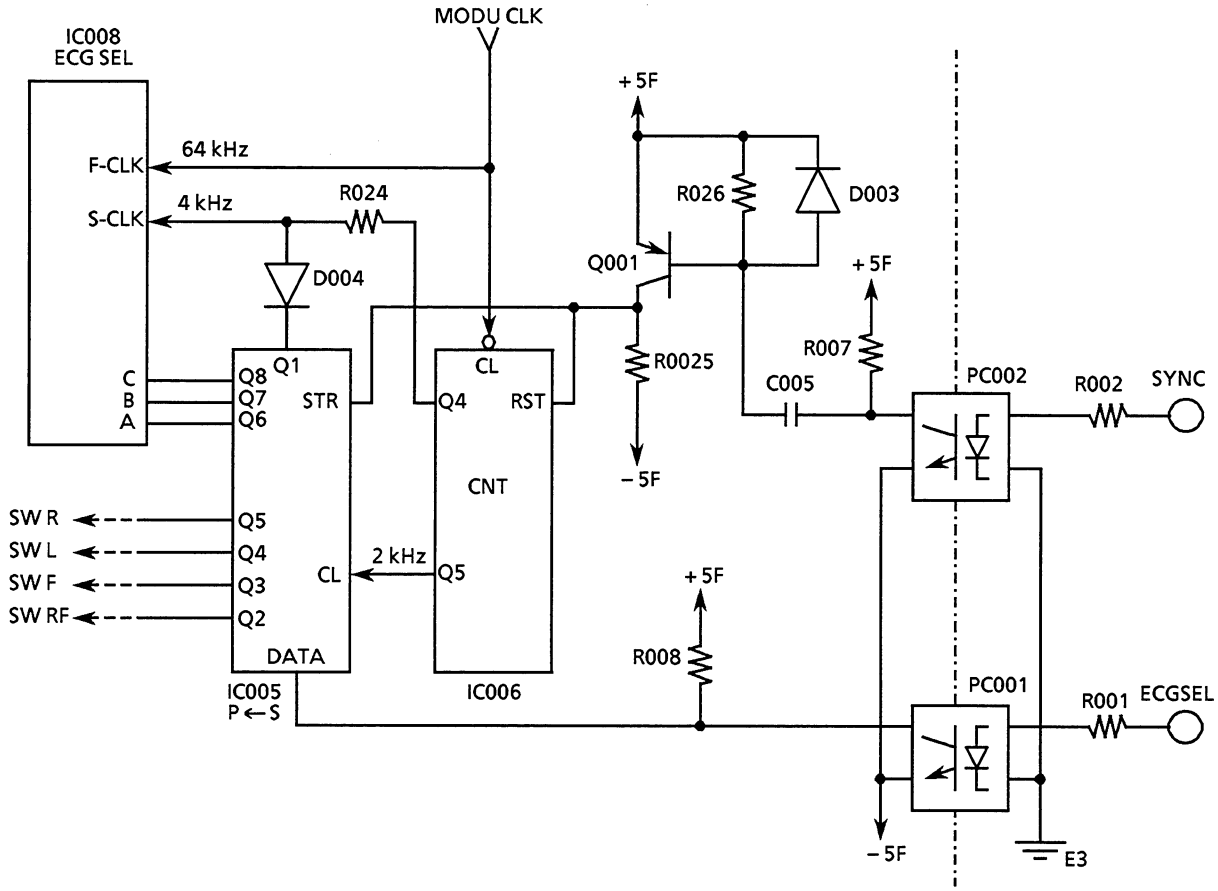
◆ Negative Feed-back Circuit

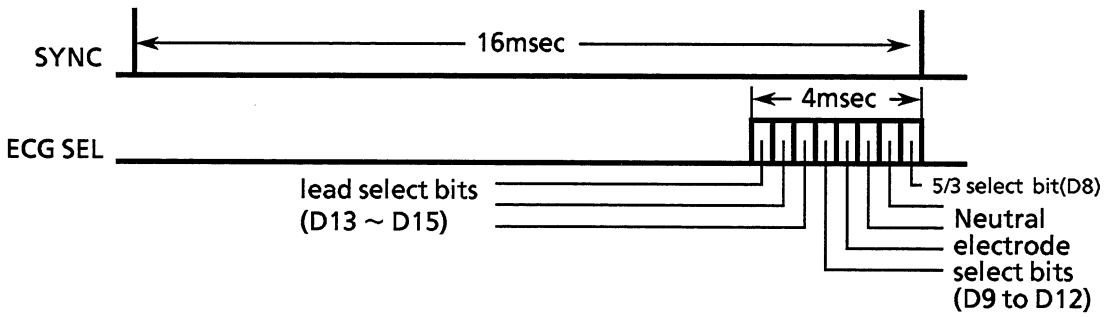
In theory, an in-phase artifact included in an ECG wave should not interfere with the ECG wave signal since the ECG signal is pre-amplified with the differential amplifier. However, in actuality, an ECG signal with an in-phase artifact appears between DIF1 and DIF2 since the in-phase signal changes to a signal with some phase difference due to the impedance unbalance between electrodes. To overcome this, the output signals from the differential amplifier are branched to the negative feed-back circuit for neutral electrode (DIF1 & DIF2). The negative feed-back circuit attenuates the in-phase component based on the Floating Ground (EF) and obtains a high Common Mode Rejection Ratio (CMRR).



◆ ECG Lead Selecting Circuit

The following ECG SEL signal through the photocoupler (PC001) selects an ECG lead and a neutral electrode line for negative feed-back from input signal lines. The ECG SEL signal is converted with the S-P converter (IC005) to parallel signals. SW R, SW L, SW F, or SW RF of the parallel signals controls each ECG BUF (IC009 ~ 012) to select a neutral electrode from the four electrodes.





Each bit combination of an ECG SEL signal and an ECG lead is related as follows:

[3 Electrode leads]

Lead	Electrodes				ECG SEL bits
	ECG1			ECG2	D15 D14 D13 D12 D11 D10 D9 D8
	+	N	−	(= ECG1)	
I	L	F	R	(The same as the left)	1 1 1 1 1 0 1 1
II	F	L	R		1 1 0 1 0 1 1 1
III	F	R	L		1 0 1 0 1 1 1 1

[5 Electrode leads]

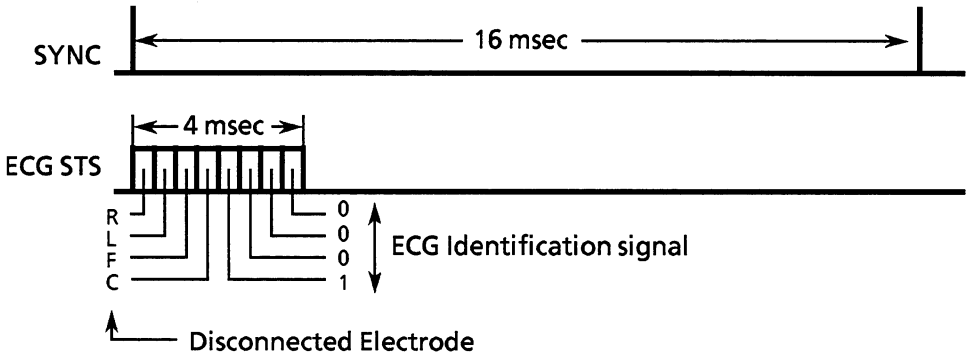
Lead	Electrodes						ECG SEL bits
	ECG1			ECG2(Lead-II)			D15 D14 D13 D12 D11 D10 D9 D8
	+	N	−	+	N	−	
I	L	RF	R	F	RF	R	1 1 1 1 1 1 0 0
II	F	↓	R	↓	↓	↓	1 1 0 1 1 1 0 0
III	F	↓	L	↓	↓	↓	1 0 1 1 1 1 0 0
aVR	R	↓	(L + F)/2	↓	↓	↓	1 0 0 1 1 1 0 0
aVL	L	↓	(R + F)/2	↓	↓	↓	0 1 1 1 1 1 0 0
aVF	F	↓	(R + L)/2	↓	↓	↓	0 1 0 1 1 1 0 0
V	C	↓	(R + L + F)/2	↓	↓	↓	0 0 1 1 1 1 0 0
MCL	C	↓	L	↓	↓	↓	0 0 0 1 1 1 0 0

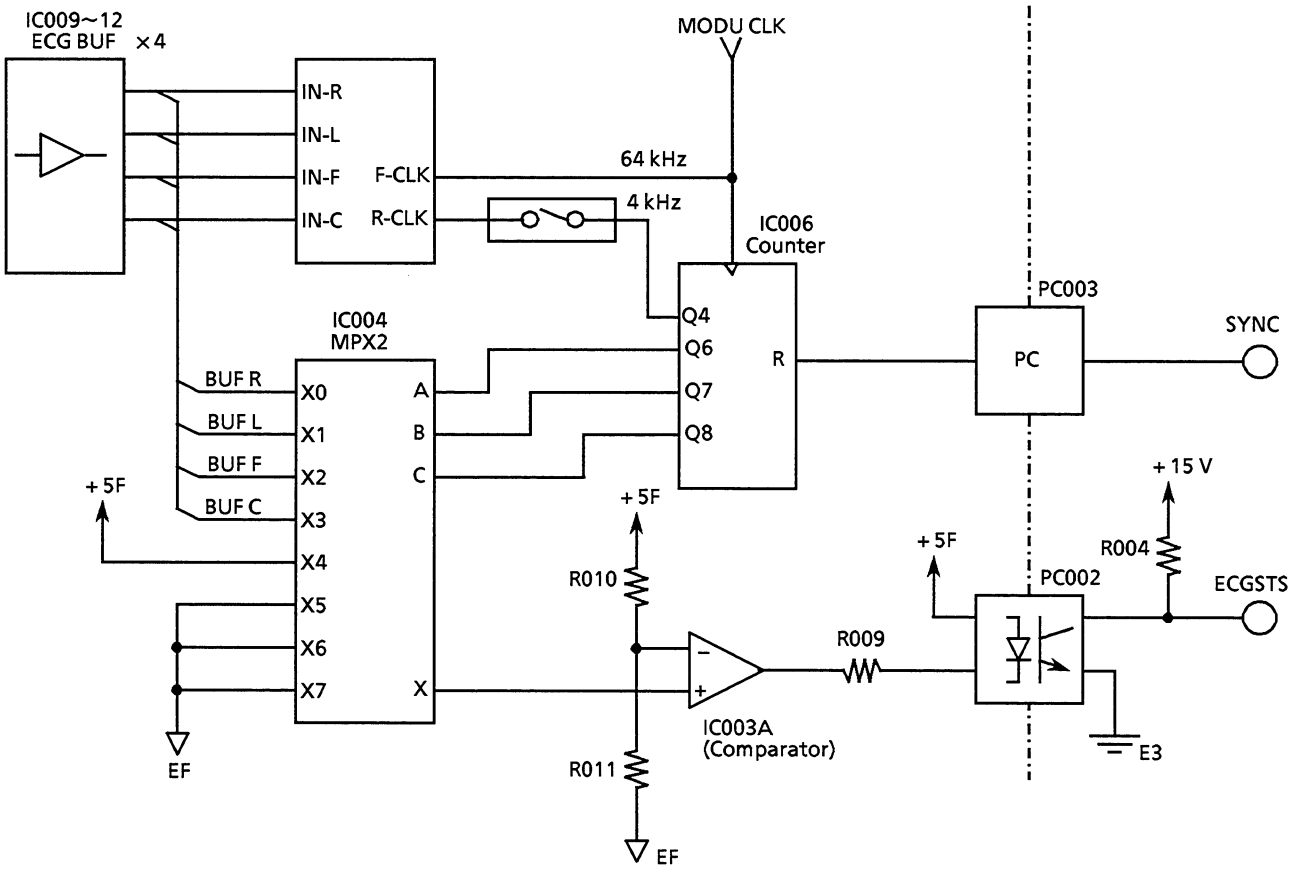
◆ Electrode Disconnection Detecting Circuit

The loop circuit between a patient and the input circuit is closed through a negative feed-back circuit when the electrode leads are connected to the patient. However, the loop circuit is opened and the related ECG BUF output (BUF R, BUF L, BUF F or BUF C) is drawn to the floating power voltage when an electrode or a lead wire is disconnected.

The Multiplexer (IC004) "MPX2" time-shares the BUF R, L, F or C signal to be a serial format signal (ECG STS signal).

The comparator (IC003A) compares the time-shared signal with the reference voltage and outputs an ECG STS signal to the nonfloating circuit.





A disconnected electrode and the bits combination of the ECG STS signal are related as follows:

[3 Electrode leads]

Lead	Neutral Electrode	Electrode Condition	ECG STS bits			
			D7	D6	D5	D4
			R	L	F	C
I	F	Normal	0	0	0	1
		R: disconnect	1	0	0	1
		L: disconnect	0	1	0	1
		F: disconnect	1	1	0	1
		Open	1	1	0	1
II	L	Normal	0	0	0	1
		R: disconnect	1	0	0	1
		L: disconnect	1	0	1	1
		F: disconnect	0	0	1	1
		Open	1	0	1	1
III	R	Normal	0	0	0	1
		R: disconnect	0	1	1	1
		L: disconnect	0	1	0	1
		F: disconnect	0	0	1	1
		Open	0	1	1	1

[5 Electrode leads]

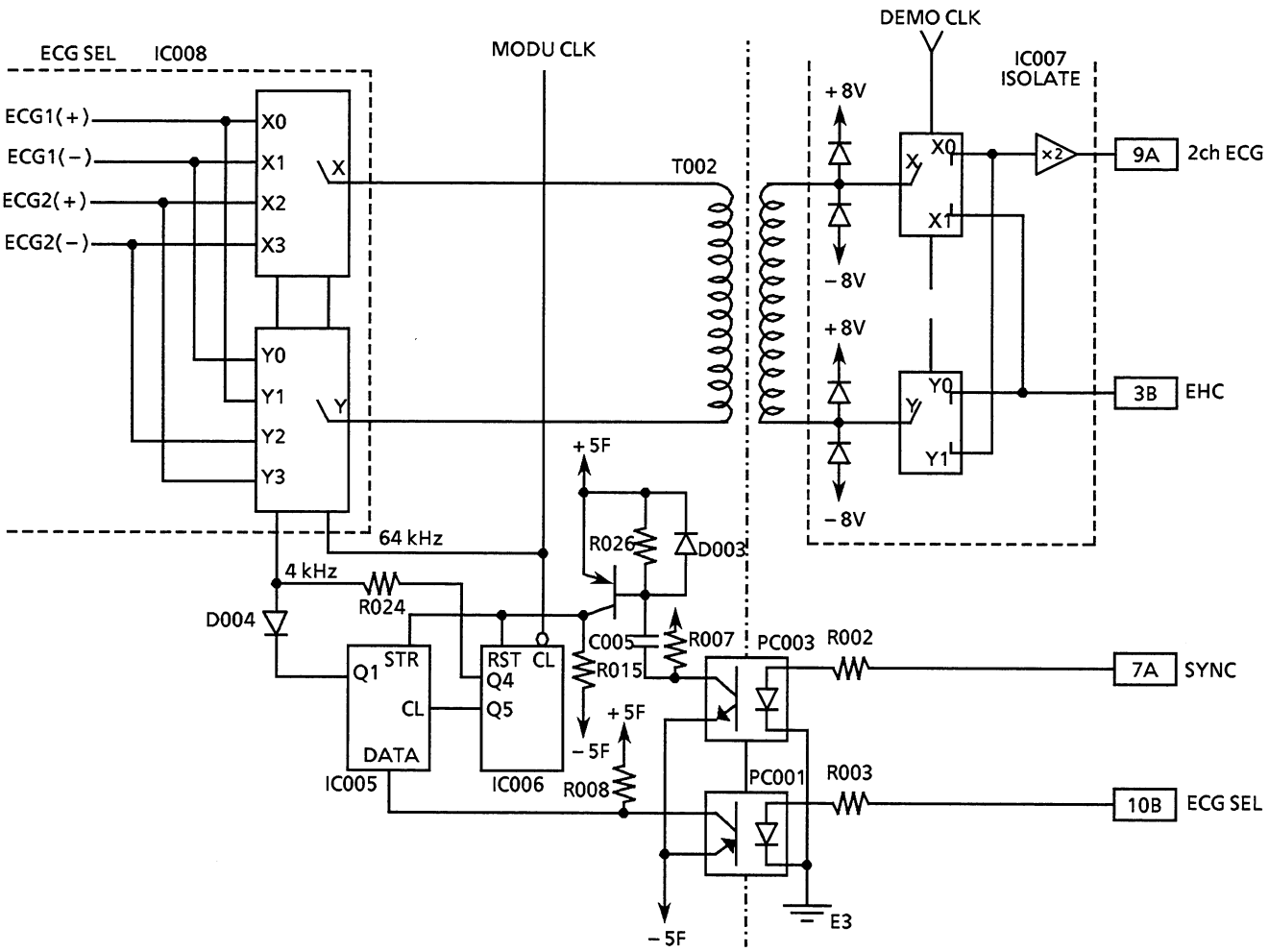
Lead	Neutral Electrode	Electrode Condition	ECG STS bits			
			D7	D6	D5	D4
			R	L	F	C
All	RF	Normal	0	0	0	0
		R: disconnect	1	0	0	0
		L: disconnect	0	1	0	0
		F: disconnect	0	0	1	0
		C: disconnect	0	0	0	1
		RF:disconnect	1	1	1	1
		Open	1	1	1	1

◆ ECG signal Modulation/Demodulation Circuit

When the 3-electrode lead mode is selected in the main unit, only ECG1 is modulated with the MODU CLK signal on the floating circuit and demodulated with the DEMO CLK signal on the nonfloating circuit since IC005-Q1 is set to low level.
When the 5-electrode lead mode is selected in the main unit, ECG1 and ECG2 are alternately time-shared every 125μsec with the 4kHz clock from IC006-Q4 and modulated with MODU CLK since IC005-Q1 is set to high level.
The time-shared signal 2ch ECG is divided into two signals, ECG1 and ECG2 on UP-0270.

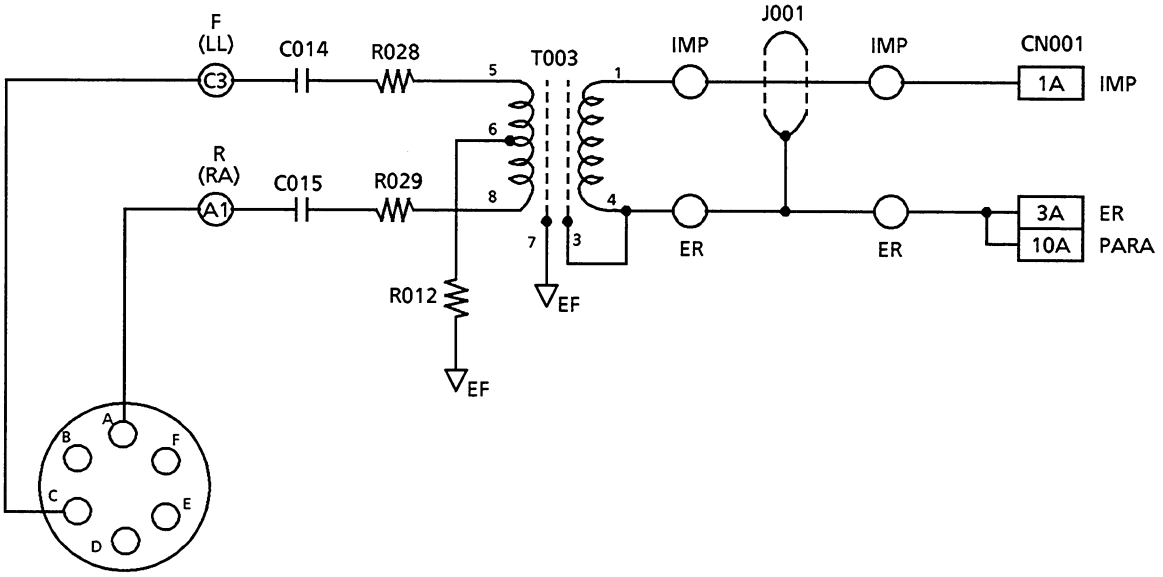
NOTE

Modulation with MODU CLK and Demodulation with the DEMO CLK circuit, which are provided on the other Head Amp board, are the same as the above circuit.



◆ Respiration Signal Detecting Circuit

Respiration waveform is detected by means of the impedance method.
An impedance between two electrodes, R(RA) and F(LL), is excited with an 80kHz (respiration) carrier signal (10Vp-p) from UP-0271. The impedance is changed by respiration, inspiration and expiration.



3-4-2 PRESS Head Amp (AP-800PA) Board, UP-0369

◆ General

The exciter (IC006) generates an excitation voltage to drive the Blood Pressure Transducer (BP1,BP2).

The blood pressure signals, P1 and P2, from the BP transducer are time-shared with the analog switch (IC003A) through a 200-times preamplifier (P1: IC007/008/011B, P2: IC009/010/012B) and 33Hz low-pass filter (P1: IC011A, P2: IC012A).

The analog switch (IC003A) is controlled with a 125Hz clock from the counter (IC004).

The comparator (IC013A/B) selects one of four states of the PARA signal according to the connection of BP1 or BP2.

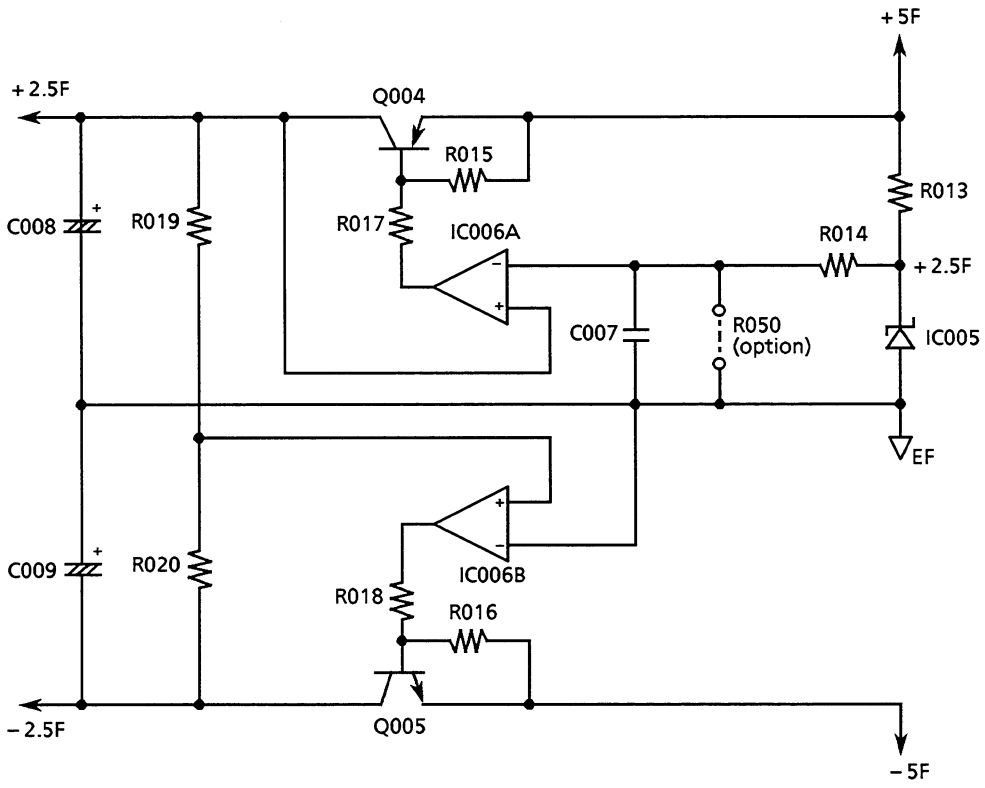
◆ Exciter Circuit

This circuit generates a ±2.5 V excitation voltage to excite the blood pressure transducers.

The ±2.5V excitation voltage is stabilized through the reference voltage generator (IC005).

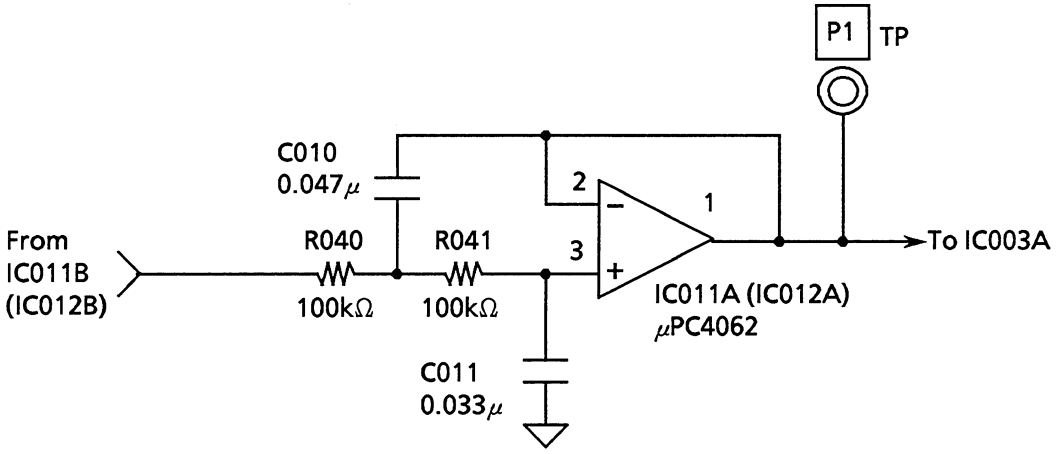
The excitation voltage can drive two transducers with an exciting load up to 200 Ω.

The excitation voltage can be attenuated by mounting a resistor on "R050" location and can be set to the proper voltage for a BP transducer by combining the resistor (R050) with 10 kΩ (R014).



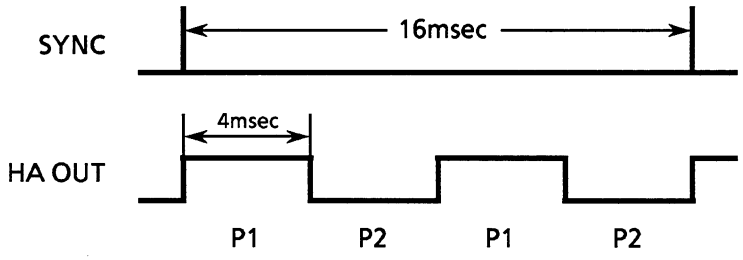
◆ 33Hz Low-pass Filter Circuit

The following 2-stage low-pass filter is provided through the preamplifier to pass the frequency component of the blood pressure waveform only.
In the following filter, the cut-off frequency is 33Hz. However, the total cut-off frequency is 20Hz or 10Hz (selectable on the System Setup display) by passing the software-filter in the Main unit.



[Output timing]

The P1 and P2 signals are alternately outputted from HA OUT every 4msec synchronizing with the SYNC signal as follows:



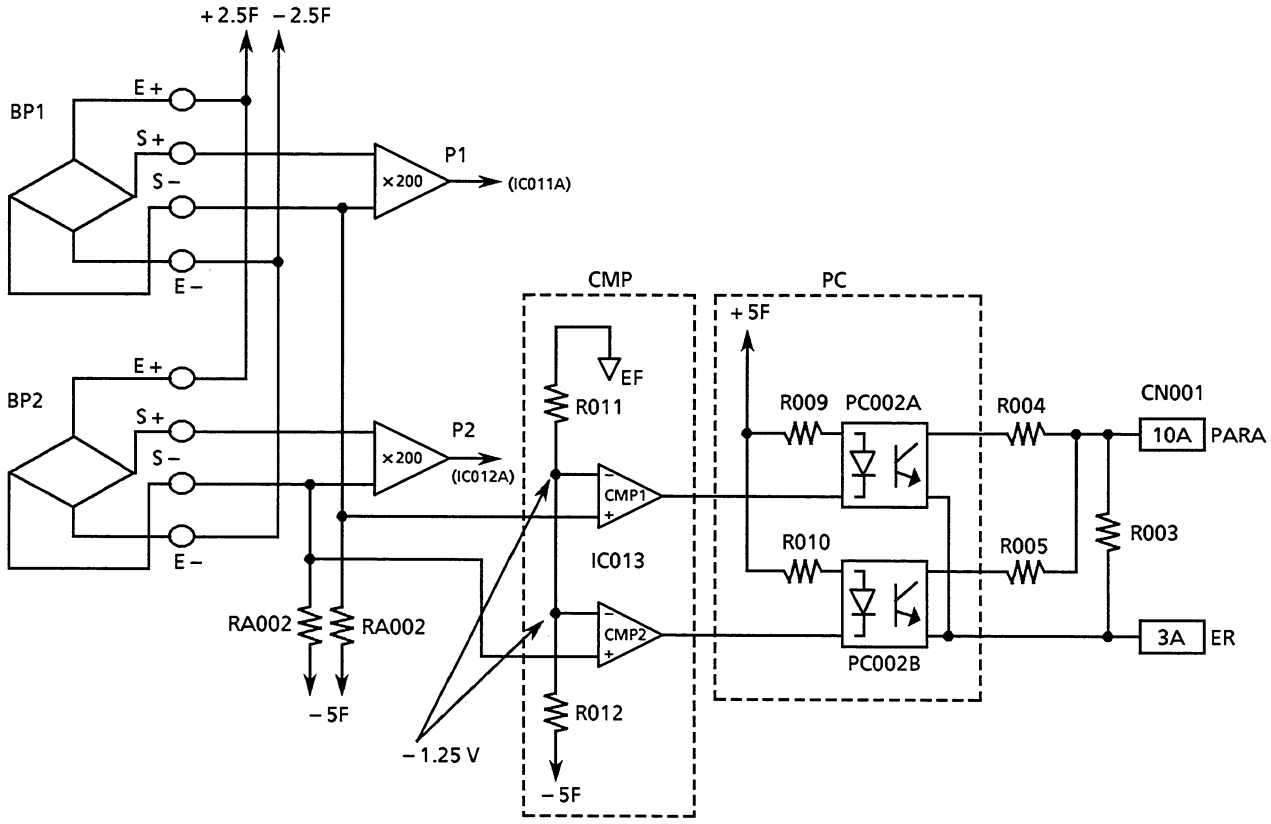
◆ PARA signal Generating Circuit

The following voltages for the PARA signal are generated according to the connection of Blood Pressure Transducers BP1 or BP2.

Connected BP Transducer	PARA Voltage
BP1 and BP2	1.5V ± 25mV
BP1	1.35V ± 25mV
BP2	1.2V ± 20mV
No connection	1.1V ± 20mV

When a transducer is not connected, the output from the comparator (IC013A/B) is low level since the positive terminal on IC013A/B is biased to 5V. The photocoupler (PC002A/B) is set to "ON". The generating voltage for the PARA signal is 1.1V since +5V REF is divided between the pull-up resistor (10kΩ) for 5V REF and resistors (R003 ~ 005) in parallel.

When one or two transducers are connected, the output from IC013A/B is high level since the positive terminal on IC013A/B is approx. 0V. The PC002A/B is set to "OFF". The generating voltage for the PARA signal is different from 1.1V since resistors in parallel decrease according to the BP1 or BP2 connection.



3-4-3 CO Head Amp (AH-800PA) Board, UP-0318

◆ General

The 16Hz Low-pass filter (R015&C009, R023&C011) eliminates only high frequency component, such as electrosurgery interference.

The Multiplexer (IC009) time-shares a Reference signal (REF), Injection fluid Temperature signal (Ti), Blood Temperature signal (Tb) and Blood Temperature variation signal (ΔTb).

The Auto-shift circuit (IC012) shifts the DC voltage of the baseline so as not to saturate the ΔTb signal due to 1000-times amplification.

The S-P converter (IC011) controls IC012.

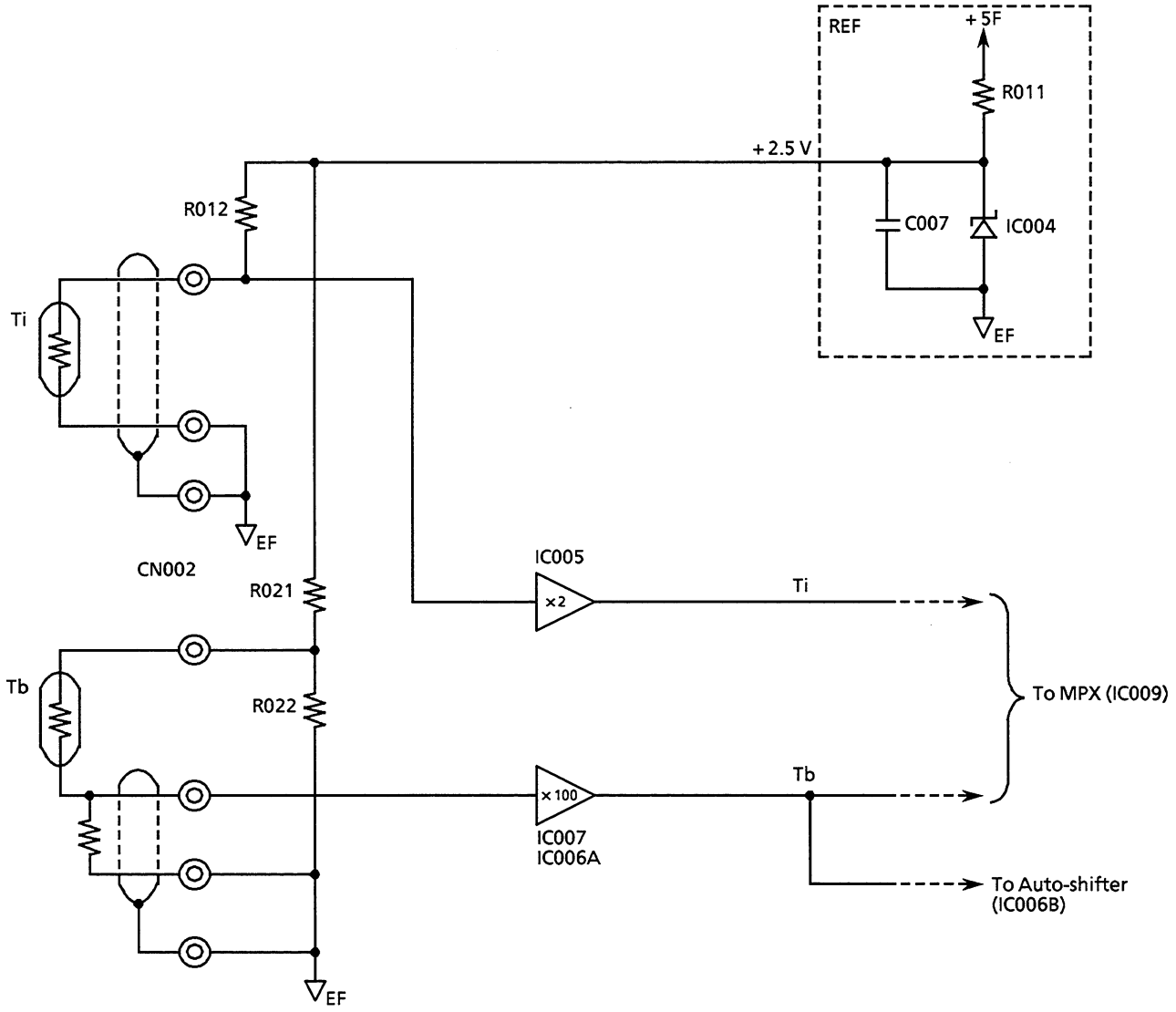
The Counter (IC010) generates a 250Hz clock for IC012 and control signals for IC009.

◆ Resistance-Voltage (R-V) Converter Circuit

The following IC004 generates a +2.5 V reference voltage.

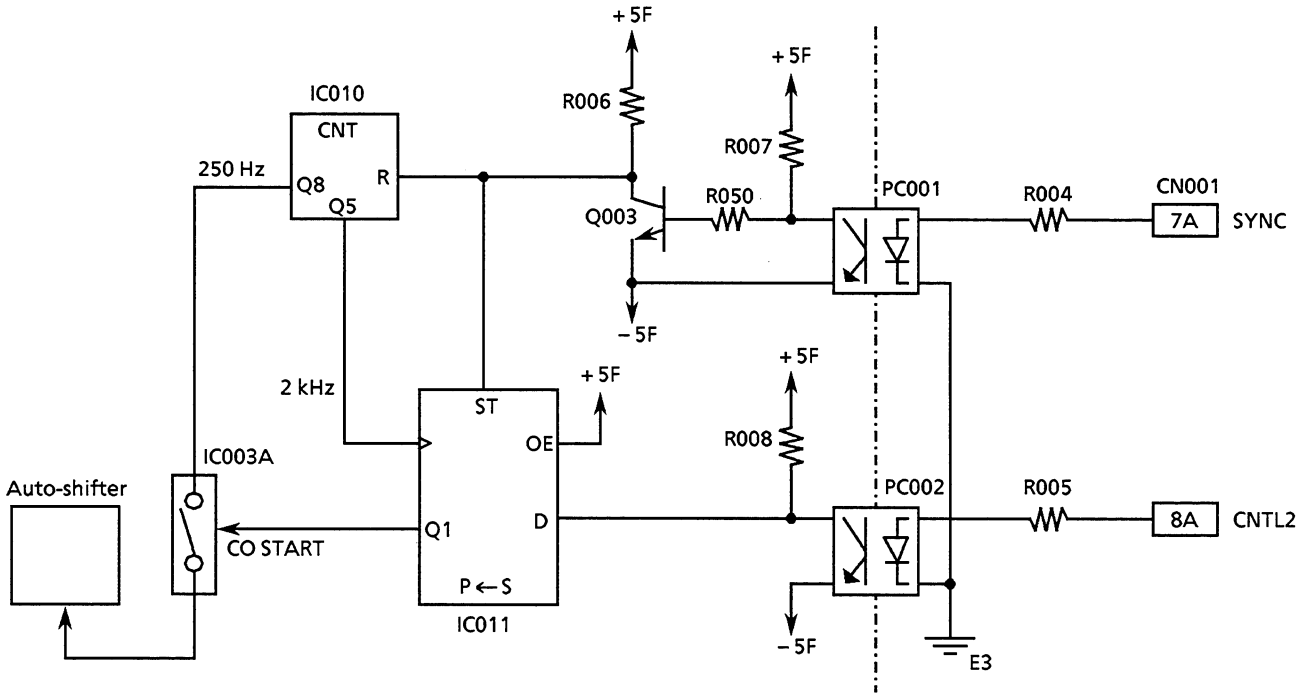
By dividing the reference voltage between R012 and Ti-thermistor resistance, the Ti-voltage is obtained according to the Ti-thermistor resistance variation caused by the injection fluid temperature.

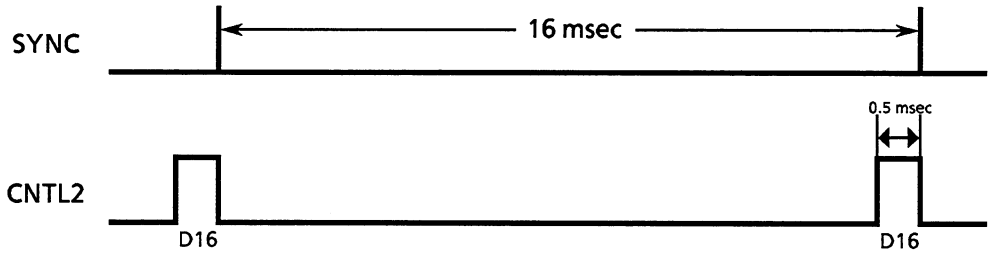
By dividing the reference voltage between R021 and R022 and shunting the Tb-catheter thermistor resistance to the R022, the Tb-voltage is obtained according to the Tb-resistance variation caused by the fluid injection.



◆ S-P Converter Circuit

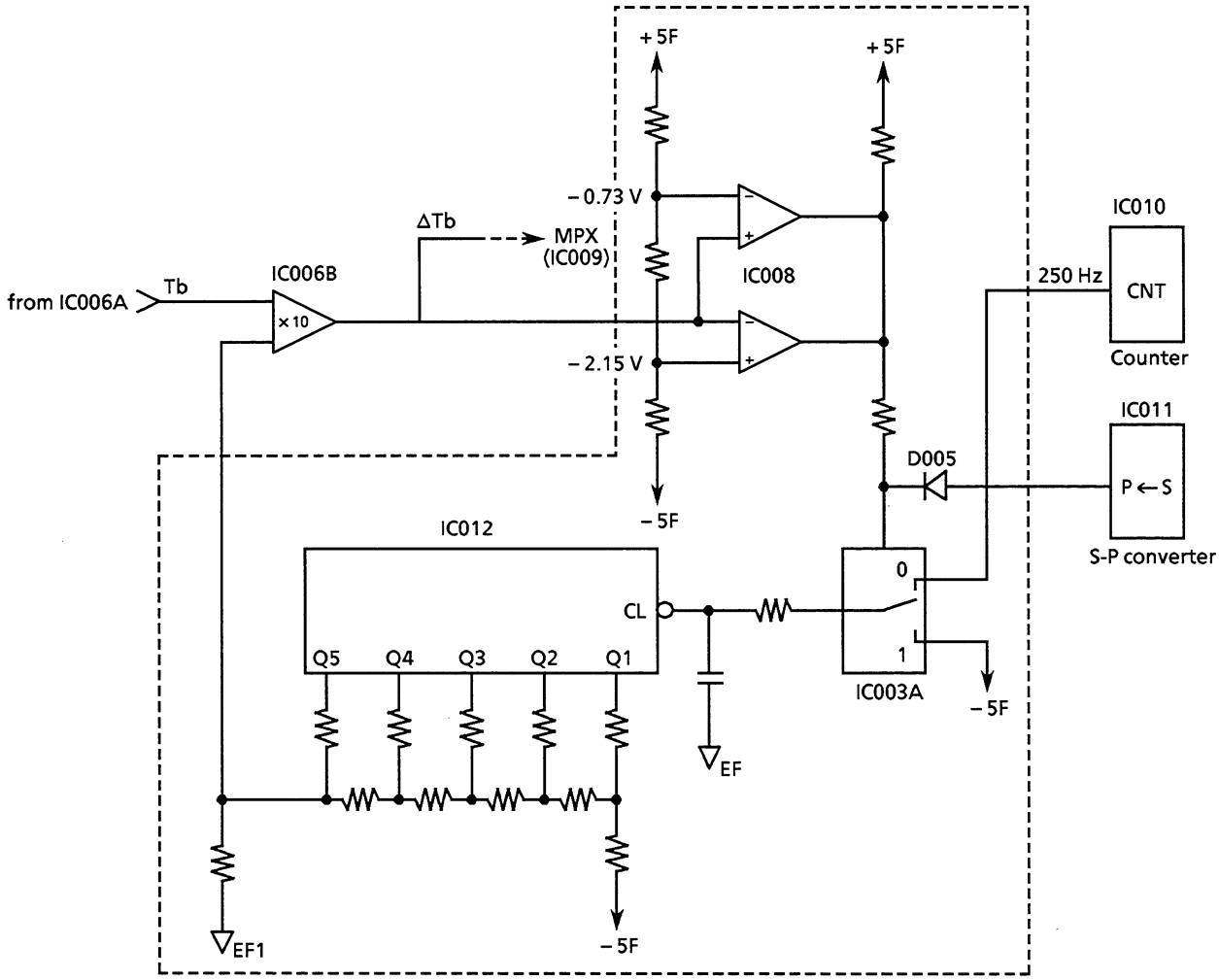
The "ST" terminal of the S-P converter (IC011) is set to High level when the SYNC signal varies from Low level to High level. Then analog switch (IC003A) is connected to 250 Hz clock to work the Auto-shifter (IC012) with Low signal from Q1 on IC011 after D16 on serial format signal CNTL2 is set to High level (CO Start signal) as follows:





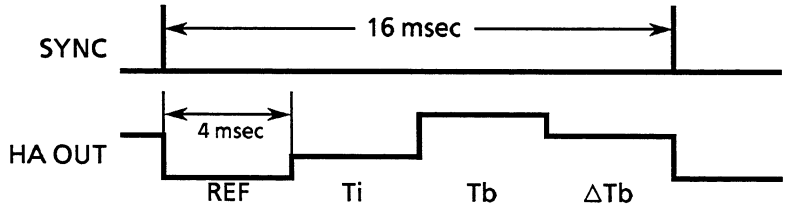
◆ Auto-shift Circuit

Blood Temperature Variation ΔTb needs more amplification than Ti or Tb since the ΔTb signal is a smaller signal variation than Ti or Tb.
The following auto-shift circuit shifts the ΔTb output voltage so as not to saturate the ΔTb output.
When the S-P converter (IC011) outputs a Low level signal to the analog switch (IC003A) after the CO start signal on serial format signal CNTL2 is inputted to IC011, IC003A connects the Counter (IC010) with the Auto-shifter Stair-type wave generator (IC012) to shift the ΔTb output voltage from the 10-times amplifier (IC006B).
When the output voltage falls within −2.15 V to −0.73 V, the comparator (IC008) outputs a High level signal to IC003A so as to complete the auto-shift function.



[Output timing]

REF, Ti, Tb and ΔTb are outputted from HA OUT every 4msec in the following order.



3-4-4 TEMP Head Amp (AW-800PA) Board, UP-0319

◆ General

The 160 Hz low-pass filter (R022&C007, R023&C008) eliminates any high frequency component, such as interference caused by an electrosurgery unit.

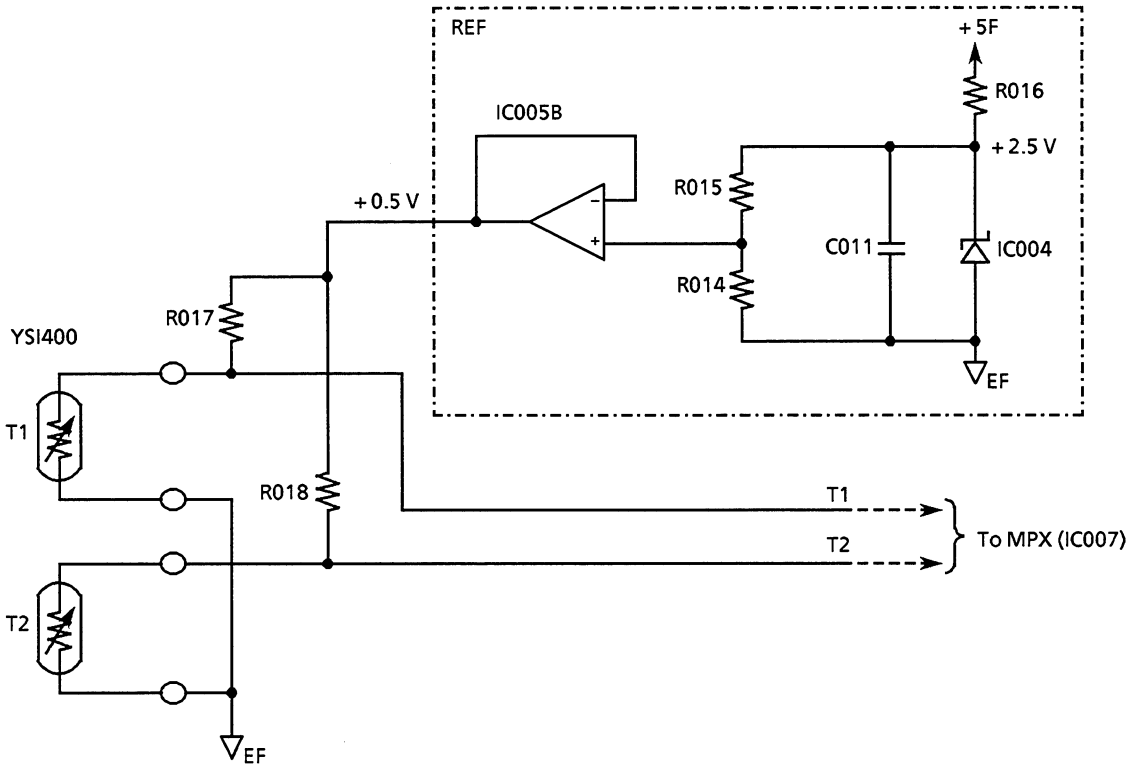
The multiplexer (IC007) time-shares the reference voltage for 27°C, REF0, calibration voltage for 37°C, CAL37 and body temperature T1 or T2.

The counter (IC008) generates control signals for IC007.

◆ R-V Converter

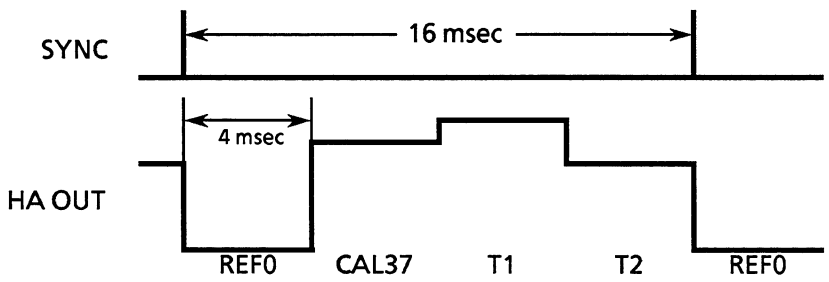
The following circuit composed of IC004/005B, R014 ~ 016 and C011 generates an + 0.5 V reference voltage.

T1 or T2 voltage is obtained according to temperature by dividing the 0.5 V reference voltage between R017 and T1-thermistor or R018 and T2-thermistor.



[Output timing]

REF0, CAL37, T1 and T2 are outputted from HA OUT every 4msec in the following order.



3-4-5 Respiration Head Amp (AR-800PA) Board, UP0548

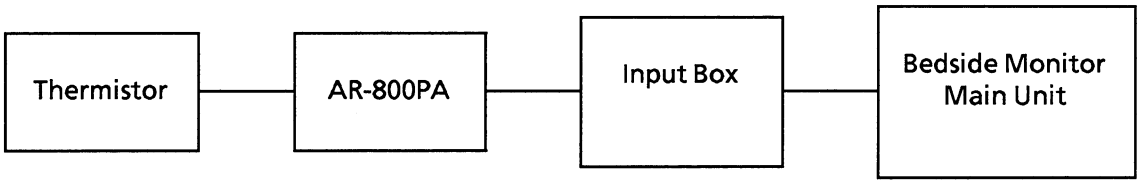
◆ Specifications

● General

AR-800PA is one of the head amplifiers for the BSM-8000 series bedside monitor to measure respiration with a thermistor pickup.

● System connection

Respiration head amplifier is inserted into the input box of the bedside monitor and a thermistor is connected to the head amplifier.



◆ General Description

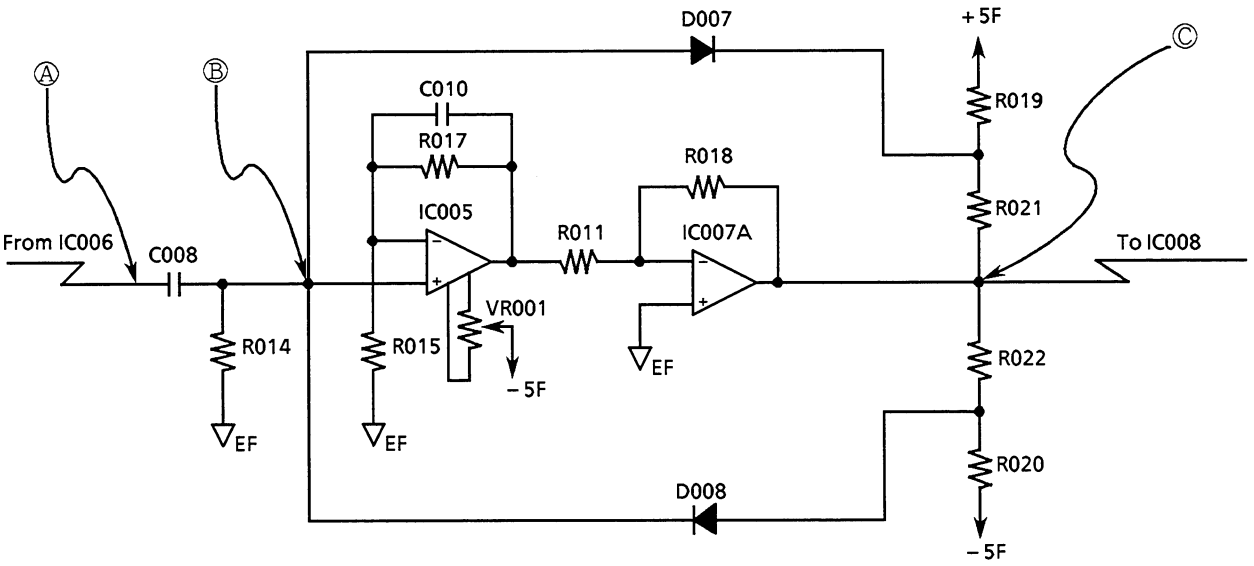
The AR-800PA consists of UP-0548 respiration board mounting floating power supply, respiration pickup exciter voltage (EXC) generator, input high-cut filter (3Hz), amplifier, auto inst (instantaneous baseline recovery) circuit, etc.

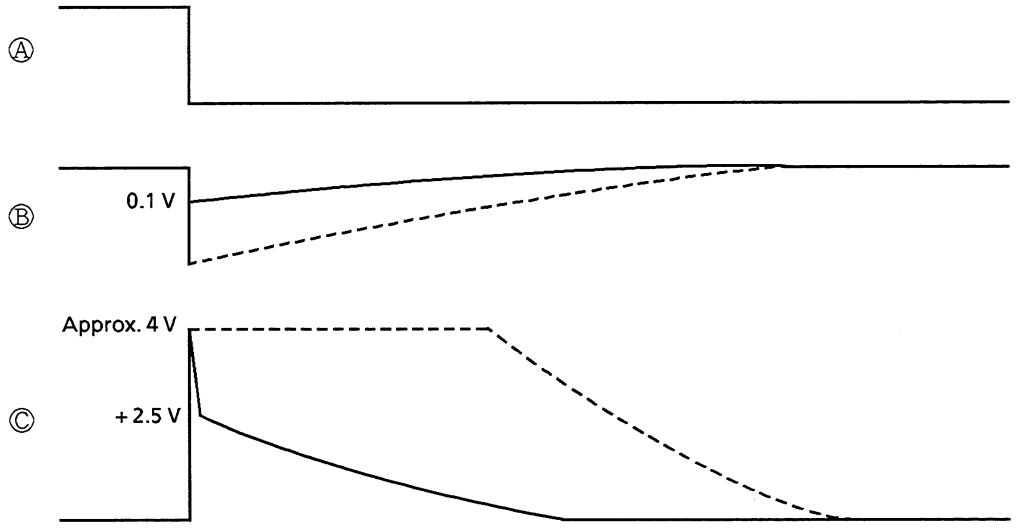
◆ Output

Analog signal is outputted without being time shared which is different from other head amplifiers.

◆ Auto Inst (Instantaneous Baseline Recovery) Circuit

Auto Inst function works when respiration waveform signal saturates in the circuit just after the pickup is connected to the amplifier or due to over-input.



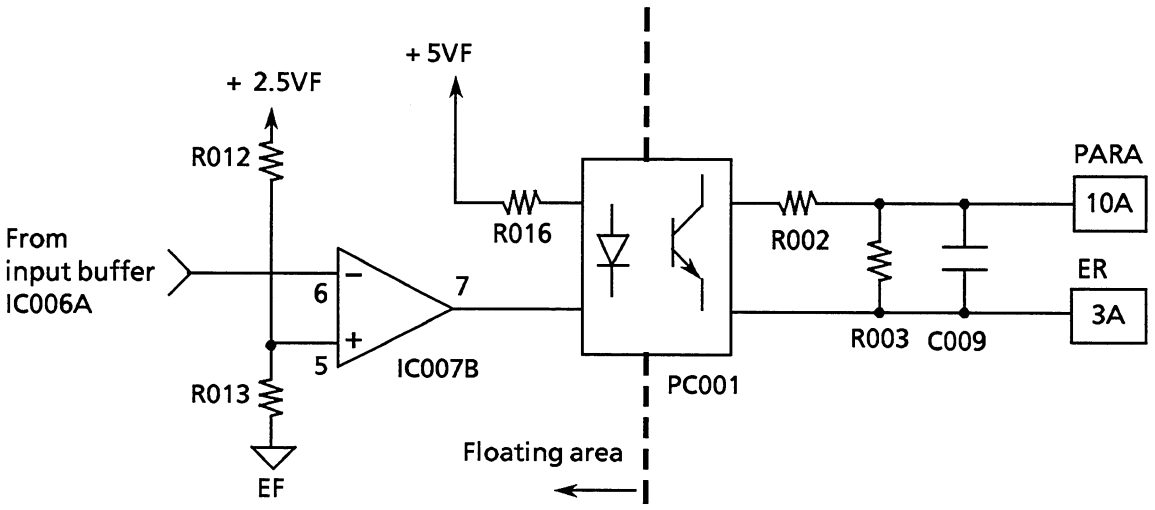


Straight lines indicate the voltages with the auto inst function and dotted lines indicate the voltages without diodes D007 and D008.

◆ PARA Signal Generating Circuit

Connection and disconnection of the respiration pickup change the PARA voltage as below:

+0.58V ±20mV ..... no connection
+0.65V ±20mV ..... connection



When the thermistor respiration pickup is not connected, comparator input pin-6 of the IC007B is approximately +2.5V and the comparator outputs level L. At this condition, PC001 photocoupler is conductive and +0.58V PARA output voltage is obtained. This voltage indicates no respiration measuring condition with the thermistor pickup.

When the pickup is connected, comparator pin-6 input is approximately +1V and the PC001 photocoupler becomes off, and +0.65V PARA voltage is obtained. This voltage indicates respiration measuring condition with the thermistor pickup.

3-4-6 SpO_2 Head Amp (AL-800PA) Boards, UP-0551 & 0552

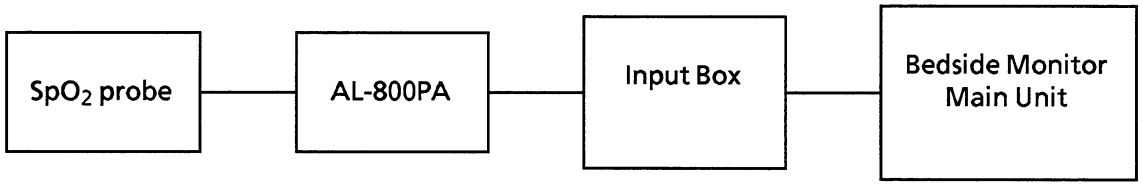
◆ Specifications

● General

AL-800PA is one of the head amplifiers for the BSM-8000 series bedside monitor to measure SpO_2 oxygen saturation.

● System connection

SpO_2 head amplifier is inserted into the input box of the bedside monitor and a SpO_2 probe is connected to the head amplifier.



◆ General Description

This unit has a function to detect the following four signals for calculation of % SpO_2 (oxygen saturation).

R	.....	Transmitted red light intensity
△R	.....	Transmitted red light intensity variation (△ R1 = △R2 × 8)
IR	.....	Transmitted InfraRed light intensity
△IR	.....	Transmitted InfraRed light intensity variation (△IR1 = △IR2 × 8)

The SpO_2 head amplifier composes of UP-0551 Main board and UP-0552 Sub board. Block diagram on page 11.17 shows the major functions of each board.

● UP-0551 Main board

Red light and infrared light are emitted from the two LED lamps alternatively at 1kHz interval which is controlled by LED control circuit. Transmitted light through the subject are detected and converted into voltages by a photo detector and an amplifier, amplified to a specified level of signal by an auto gain controller, and then transferred to the Sub board.

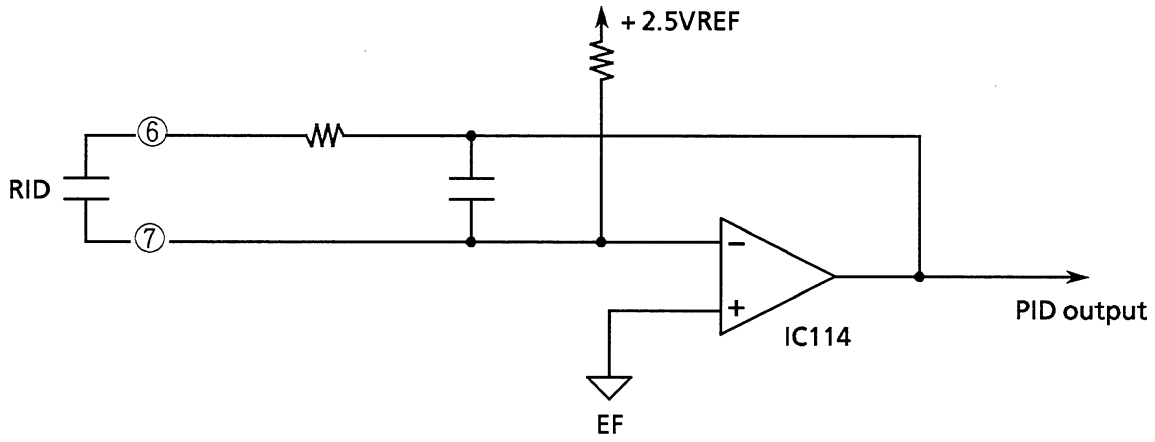
● UP-0552 Sub board

Noise in the transmitted light signal from the Main board is reduced by a time sharing filter. Base hold circuit holds the signal level while there is no light emission to the –2.5V reference voltage (REF). R (Red light intensity signal) and IR (InfraRed light signal) are separately demodulated by two sample hold circuits and △R2 and △IR2 are outputted by AC amplifiers with auto inst (instantaneous baseline recovery) function. At the same time, △R1 and △IR1 are outputted by 8 time gain amplifiers. Finally these signals are converted into a time-shared signal by a multiplexer and then outputted through the UP-0551 Main board.

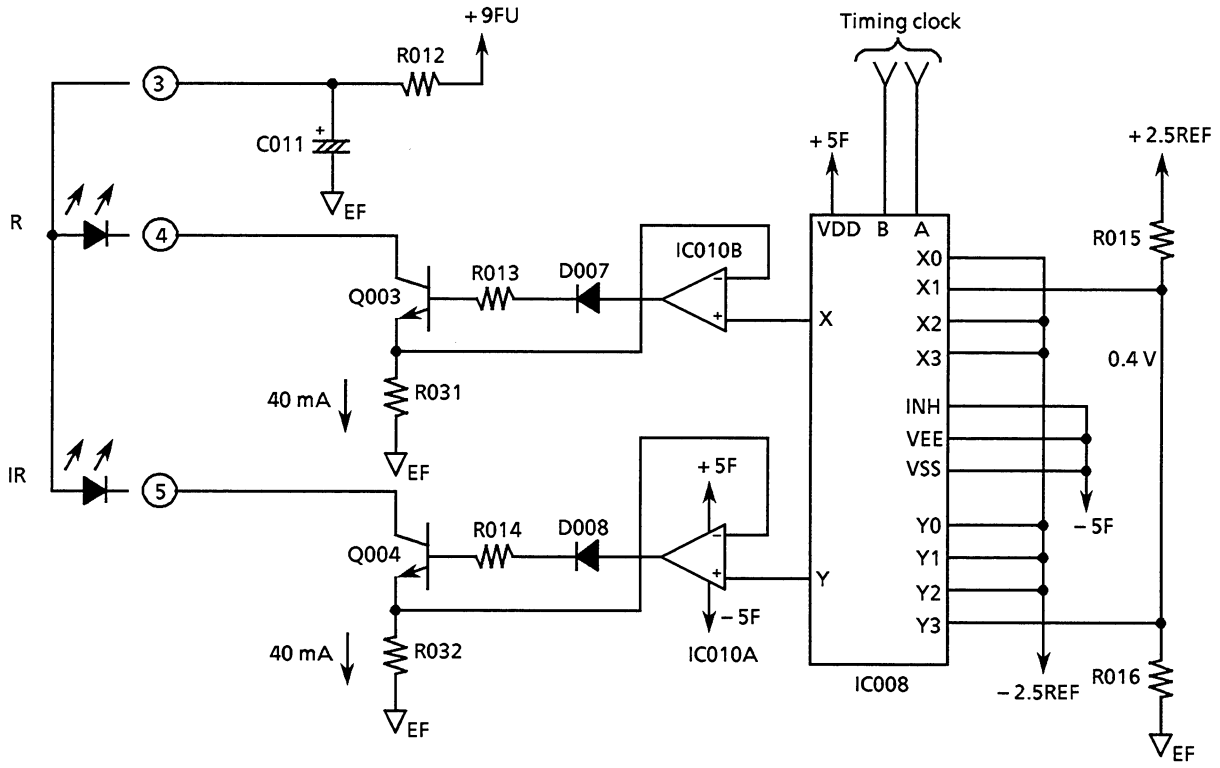
◆ Probe ID Amplifier

The probe ID amplifier compensates the variations of wavelength of light emitted from the LED lamps and also detects probe connection to the SpO_2 head amplifier.

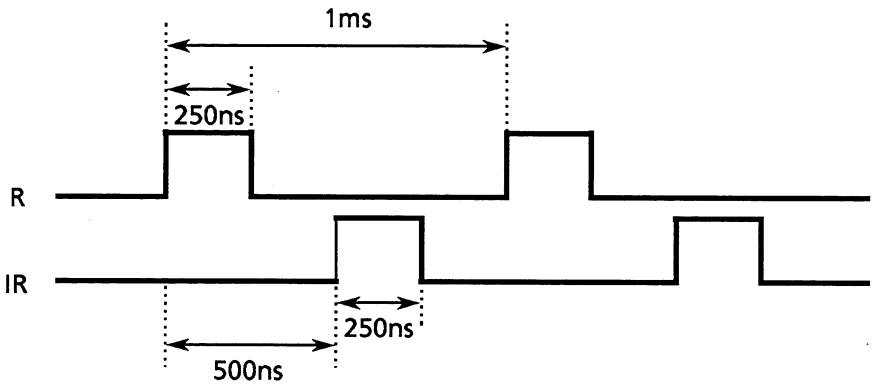
Each SpO_2 probe has its own ID (determined by the RID) which is converted into voltage signal (PID: Probe ID).



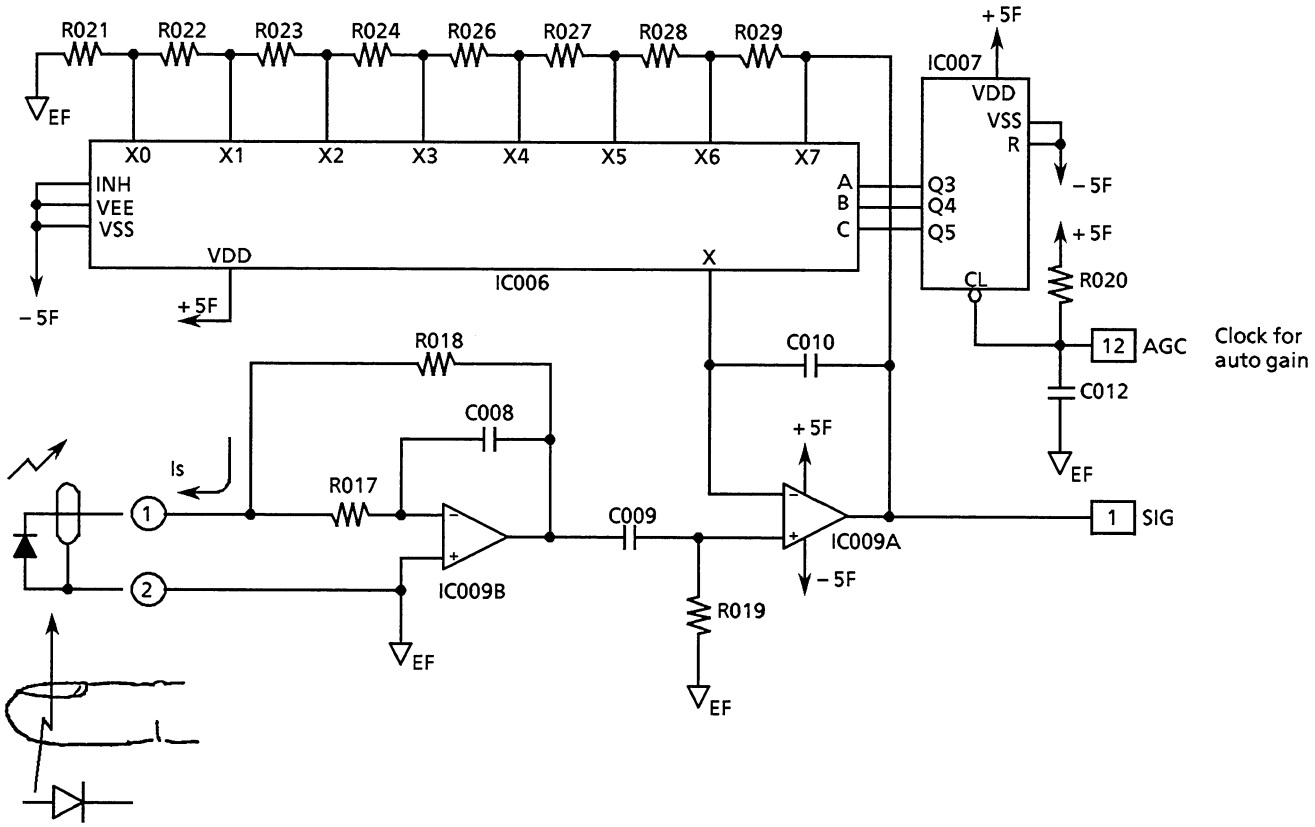
◆ **LED Control Circuit**



Red light and infrared light are emitted from the two LED lamps alternatively at 1kHz interval controlled by above LED control circuit. Peak current flow of each LED is 40mA.



◆ Input Amplifier and Auto Gain Control Circuit



Transmitted light detected by the photodiode and the detection current "Is" is converted into voltage signal by the amplifier and the feedback resistor R018.

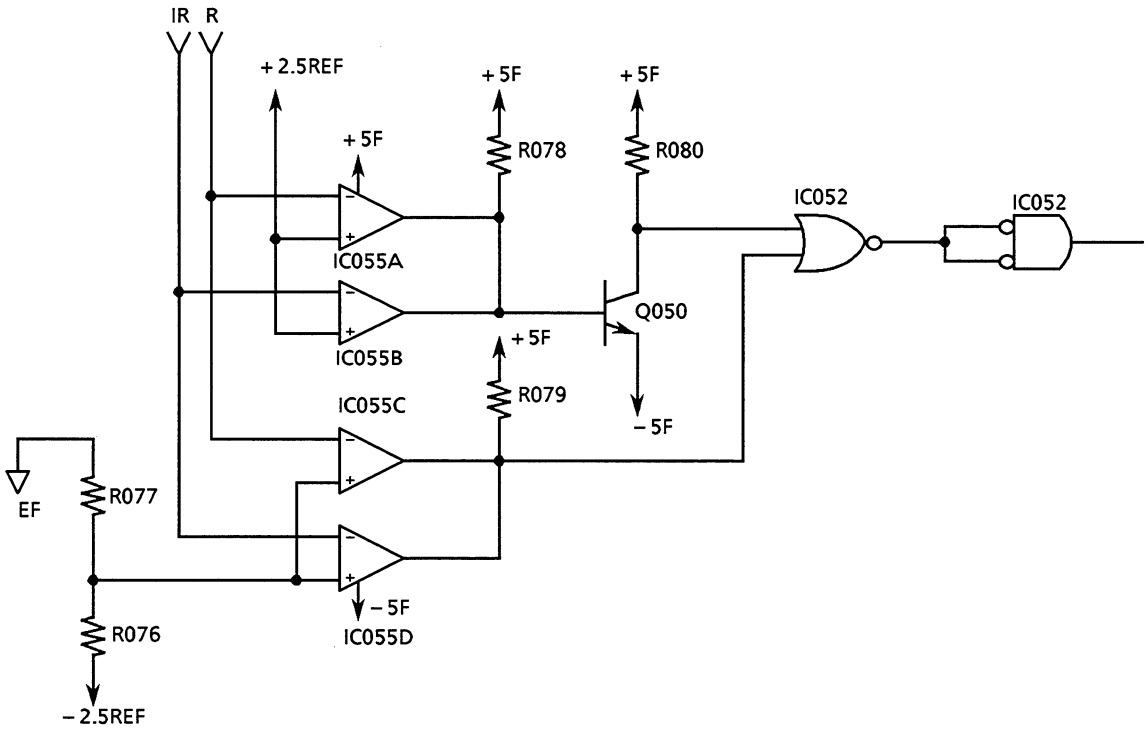
After being DC cut by the capacitor C009, voltage signal is amplified to a specified level by the auto gain control circuit consists of the IC switch IC006 and resistors.

AGC (Auto Gain Clock signal) stops which is triggered by the auto gain control circuit when R or IR signal comes into a specified range.

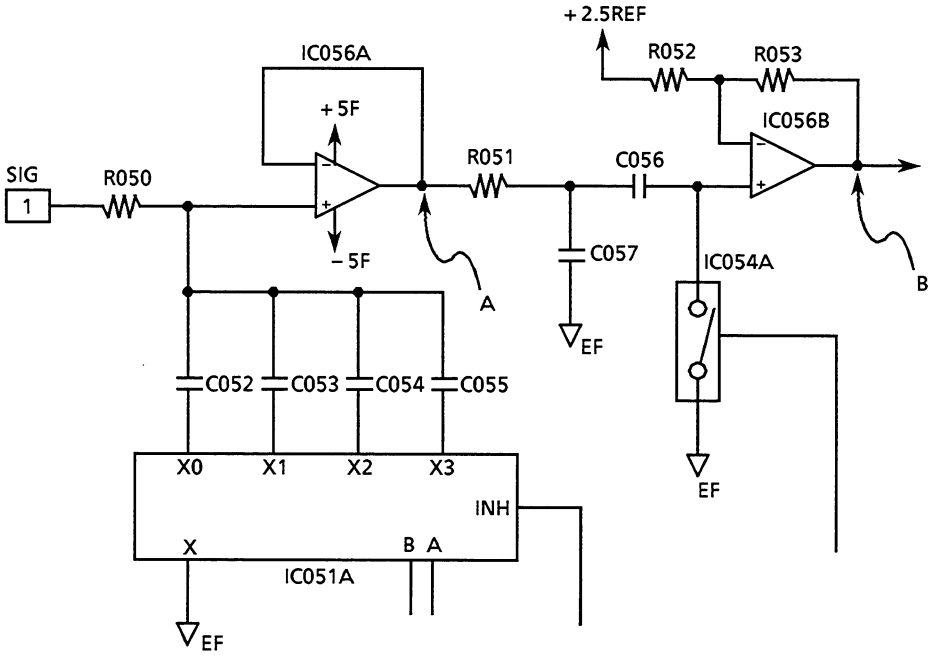
◆ Comparator for Auto Gain Control

The comparator controls the AGC (Auto Gain Clock signal) on/off or the auto gain control circuit.

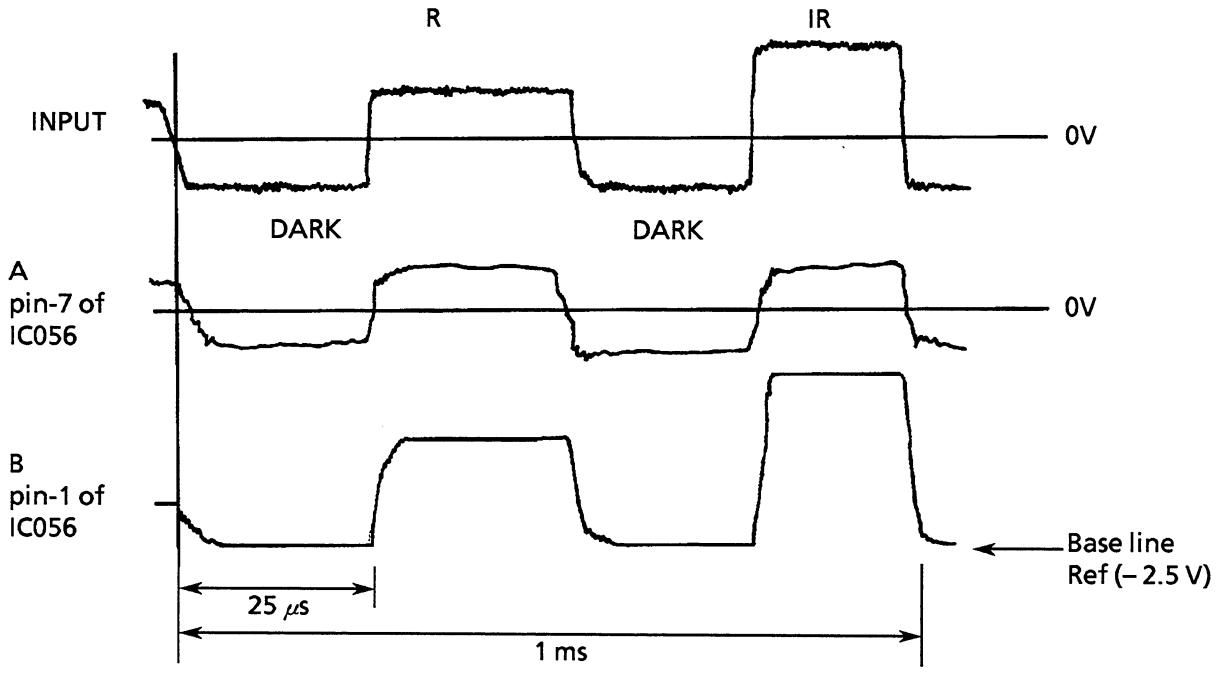
When either R or IR signal comes into a range from −1 V to +2.5 V, the output pin-4 of the IC052 turns to LOW to stop the AGC signal.



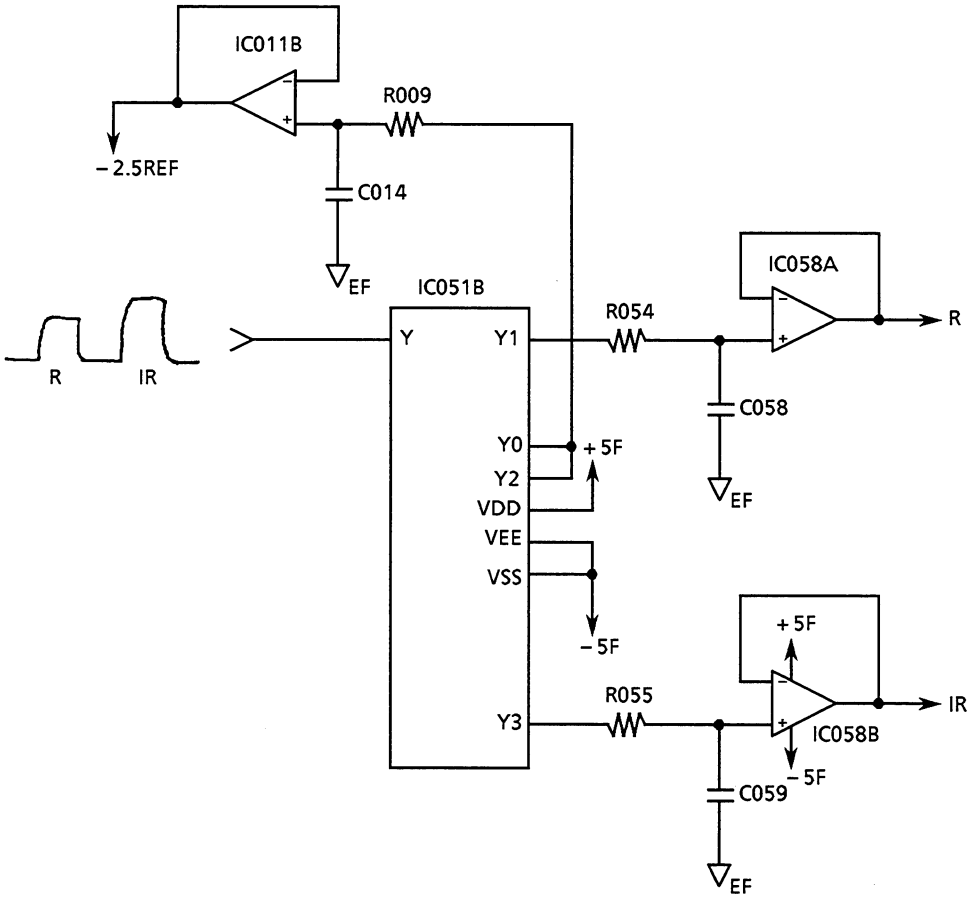
◆ Time Sharing Filter with Base Hold Circuit (Sub Board)



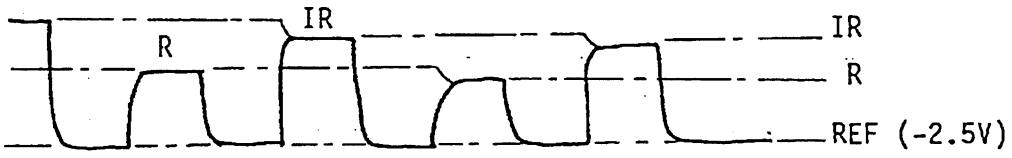
This circuit reduces noise component in the signal from the Main board and holds the baseline (signal level while there is no light emission) of the signal to −2.5V reference voltage (REF).



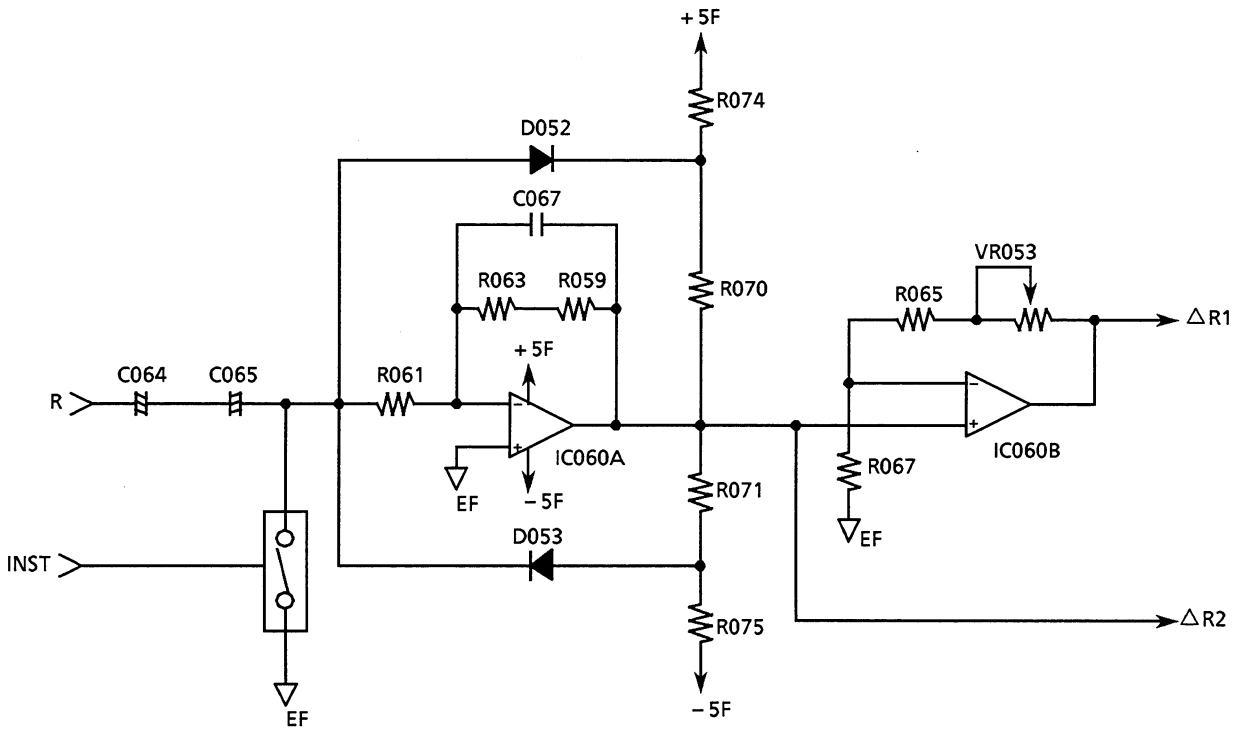
◆ Sample Hold Circuit



This circuit sample holds the R, IR, and REF (baseline) signals of the base held signal as below:



◆ AC Amplifier with Auto Inst Function



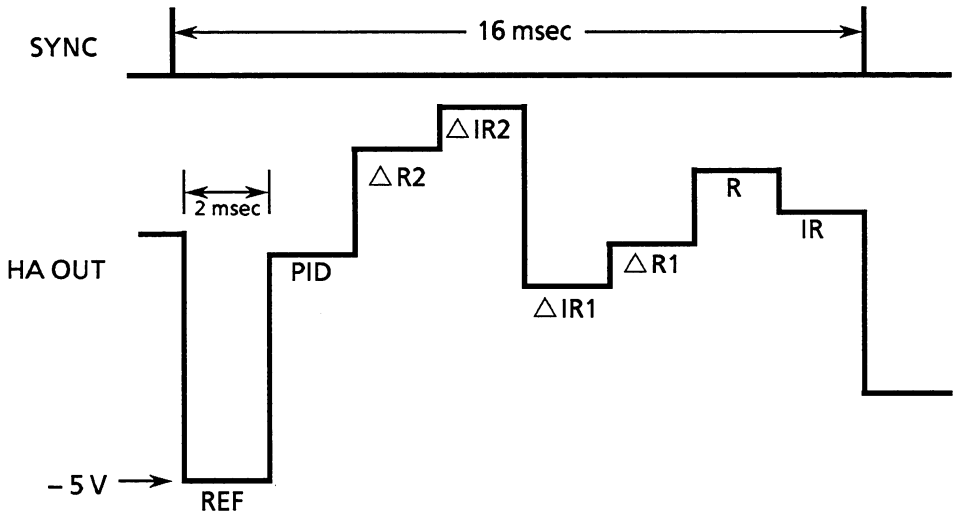
After being DC cut by the capacitors C062 and C063, the sample-held R signal is 5 times amplified by the IC059A to be the △R2 signal.

The diodes D050 and D051 recover the baseline when the signal level is saturated in the circuit (auto inso function).

The analog switch IC054B shortens the input line of the amplifier IC059A during auto gain control so that the signal level can quickly recover after the auto gain control is released. △R2 signal is 8 times amplified by the IC059B into the △R1 signal.

Above operations are applied to the IR signal in the same manner applied to the R signal.

◆ Output Timing



◆Adjustment

Volume on the PC boards are for gain adjustment of amplifiers. If you replace resistors concerning amplification gain, volumes should be readjusted.

There is no need to adjust the volumes when IC chips are replaced.

3-4-7 EEG Head Amp (AE-800PA) Boards, UP-0421 & 0422

The AE-800PA consists of UP-0421 EEG main board mounting, an EEG, control, output and floating power supply circuits, and UP-0422 EEG sub board mounting an amplifier processing circuit.

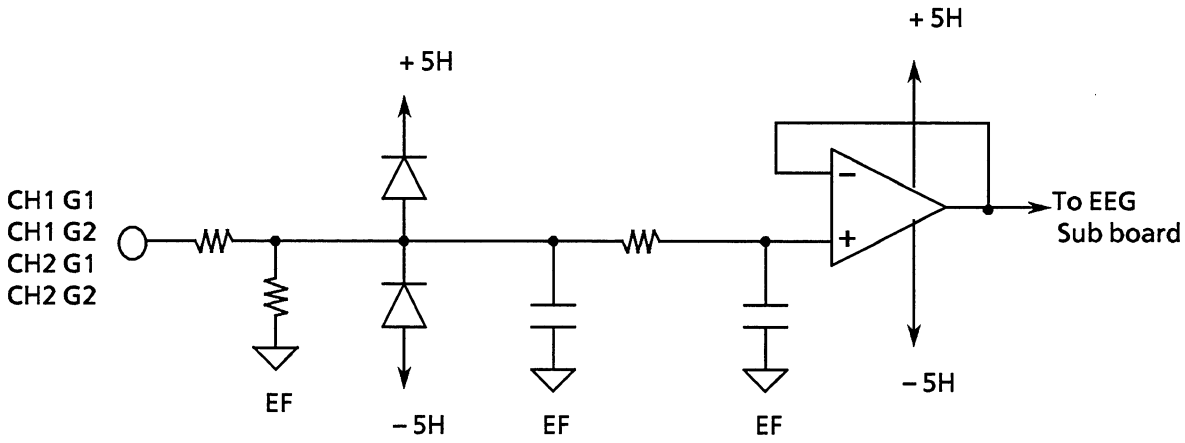
• UP-0421 EEG main board

Protection filters protect the circuits against large input generated by an ESU and defibrillator, etc. EEG input signals after the protection filters are transferred to the EEG sub board, and amplified, filtered and then returned to the EEG main board. Two EEG signals are time shared every 4msec into EEG1 and EEG2 output signals of the AE-800PA EEG head amplifier. Each buffer output is fed back to the EEG neutral electrode terminal (N) to increase the CMRR(Common Mode Rejection Ratio) to be called Reference Feedback for later descriptions.

• UP-0422 EEG sub board

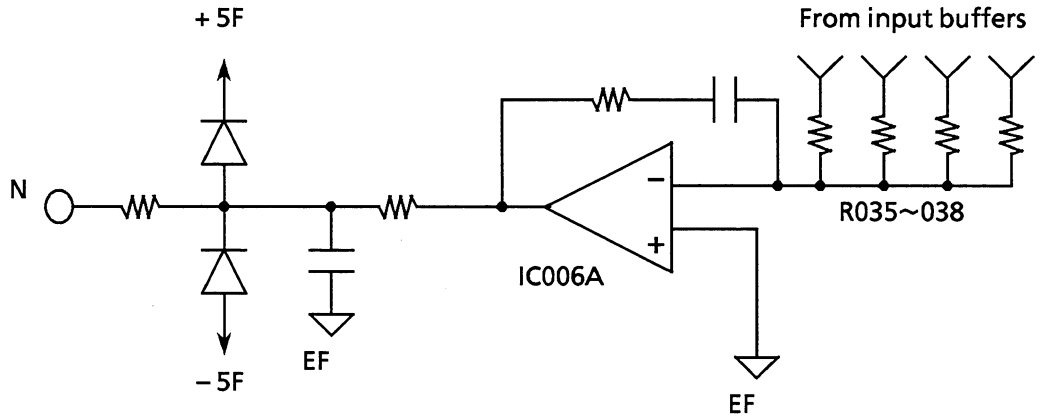
The UP-0422 consists of pairs of total 5000 gain amplifiers, 35Hz high-cut filters and AC interference filters. 0.3sec time constant is determined in this block.

◆ Input Buffer on the UP0421 Main Board



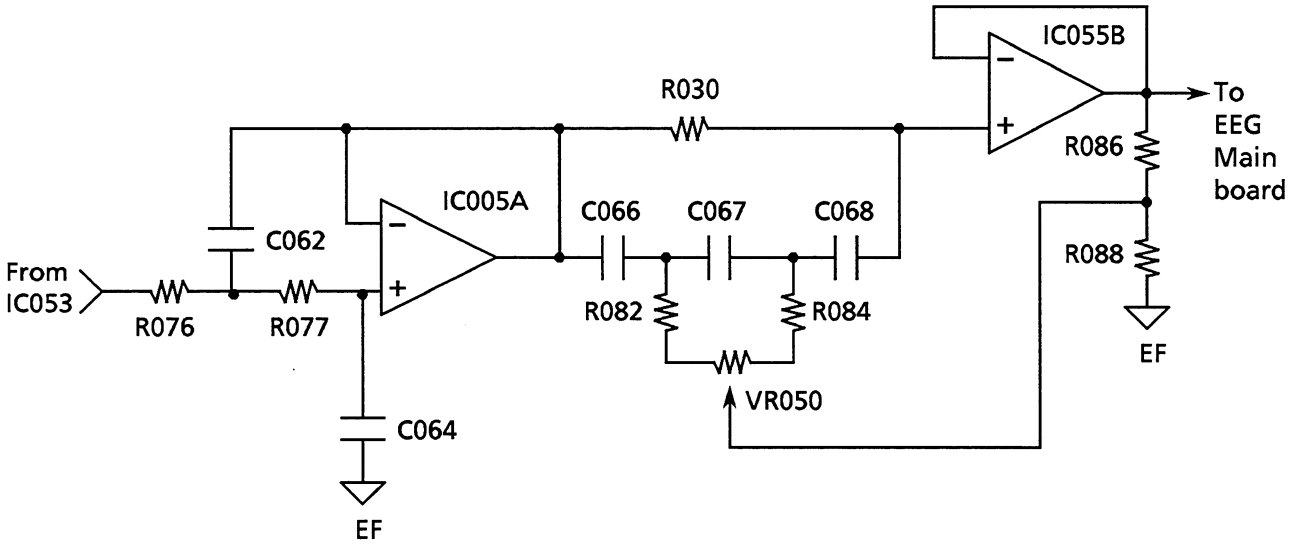
Two CR high-cut filters attenuate noise component in the EEG signal. Resistors limit large current and diodes limit large voltage (from ESU, defibrillator, etc.) to protect against damage of the circuit.

◆ **Reference Feedback**

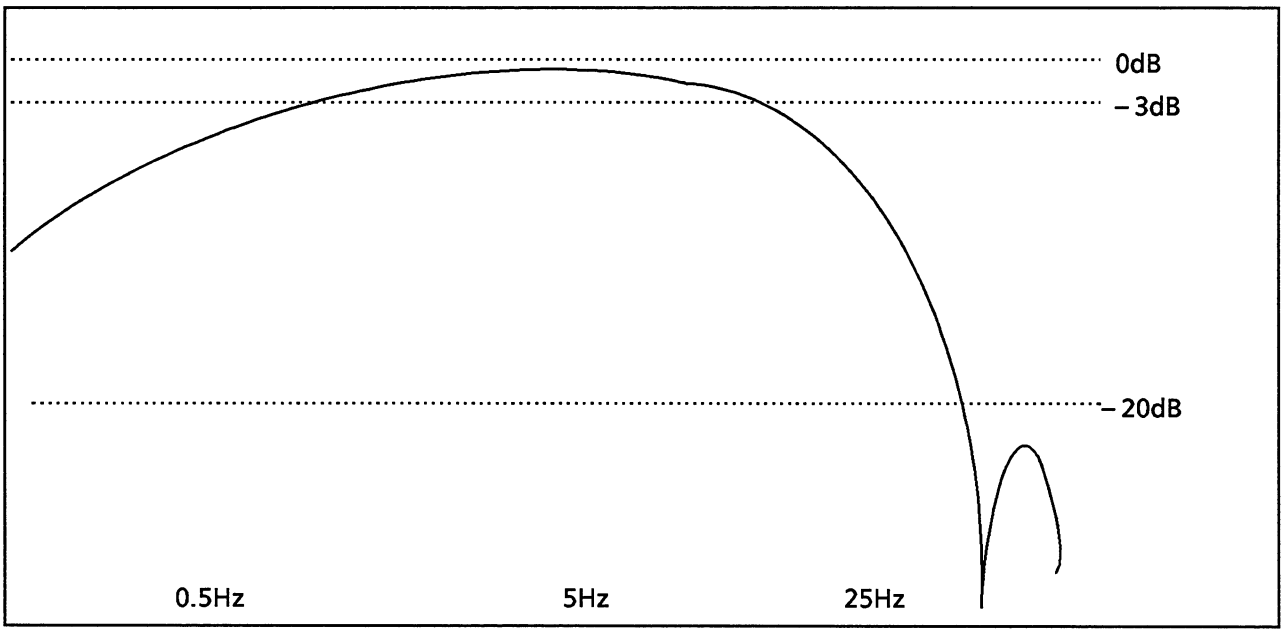


As the EEG signal is amplified by the differential amplifier, theoretically it is not interfered by common mode noise. However, due to variation in electrode impedance and electronic devices used, difference between the phases of the common mode component appears at the EEG amplifier output as noise.
By feeding back (negatively) each buffer output to the neutral electrode terminal(N), common mode component referred to the floating ground (EF) is reduced and the CMRR is increased.

◆ **High-cut Filter and AVC Filter on the UP-0422 EEG Sub Board**

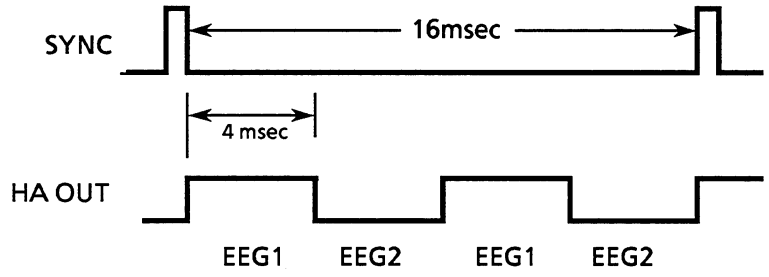


Two stage high-cut filters consisting of IC055A, C062, C064, R076 and R077, and AC filter consisting of IC005B, C066, C067, C068, R080, R082, R084, R086, R088 and VR050 filter high frequency components and AC noise in the EEG signal. Total frequency characteristics of the filters is shown below.



◆ Timing of the Output Signals

This EEG head amplifier outputs in the following timing

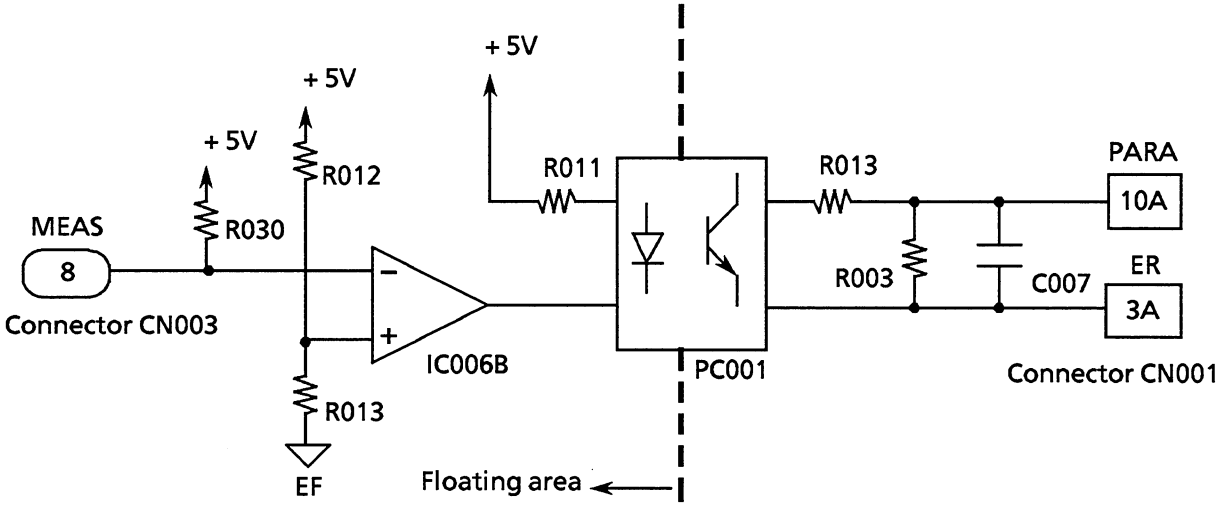


* Refer to the pages of BP head amplifier for signal signal modulation/demodulation between the floating area and grounded area.

◆ PAPA Signal Generating Circuit

Connection and disconnection of the EEG cable change the PARA voltage as below:

+1.7V ±40mV ..... not connected
+1.9V ±40mV ..... connected



When the EEG cable is not connected, comparator input pin-6 of the IC006B is pulled up to +5F through the R030, and the comparator outputs level L.
At this condition, the PC001 photocoupler is conductive and the resistance (PARA resistance) across the PARA and ER terminals is a parallel value of the R004 and R003, and the PARA voltage reads +1.7V. This voltage indicates EEG non measuring condition.

When the cable is connected, the PC001 is not conductive, the PARA resistance is R003 only, and PARA voltage reads +1.9V. This voltage indicates EEG measuring condition.

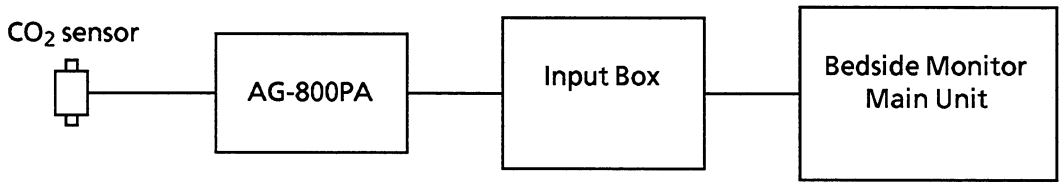
3-4-8 CO_2 Head Amp (AG-800PA) Boards, UP-0588 & 0589 and TG-706P

◆ General

AG-800PA is one of the head amplifiers for the BSM-8000 series bedside monitors to measure CO_2 partial pressure of expired gas of a patient with TG-706P CO_2 sensor.

◆ System Connection

CO_2 head amplifier is inserted into the input box of the bedside monitor and the CO_2 sensor is connected to the head amplifier.



◆ Description of Each Function Block

• UP-0588 CO_2 Main board

Power (DC-DC) line is a power to drive the CO_2 sensor TG-706P and DRIVER is a electrical current driver of a motor in the sensor.

S-P and D/A circuit reads the linearization data (compensation factor for CO_2 calculation, differs in each sensor) which written in the ROM in the sensor.

TIMING CONTL 1 circuit controls output timing for reading linearization data, and HAOUT output timing.

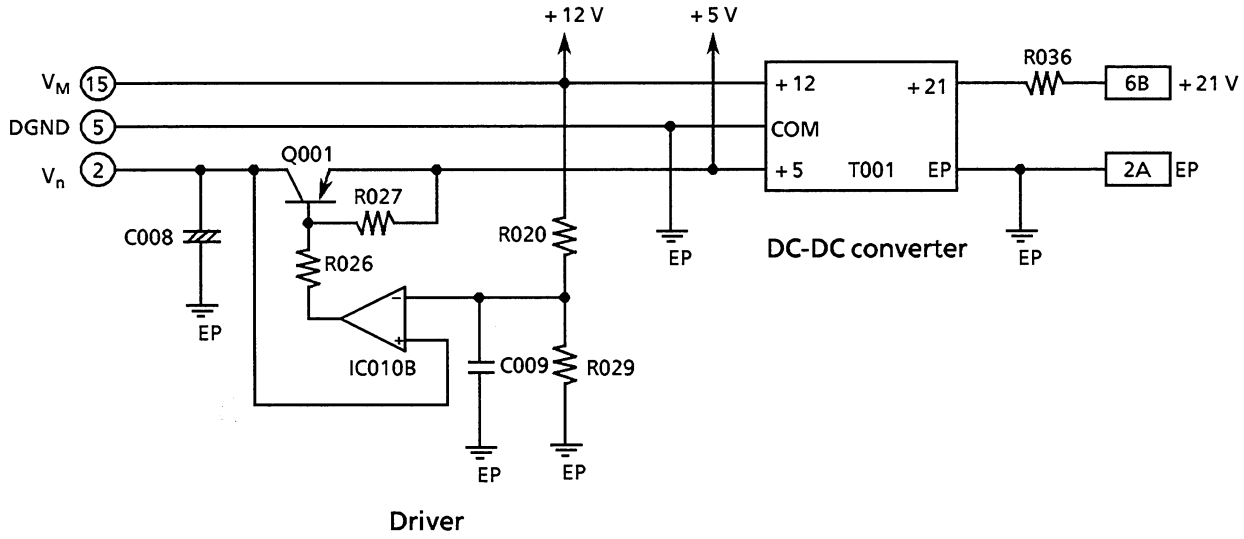
• UP-0589 CO_2 Sub board

ZERO SHIFT circuit shifts the VAC sensor signal baseline to – 5REF (-4.75V) in order to widen dynamic range of the signal.

P/H (peak-hold) circuit holds amplitude of the signal based on – 5REF reference voltage.

3.75S/H (Sample and hold) and 4.3S/H circuits sample each V3.7 signal and V4.3 signal in the VAC signal.

◆ **Sensor Driver Power (DC-DC, DRIVER on CO_2 Main Board)**



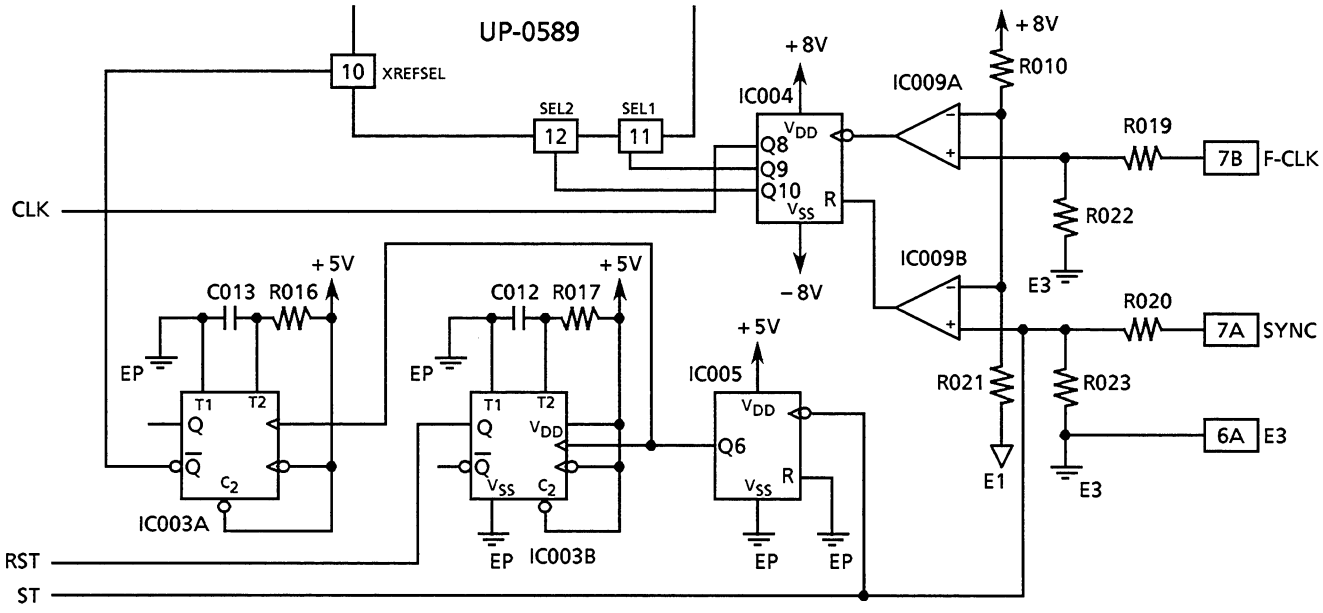
Driver

DC-DC (T001) is a DC-DC converter that generates +12 V and +5 V voltages from +21 V unregulated power.

+12 V is a power for an infrared ray lamp in the CO_2 sensor of 120mA continuous load current and +12 V ±1% stability.

+5V drives a motor and digital IC devices in the sensor. The circuit indicated with DRIVER drives the motor.

◆ TIMING CNTL 1 (CO_2 Main Board)



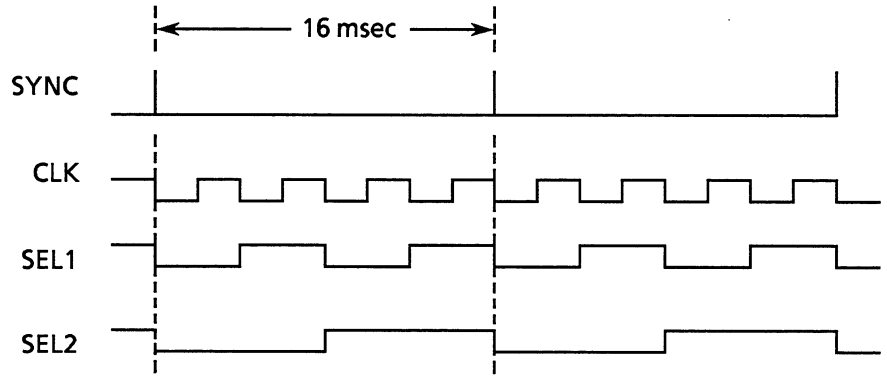
* SEL1, SEL2 ..... Clock signals to control HAOUT signal output timing.

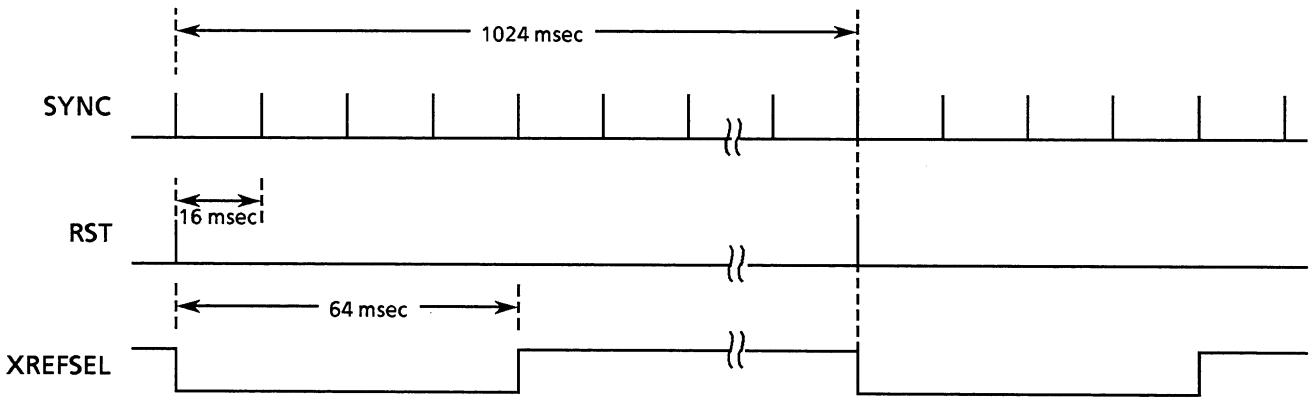
* XREFSEL ..... Control signal to output data to HAOUT by switching –5REF signal and linearization data.

* CLK ..... Clock signal to control ROM and S/P (Serial to Parallel) converter in the sensor.

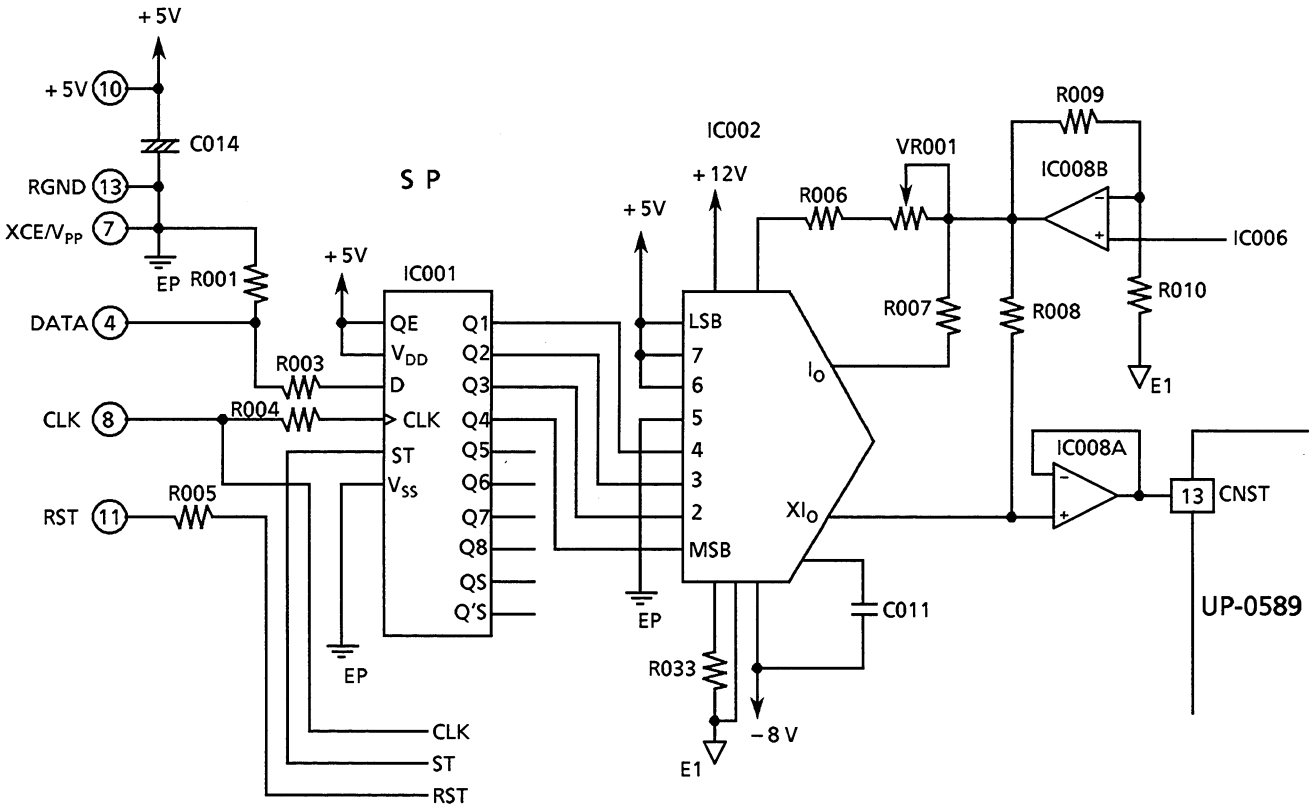
* RST ..... Signal to reset the ROM in the sensor.

* ST ..... Signal to control S/P conversion.





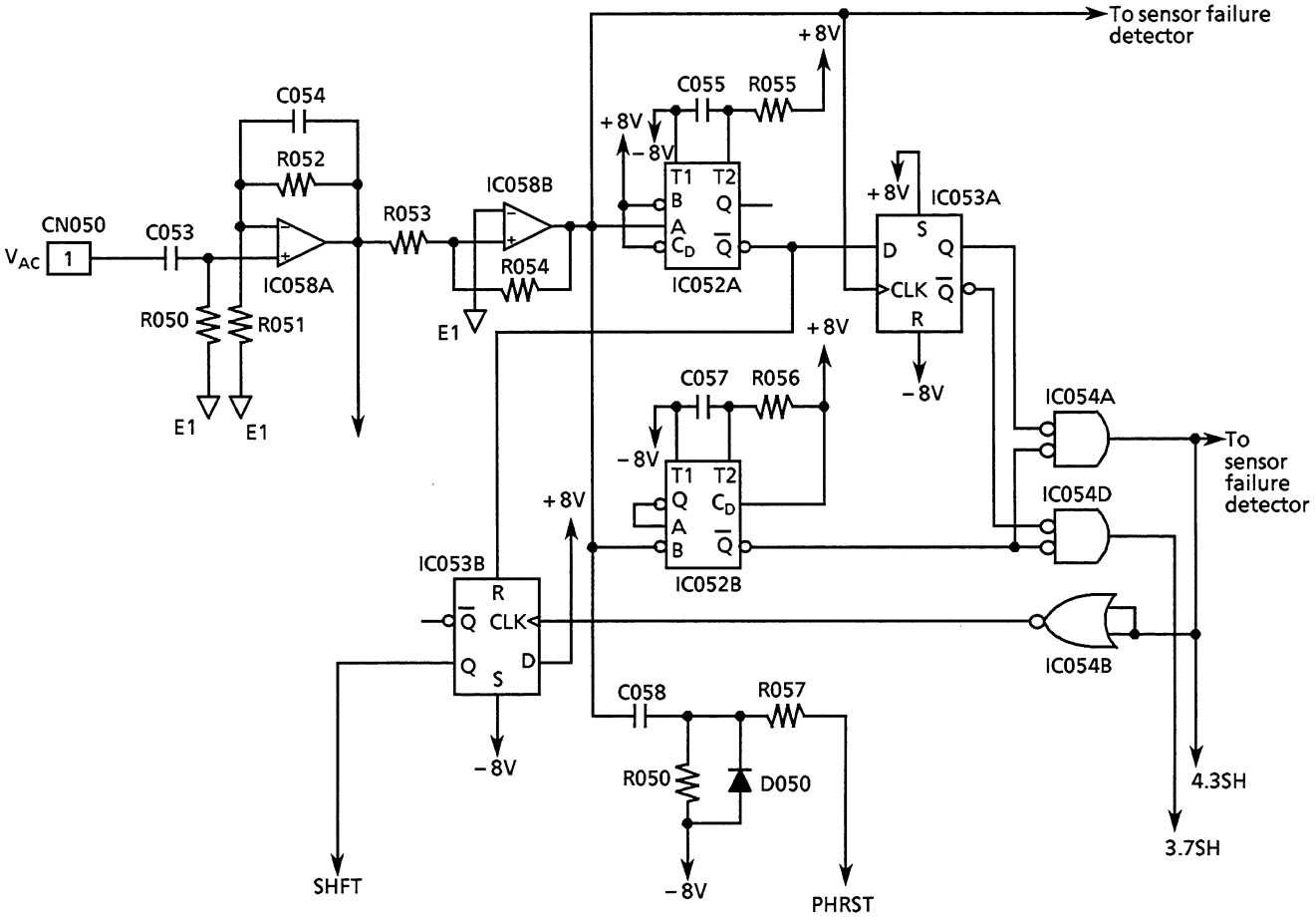
◆ S/P Conversion and D/A Conversion (CO_2 Main Board)



Linearization data (DATA) stored in the ROM in the sensor is output from the ROM in synchronization with CLK signal in serial format data. This serial format data is S/P converted into parallel format data in synchronization with ST signal.
Relation between the linearization data and D/A output is as below.

Linearized data	D/A out (V)	Linearized data	D/A out (V)
0 0 0 0	−4.80	1 0 0 0	+0.32
0 0 0 1	−4.16	1 0 0 1	+0.96
0 0 1 0	−3.52	1 0 1 0	+1.60
0 0 1 1	−2.88	1 0 1 1	+2.24
0 1 0 0	−2.24	1 1 0 0	+2.88
0 1 0 1	−1.60	1 1 0 1	+3.52
0 1 1 0	−0.96	1 1 1 0	+4.16
0 1 1 1	−0.32	1 1 1 1	+4.80

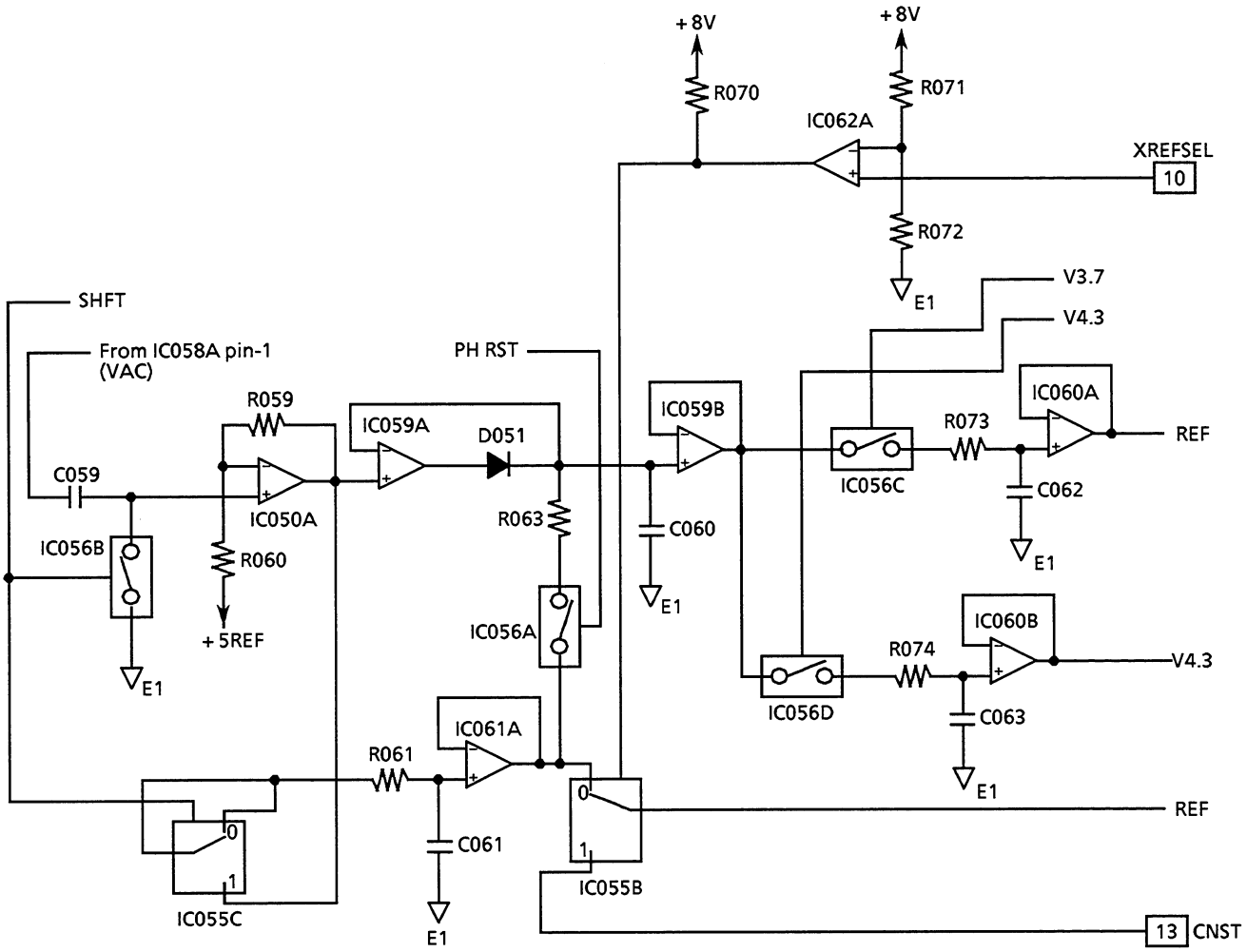
◆ TIMING CONTL 2 (CO_2 Sub Board)



* SHFT	.....	Control signal to shift V_{AC} signal baseline in the ZERO SHIFT circuit to −5REF (−4.75 V) level.
* PH RST	.....	Pulse to reset Peak-Hold circuit following the ZERO SHIFT circuit.
* 3.7SH	.....	Sampling pulse of V3.7 signal in the V_{AC} signal.
* 4.3SH	.....	Sampling pulse of V4.3 signal in the V_{AC} signal.

Refer to page 3.155 for CO_2 signal demodulation timing.

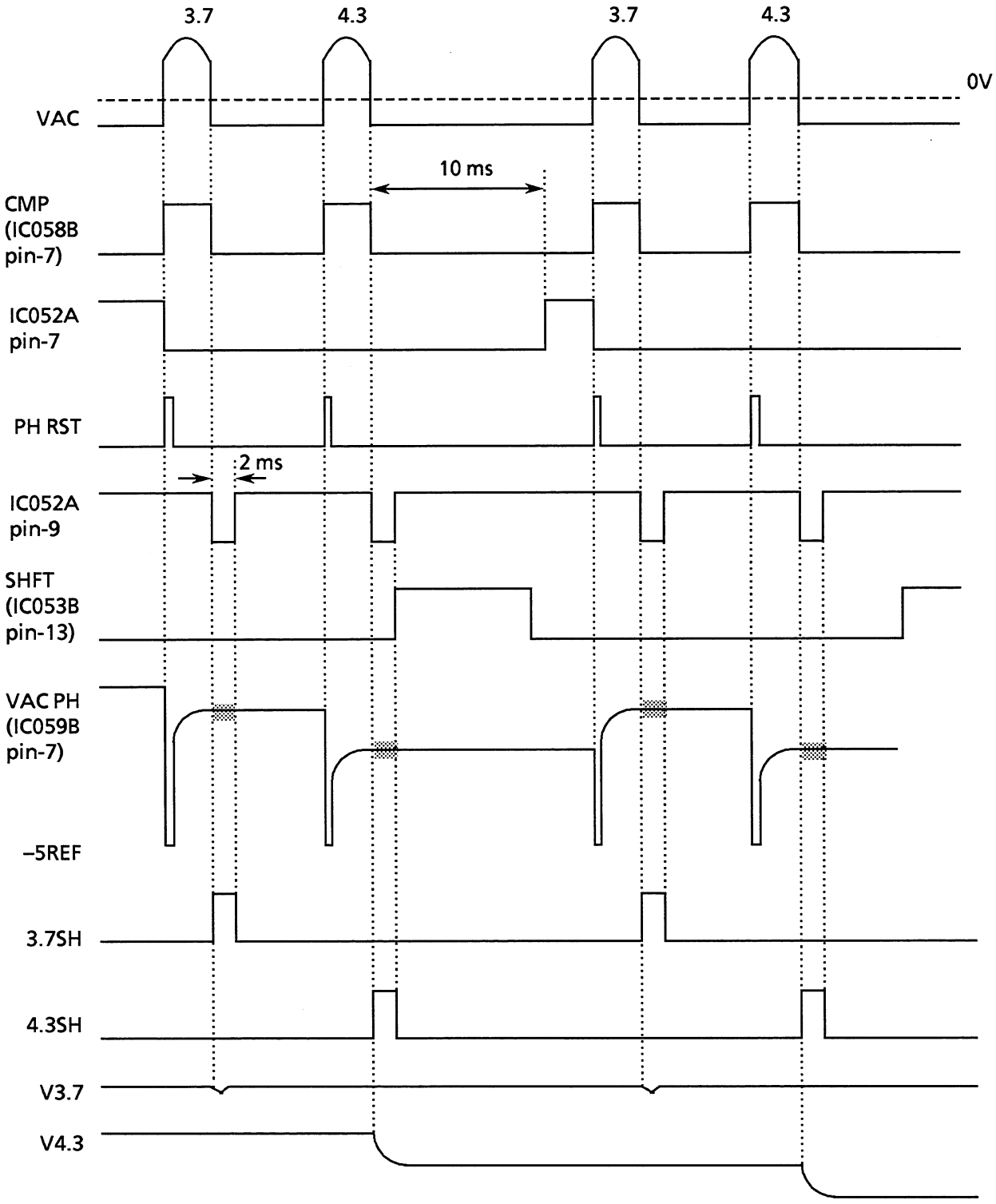
◆ V3.7, V4.3 and REF Signal Detection Circuit (CO_2 Sub Board)



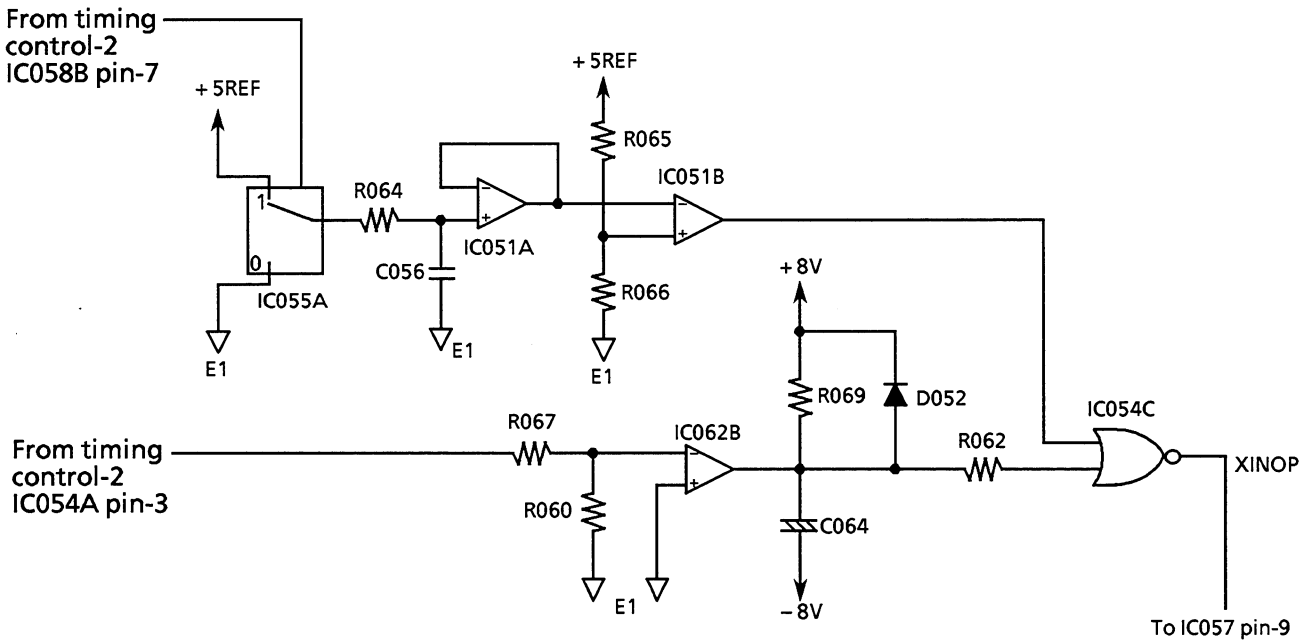
VAC signal baseline is shifted (IC050A pin-1) into – 5REF signal (IC061A pin-1) by SHFT pulse. CNST signal is D/A converted linearized data. This CNST and – REF signal output as REF signal by switching CNST signal and – 5REF signal by XRESET signal.

The IC059A peak-holds the amplitude of V_{AC} signal based on – 5REF signal and the IC060A and IC060B sample hold V3.7 and V4.3 signals composing of V_{AC} signal and output the signals as V3.7 and V4.3.

◆ CO_2 Signal Demodulation Timing



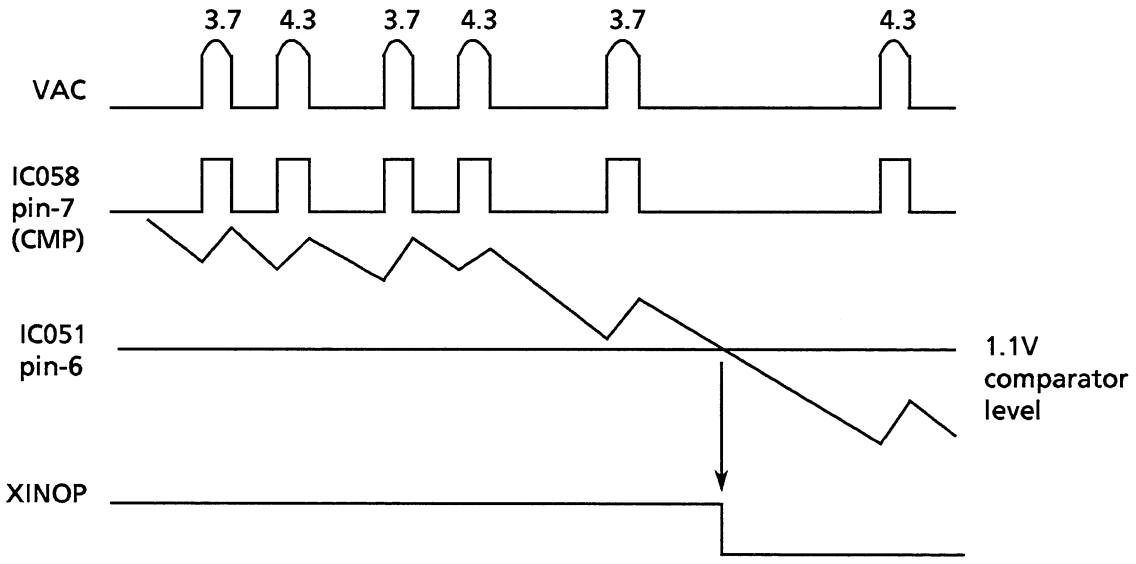
◆ Operation of Sensor Failure Detection



In normal operation, both IC054 pin-8 and pin-9 are "L" (-8V) logic level and pin-10 XINOP (Inoperative) output is "H" level.

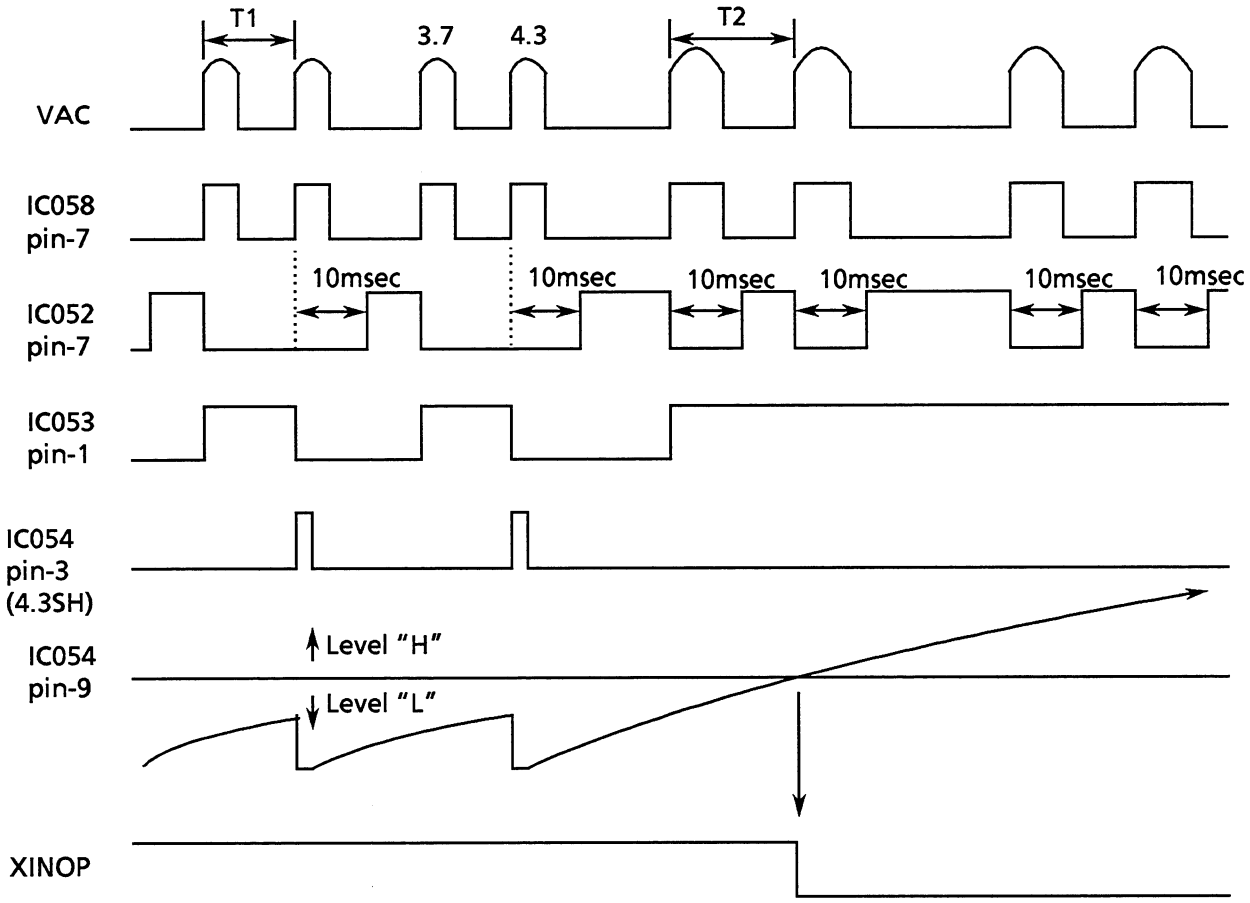
• When there is no 3.7 or 4.3 or both in the V_{AC} signal

When there is no 3.7 or 4.3 or both in the V_{AC} signal, CMP pulse is not generated or number of pulses decreases to half, and charging time of the C056 becomes short, then the comparator (IC051B) outputs "H" level and XINOP signal becomes "L". The head amplifier output signal HAOUT is – 5V in this condition.



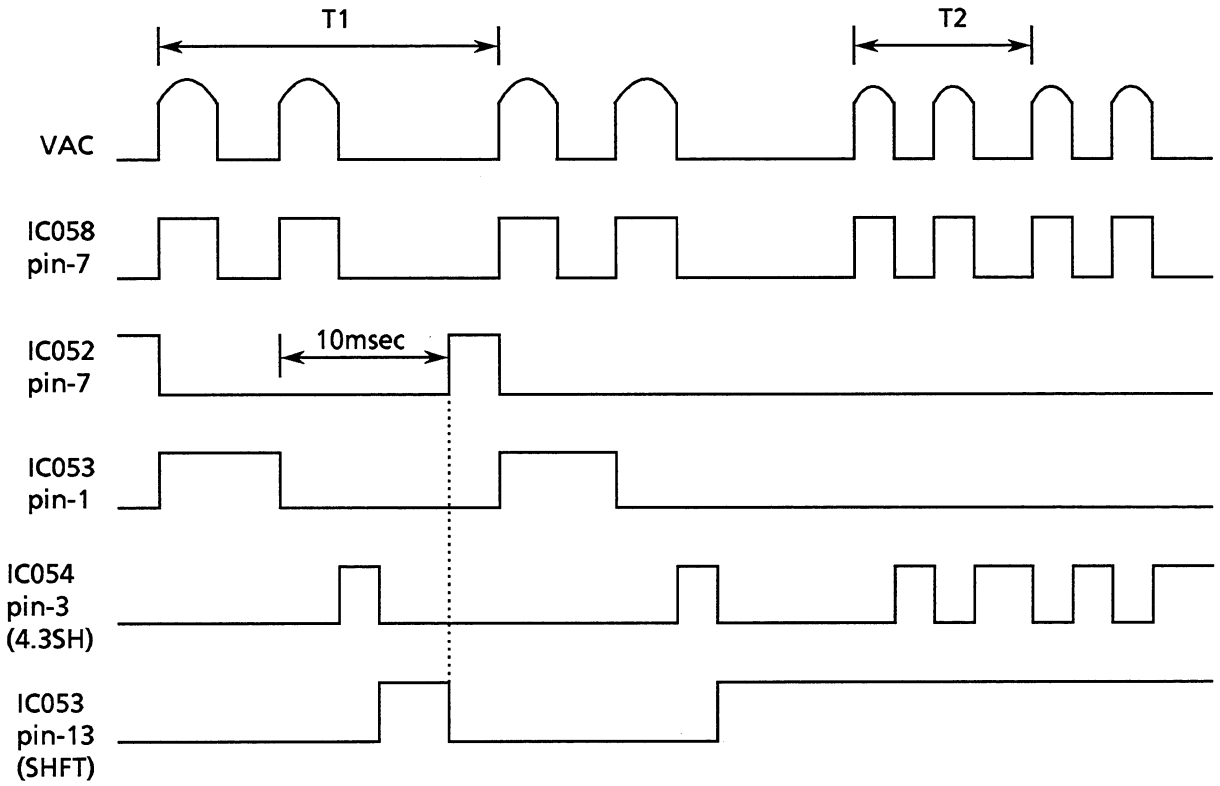
• When the V_{AC} output interval is prolonged (decrease of motor revolution)

When the V_{AC} output interval T1 between 3.7 and 4.3 is prolonged it exceeds 10msec of one-shot time of IC052A, output of the IC053A (pin-1) becomes always "H" and the C064 is charged up by +8V, then XINOP signal turns to "L" and HAOUT head amplifier output becomes – 5V.

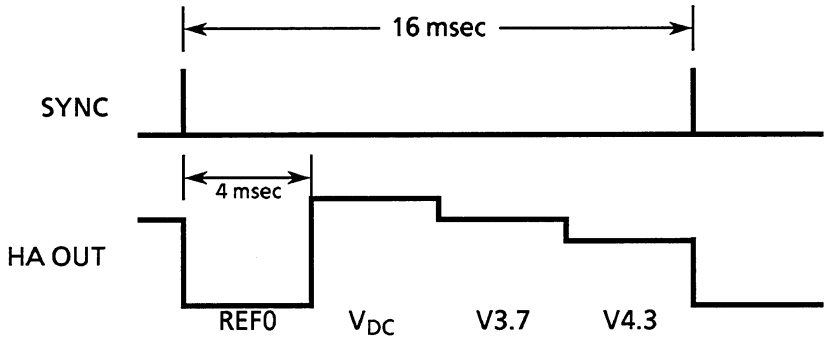


• When the V_{AC} output interval is shortened (increase of motor revolution)

When the interval T2 between the 3.7 and next 3.7, it becomes shorter than 10msec one-shot time of the IC052A output (pin-7) becomes "L" and SHFT pulse (IC053 pin-13 is fixed to "H". Then IC050A input pin-3 is fixed to E1 (ground) and head amplifier output HA4.3 becomes equal to – 5REF voltage.

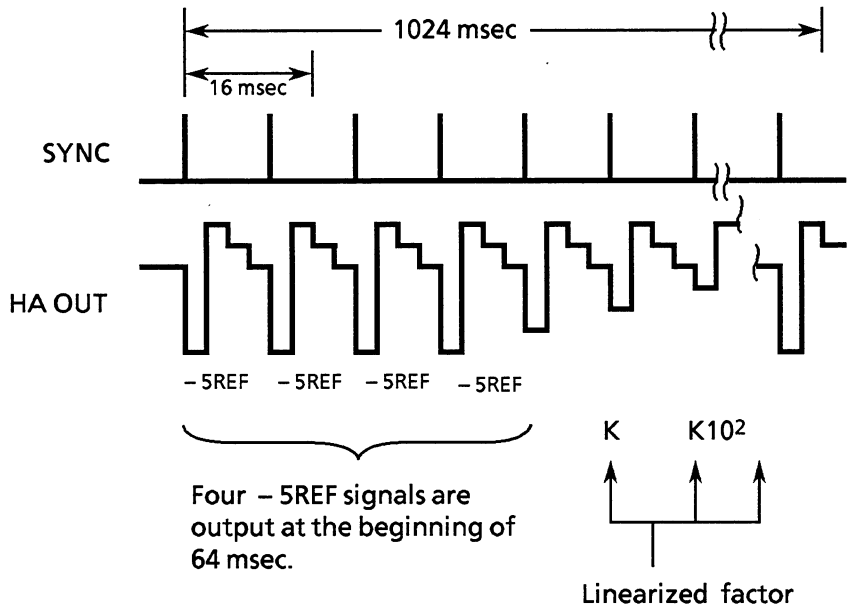


◆ **Timing of Output Signal**

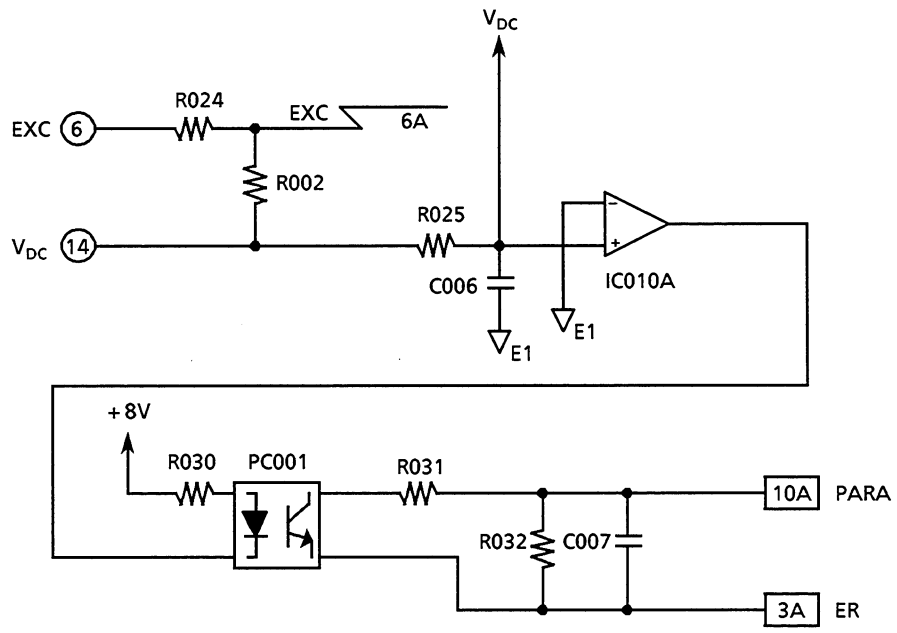


REF: –REF signal which is a reference of V3.7 and V4.3 signals and linearization data of each sensor required for CO_2 calculation are output for 4msec from the SYNC pulse every 16msec in a cycle of 1204msec.

– 5REF output range: – 4.75V ±0.2V



◆ Unit Discrimination Signal (PARA Voltage)



PARA (parameter) voltage changes when the CO_2 sensor is connected and disconnected as below.

Sensor	PARA voltage (V)
Connection	2.40 ±0.05
Disconnection	2.10 ±0.05

When the sensor is not connected, EXC (−5 V) is applied to the comparator input terminal (IC101A pin-3) and comparator output is "L". With this voltage, the photocoupler PC001 is conductive and 2.1V voltage attenuated with R031 and R032 resisters appears as PARA voltage at no sensor connection.

When the sensor is connected, +1 V to +5 V voltage is applied to the comparator input terminal (IC101A pin-3) and comparator output turns to "H". With this voltage PC001 becomes off and 2.4V appears as PARA voltage at sensor connection.

◆ TG-706P CO_2 Sensor

• General

The infrared ray which is absorbed by CO_2 gas (4.3um wavelength) and the infrared ray which is not affected by CO_2 gas (3.7us wave length) are used in the CO_2 sensor.

• Sensor output signals

The CO_2 sensor outputs three signals.

VDC ..... DC voltage for compensating signal drift due to temperature change of the sensor. It corresponds to resister value of the infrared ray detector.

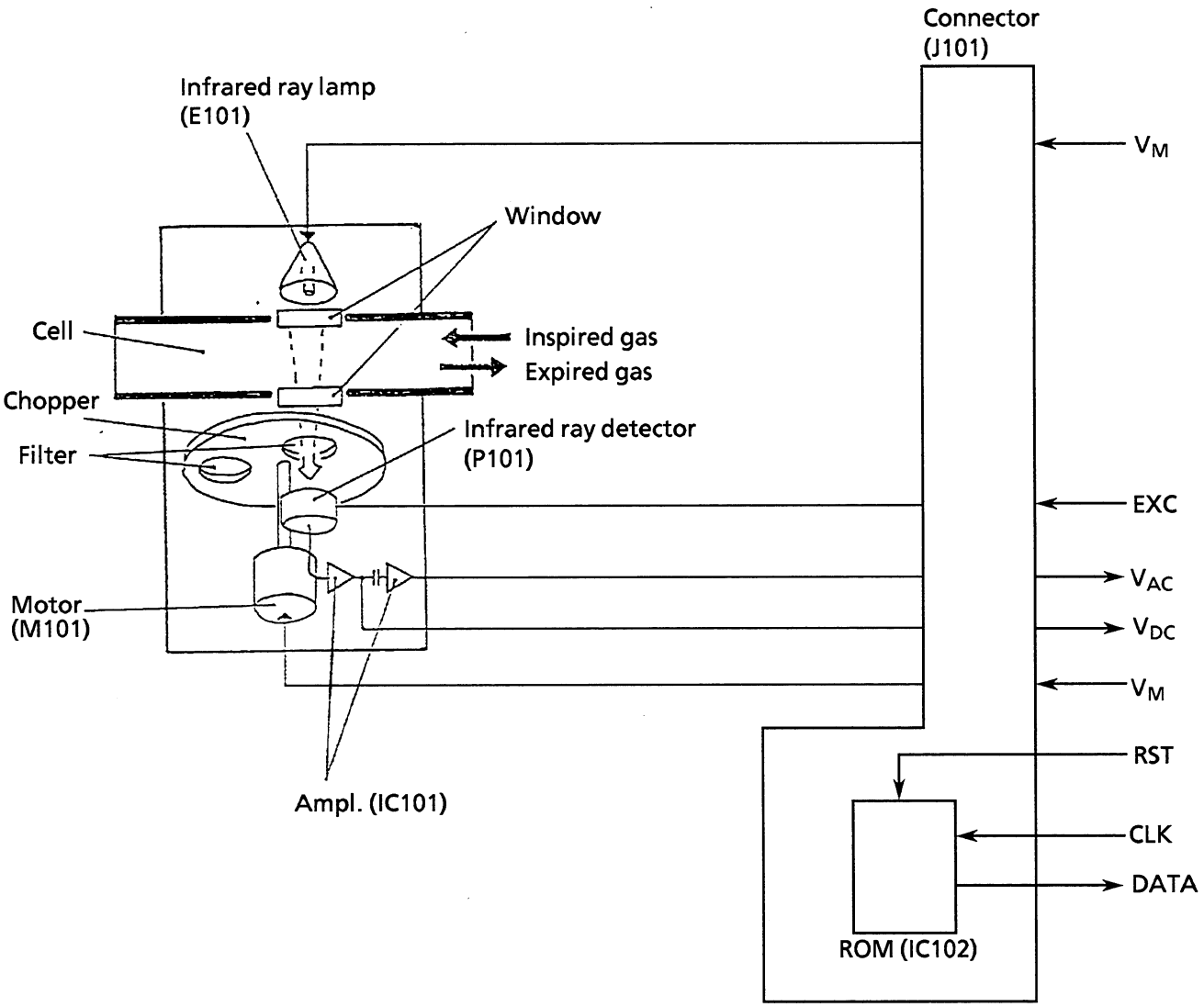
VAC ..... AC voltage of light strength signal. The infrared ray that passes through respiratory gas in the cell and the filter is converted into a light strength signal after being converted to a resistance signal and then to an electrical signal. One rotation of the chopper is taken to be one cycle, and the signal (V4.3) through the 4.3um filter (altered CO_2 partial pressure) and the signal (V3.7) through the 3.7um filter (not affected by CO_2 gas, used for reference), are output alternatively.

VAC signal is a mixture of the V4.3 and V3.7 signals.

DATA .... Compensation coefficient to calculate CO_2 value, 256 bit serial data stored in ROM chip inside each CO_2 sensor.

• Head amplifier output signals

The AG-800PA CO_2 head amplifier separates V4.3 and V3.7 signals from VAC signal and outputs DATA, VDC, V3.7 and V4.3 signals in order successively. DC voltage indicating infrared ray detector resistance value.



VAC ..... AC voltage including V4.3 signal (altered by CO_2 partial pressure) and V3.7 signal (not affected by CO_2 gas, used for reference).

DATA ..... Compensation coefficient to calculate CO_2 value, 256 bit serial data stored in chip inside each CO_2 sensor (linearization data).

EXC ..... −5 V ±2% power voltage to drive (excite) the infrared ray detector.

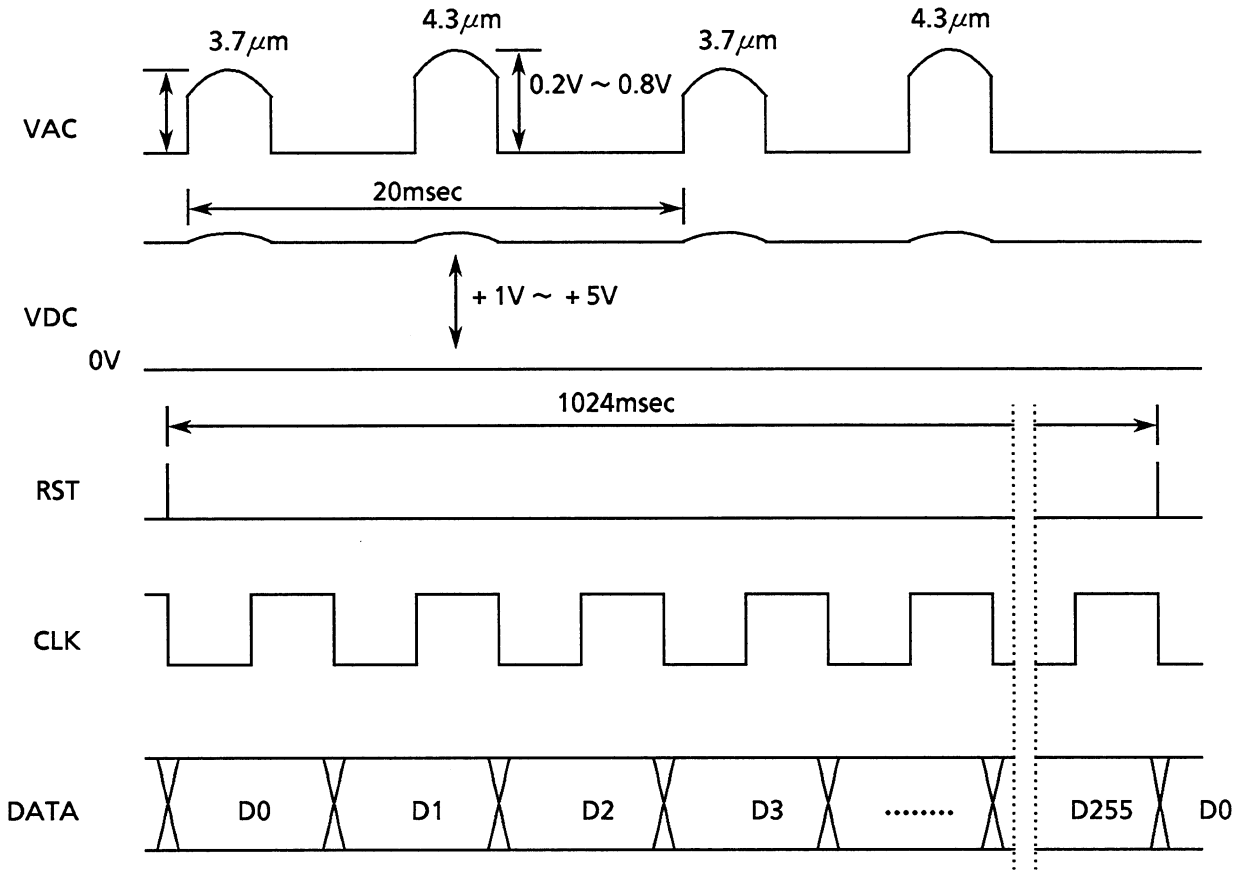
VH ..... +12 V ± power voltage to drive (heat) the infrared ray lamp.

VM ..... +2.4 V ±2% power voltage to drive the motor for chopper disc.

RST ..... ROM reset pulse, 1024 msec interval.

CLK ..... 250 Hz clock signal.

● **CO2 Sensor Input/Output Signal Timing**



NOTE
VAC and DATA are asynchronous.

3-4-9 O_2 Head Amp (AG-820PA), UP-0592

◆ General

The AG-820PA is one of the head amplifiers of BSM-8000 series bedside monitors to measure fraction of inspired oxygen (FiO_2) using an O_2 sensor connected with a ventilator, etc.

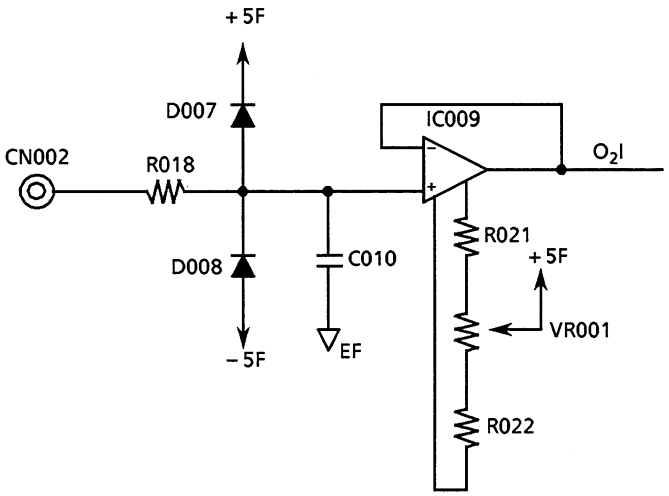
Diodes for over-voltage protection and high-cut filter for noise reduction are employed in the input circuit block.

• Composition

After filtering, signal is buffed with IC009 and IC010 and then multiplexed with IC007 multiplexer device. Multiplexer output signals are Ref0, O_2I, and O_2II. Multiplexing is controlled by clock signal generated by IC006 counter.

• Input buffer

There are two similar circuits of input buffer for O_2I and O_2II. Description below is for O_2I.

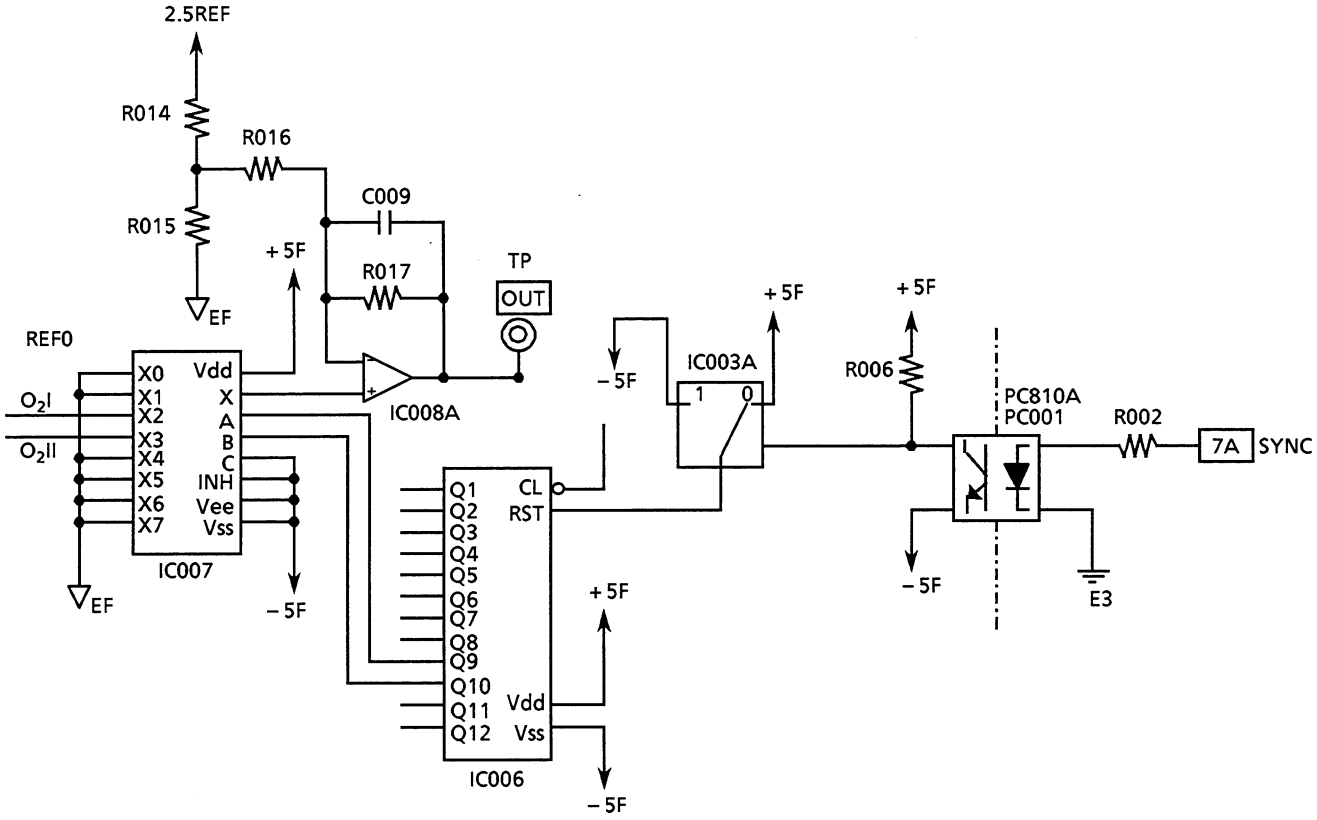


Voltage generated by the O_2 sensor in proportion to O_2 density is inputted to the IC009 through the D007 and D008 protective diodes and low-pass filter composed of R018 and C010. This low impedance signal is outputted to the multiplexer.

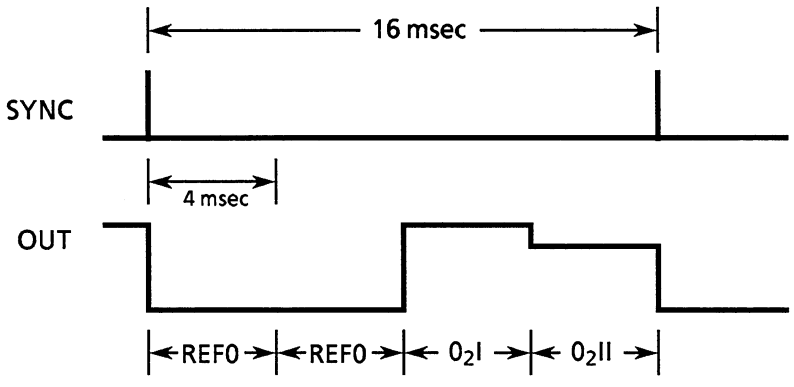
The VR001 is for offset adjustment of IC009 buffer amplifier. When the IC009 is replaced, VR001 adjustment is required.

- **Output signal timing**

Time-shared output signal is amplified and transmitted by a circuit shown below.



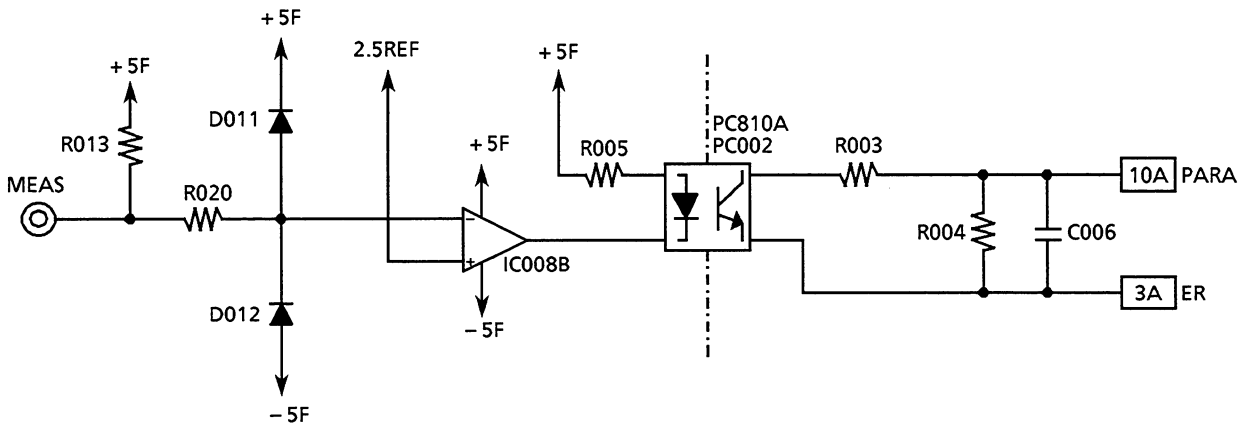
Multiplexer IC007 outputs Ref0, O_2I and O_2II signals in the timing below by the control signal from IC006 counter.



Multiplexed output signal is 35 times amplified with IC008A and level shifted (output is -4.8 ± 0.25 V when input is shortened) and then transferred to a modulation circuit.

Refer to the pages for BP head amplifier output signal modulation and demodulation of descriptions for timing from floating area to the non-floating area.

• Unit discrimination signal (PARA voltage)



PARA (parameter) voltage changes when the O_2 sensor is connected and disconnected as below.

Sensor	PARA voltage (V)
Connection	0.45 ±0.02
Disconnection	0.40 ±0.02

When the sensor is not connected, IC008A comparator output is LOW level. With this voltage, the photocoupler PC002 is conductive and 0.4 ± 0.02 V voltage attenuated with R003 and R004 resisters appears as PARA voltage at no sensor connection.

When the sensor is connected, comparator output is HI. With this voltage, PC002 becomes off and 0.45 ±0.02 V appears as PARA voltage at sensor connection.

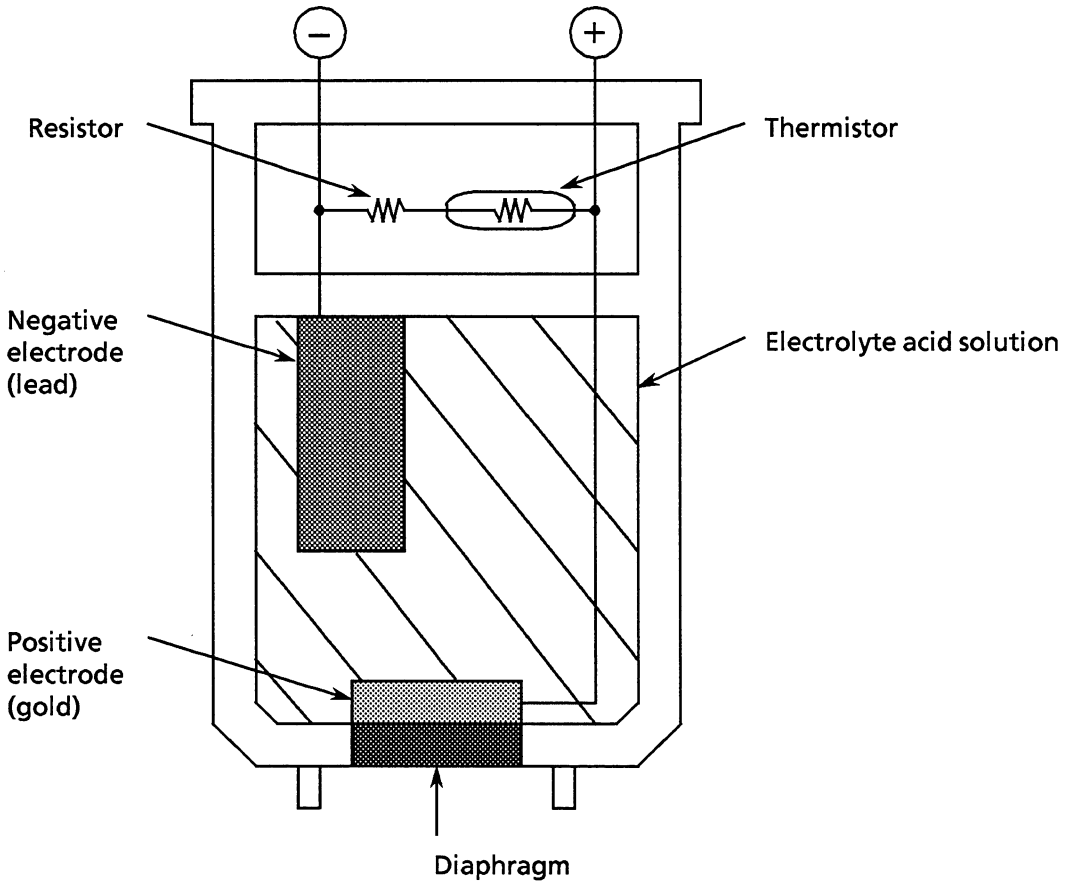
◆ OS-1000 O_2 Sensor (AIKA, Japan)

• Measuring principle of O_2 and construction of the O_2 sensor

As figured, O_2 sensor is an oxygen-lead battery composed of gold as positive electrode, lead as negative electrode and special electrolyte acid solution.

Oxygen in O_2 measurement atmosphere diffuses to gold electrode through a non porous fluororesin diaphragm and deoxidized by electrolysis and current which is proportional to oxygen density flows in the electrodes.

Voltage across a resistor and a thermistor for temperature compensation serially connected is obtained to measure oxygen density.



• Life time of the O_2 sensor

The O_2 sensor has a life time as it is an oxygen battery which generates voltage in response to oxygen in atmosphere. Life time depends upon oxygen density of measuring gas. The higher oxygen density, the shorter life time of the O_2 sensor.

It is not sure to define life time of the O_2 sensor as measurement will be done with various oxygen density.

End of life of the O_2 sensor means that the sensor does not generate voltage which is high enough for O_2 measurement.

Figure on the next page shows relation between oxygen density and output voltage of O_2 sensor model OS-1000, a product of AIKA, Japan. When O_2 sensor is exposed in oxygen for a long time of period, slope of the output voltage curve becomes small.

Nihon Kohden O_2 measurement is designed to define the end of life of the O_2 sensor when output voltage corresponding to that of 100% oxygen shows less than 35mV.

When an exhausted sensor is used, measurement error goes out of specified normal range. When such condition is detected at calibration, message "INOP" (inoperative) is displayed on the screen and "CAL??" remains on the screen without measurement.

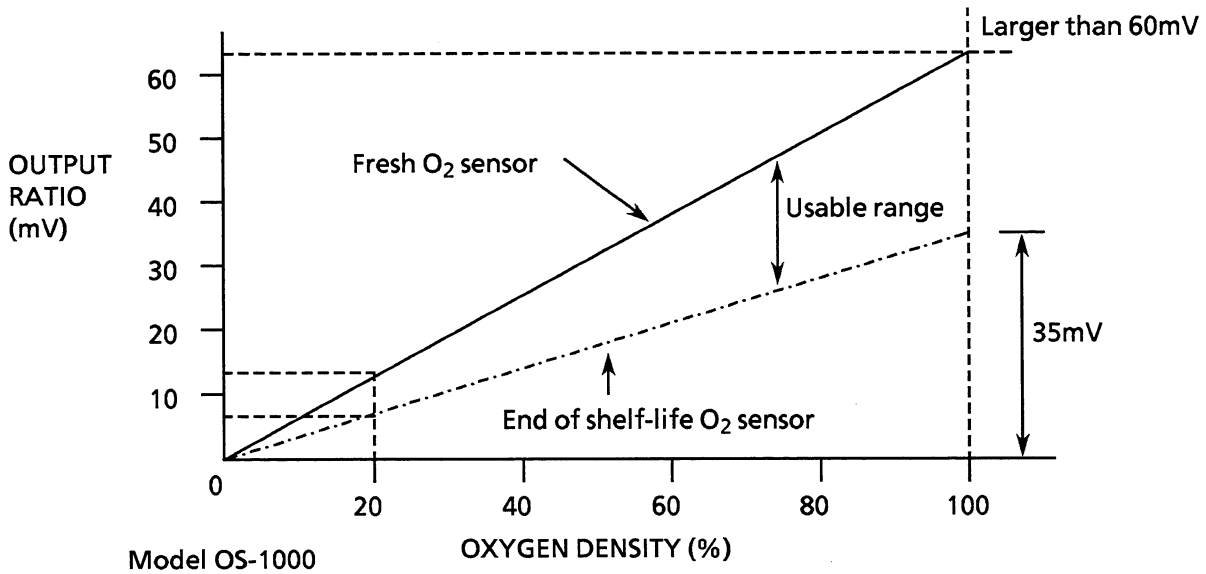
It is estimated that life time of the O_2 sensor is three to five years.

• Precautions when handling the O_2 sensor

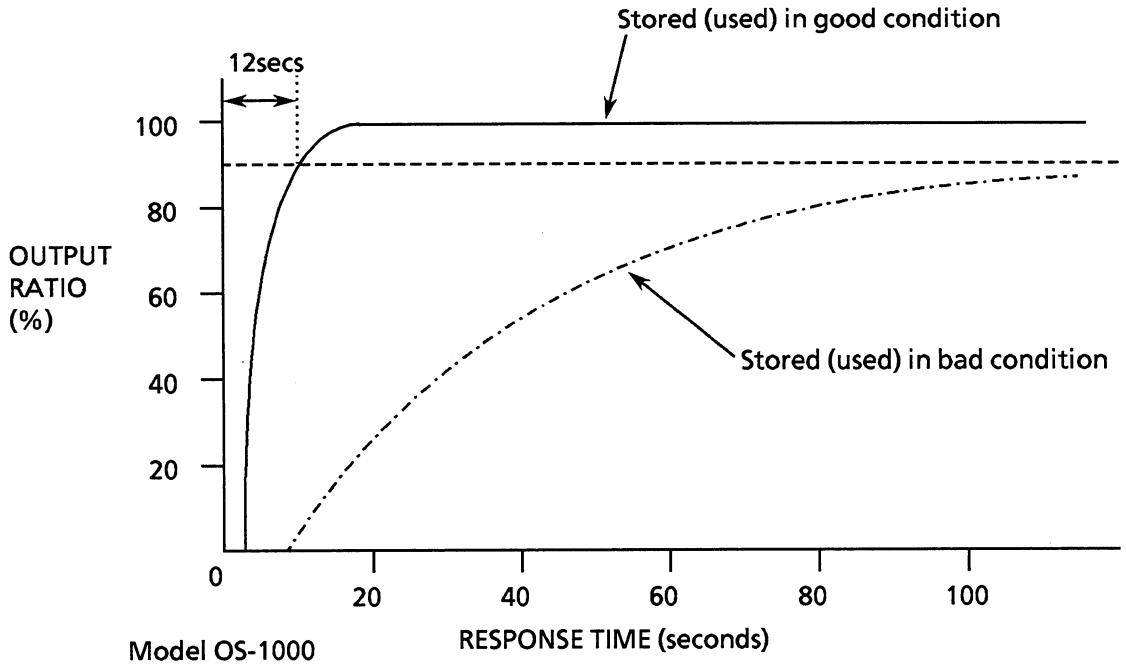
In order to avoid influence by pressure change inside the sensor due to change of atmospheric pressure, gas is filled in the sensor chamber. Therefore, when sensing part is located upwards, gas bubble will be placed on the diaphragm or electrode which will prevent electrolysis inside the chamber and correct data cannot be obtained.

Be sure to put the sensor so that the sensing part is facing downwards for correct measurement. When storing the O_2 sensor, it is recommended to put the sensing part downwards.

If the sensing part is kept upwards it takes several minutes for the sensor to become stabilized before calibration. Be sure to calibrate the sensor after several minutes.



Model OS-1000



Model OS-1000

3-4-10 NIBP Head Amp (AP-860PA), UP-0629 & UP-0630

◆ General

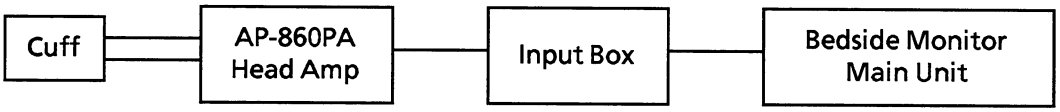
AP-860PA is one of the two types of head amplifiers for the bedside monitor used to measure Noninvasive Blood Pressure (NIBP) of a patient. This head amplifier uses the double air hose method.

NOTE

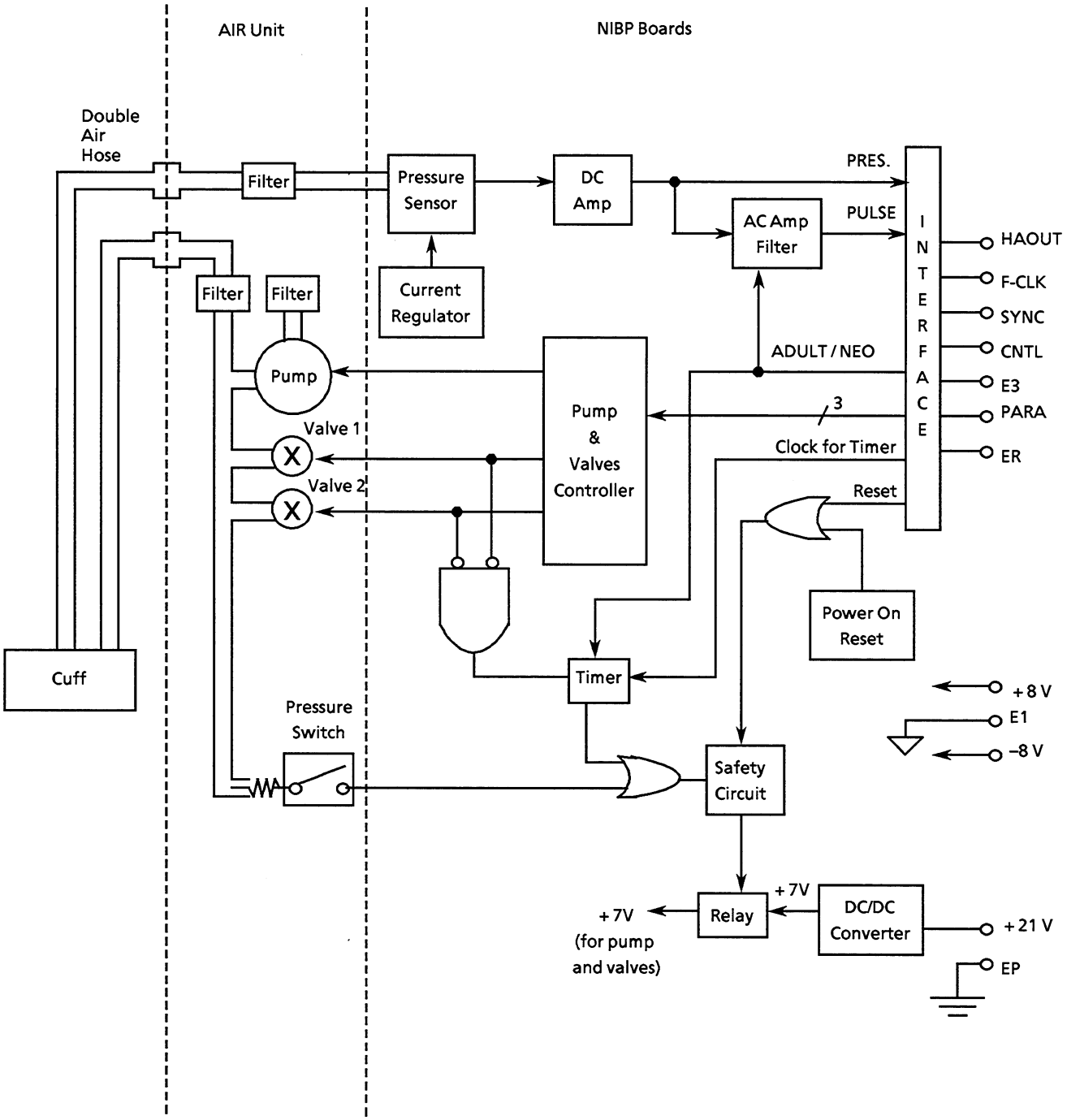
The other type of NIBP head amplifier is the AP-851PA head amplifier. The AP-851PA head amplifier uses the single air hose method.

◆ System Connection

NIBP head amplifier is inserted into the input box of the bedside monitor and the dual air hose is connected to the two NIBP sockets.



◆ Block Description



• AIR Unit, SG-001P

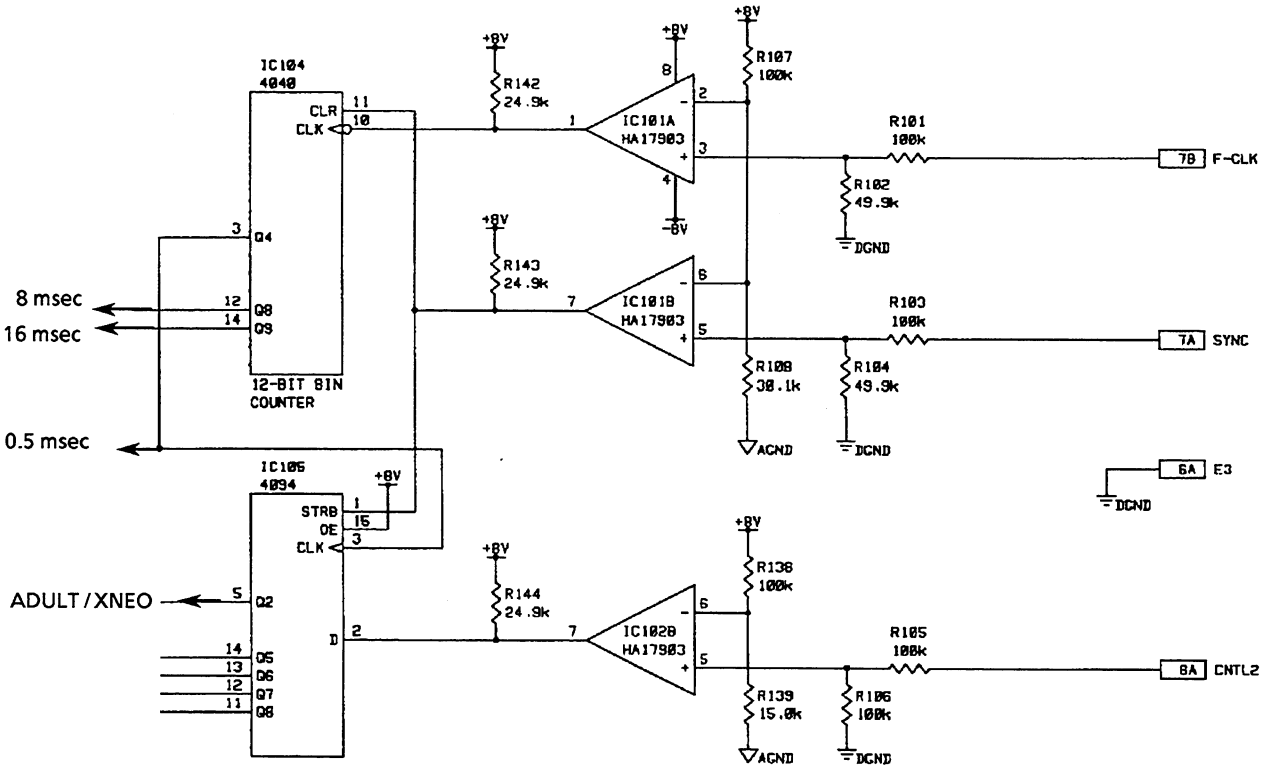
This unit consists of the pump, solenoid valves, and over pressure control switch.

• NIBP boards

There are two boards in the NIBP head amplifier unit, NIBP Main board, UP-0629, and NIBP Sub board, UP-0630. The main unit of the bedside monitor controls the NIBP Main board. The main function of the NIBP Main board is to control the pump and solenoid valves through the time limiter circuit, pressure circuit, and safety circuit. The main function of the NIBP Sub board is to regulate the current supply to the pressure sensor, process the pressure and pulse signals, and finally multiplex all the signals from both the boards before sending it to the bedside monitor.

The DC/DC converter supplies the power to the NIBP Main and Sub boards and the AIR unit.

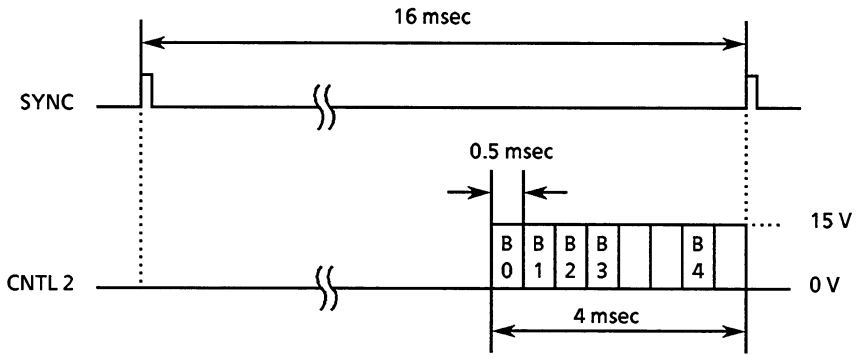
◆ Control Circuit (NIBP Main Board, UP-0629)



The signal level of the input signals, F-CLK, SYNC, and CNTL2, from the input box is within the range of 0 ~ 15 V. The comparators IC101 and 102 change the signal level of these input signals to ±8 V.

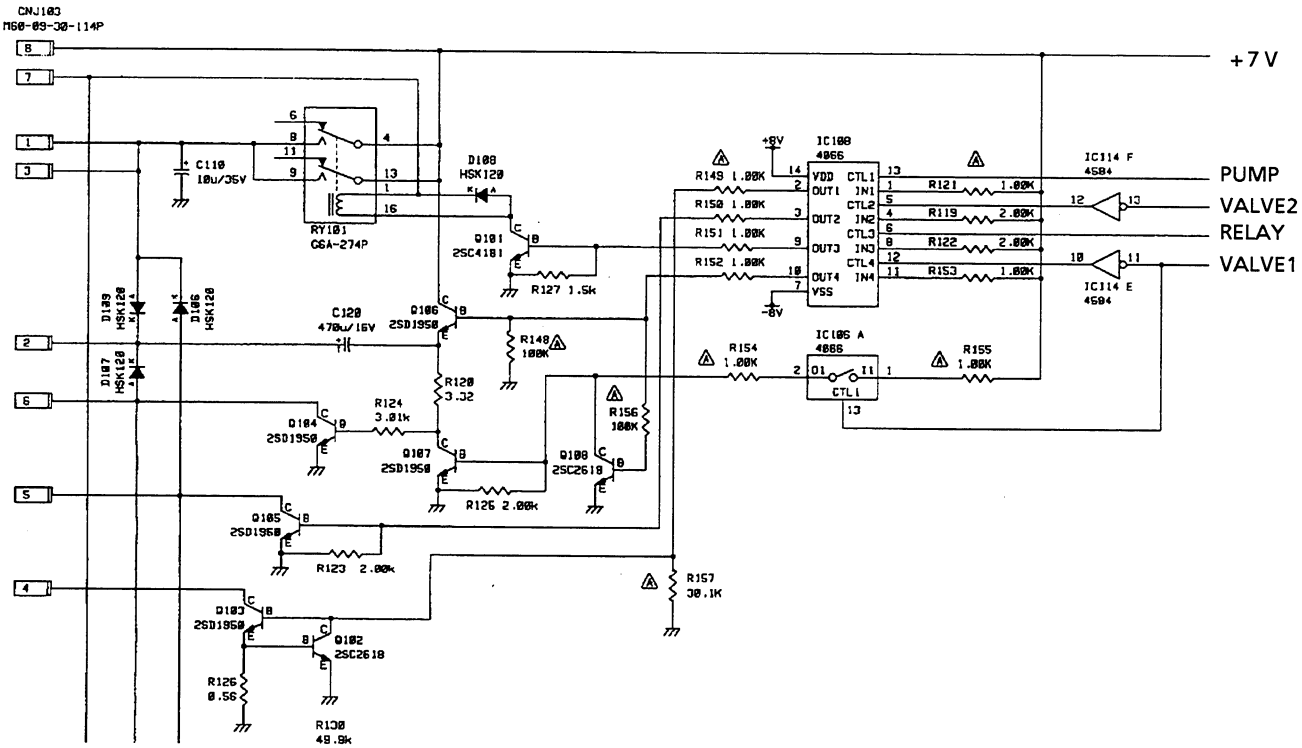
The 64 kHz F-CLK signal is then counted by counter IC104 to give 0.5 msec, 8 msec, and 16 msec timing signals. The analog switch IC106 shunt the 8 msec or 16 msec timing signal to the timer IC109 of the safety circuit. The status signal, ADULT/XNEONATUS, controls the analog switch IC106. In the adult mode, the analog switch shunt the 16 msec timing signal to the safety circuit, and in the neonatal mode, the switch shunt the 8 msec timing signal. The 8 msec and 16 msec timing signals are also output to the multiplexer IC208 of the NIBP Sub board.

The 0.5 msec timing signal in the serial to parallel converter IC105 chops the serial CNTL2 signal into parallel output. The SYNC signal provides the synchronizing signal for the serial to parallel converter. The serial to parallel conversion of the CNTL2 signal is shown below.



Bit	Description	1 (High)	0 (Low)
B0	Pump	On	Off
B1	Valve 1	Close	Open
B2	Valve 2	Close	Open
B3	Inst	On	Off
B4	Adult/Neonatal	Adult	Neonatal

◆ Relay, Pump, and Solenoid Valves Controller Circuit (NIBP Main Board, UP-0629)



The safety circuit controls the relay RY101. The relay RY101 switches on or off the +7 V power supply from the DC/DC converter to the pump and solenoid valves in the AIR unit through connector CNJ103.

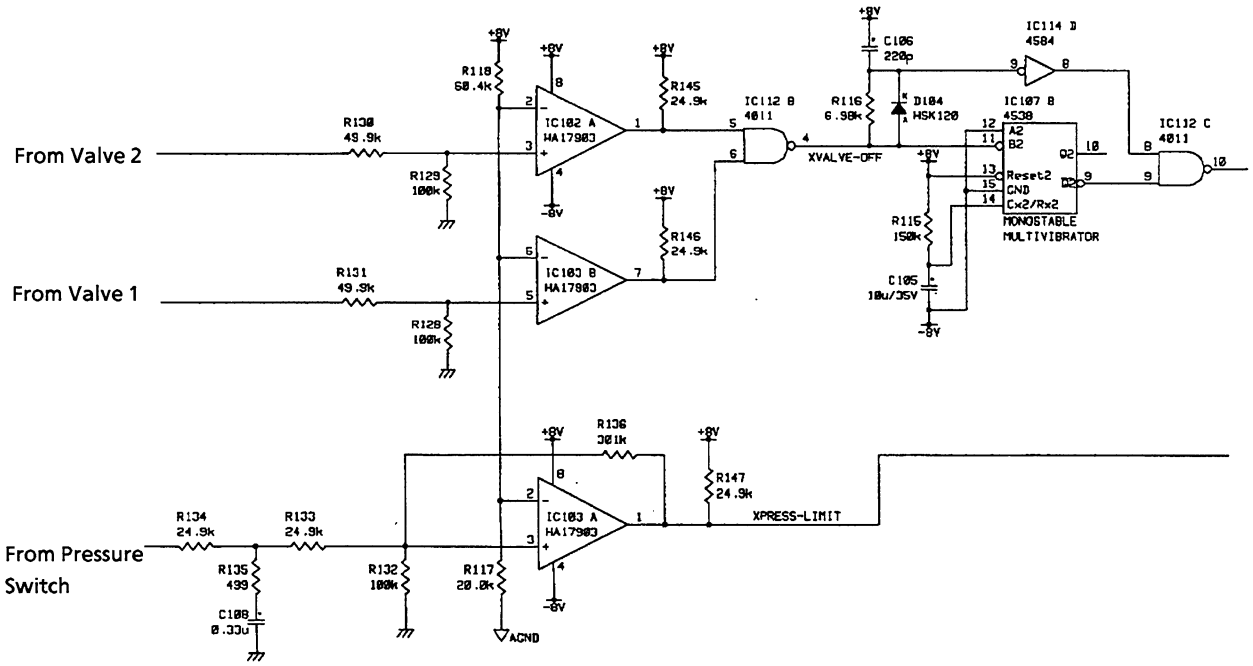
The parallel output signals from the IC105 control the pump, solenoid valves by switching on and off the transistor Q101 ~ 108.

◆ Safety Circuit (NIBP Main board, UP-0629)

The Main unit controls this circuit, but, this circuit can also operate independently under the following conditions:
1) When the cuff pressure exceeds 300 mmHg.
2) When the measuring time exceeds 120 seconds for adult and 60 seconds for neonatal.

The safety circuit has two major blocks, namely the comparator block and the timer, latch, and reset block.

a) Comparator Block

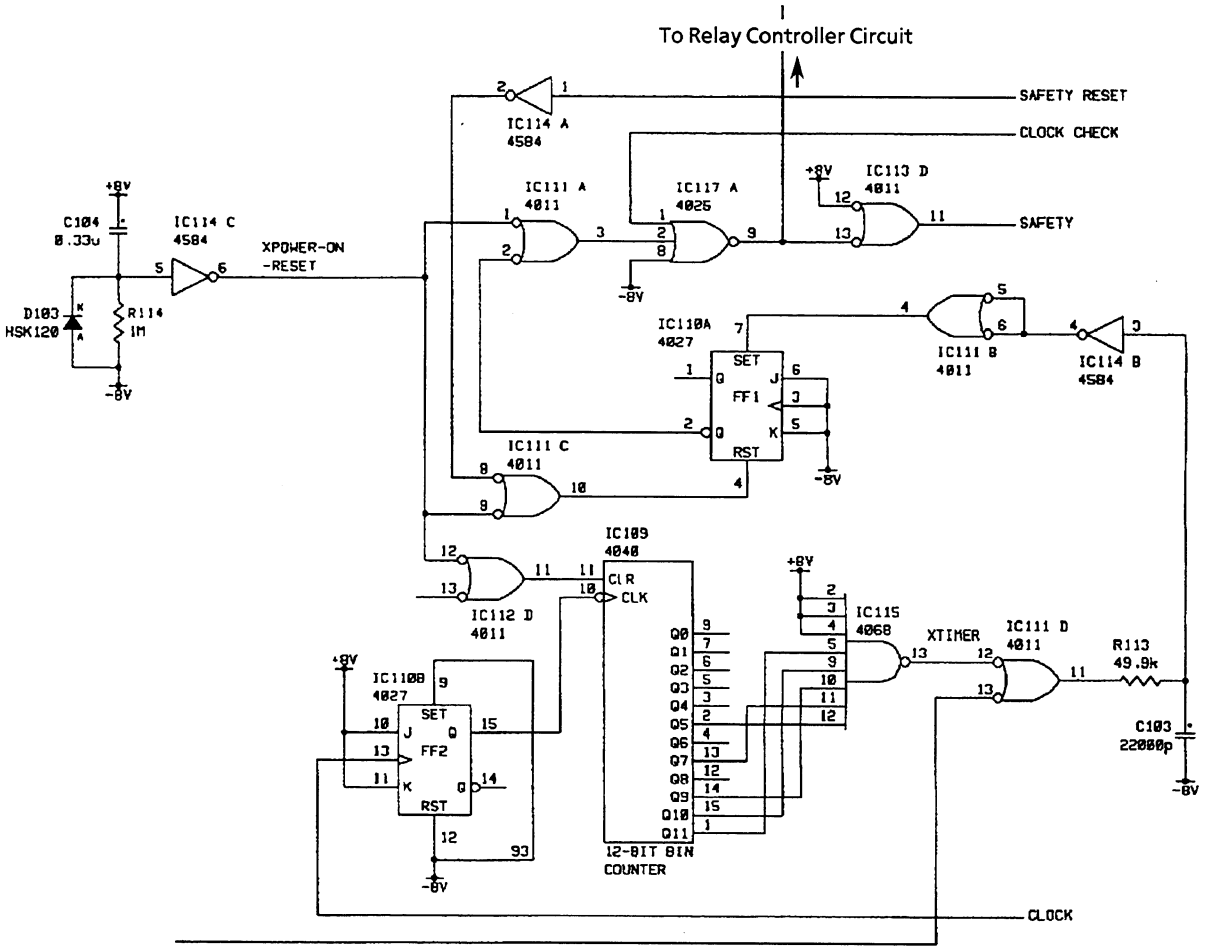


The comparators IC102 and 103 change the signal level of the input signals from the solenoid valves and pressure switch. When both of the solenoid valves are opened, the output of IC112 is set to low (−8 V). This low signal is used to reset the counter of timer circuit.

This NIBP head amplifier uses the step deflation method and this caused the solenoid valves to open and close repeatedly. This opening and closing of the solenoid valves can clear the timer circuit. To prevent this from happening, the monostable multivibrator IC107 treats the approximately 1.5 seconds of the period when the valve is opened as the period as if the valve is closed.

The pressure switch set the output of IC103 to low (−8 V) when the cuff pressure exceeds 300 mmHg.

b) Timer, Latch, and Reset Block

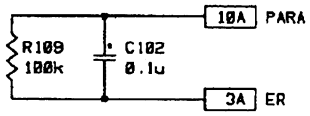


When the solenoid valves are closed during the NIBP measurement, the comparators output a high signal to the timer circuit (IC109 and IC115). A low input signal causes the timer circuit to start counting. Depending on the type of clock signal (adult mode, 16 msec; neonatal mode, 8 msec), the timer output a high signal at the pin-11 of IC111 if the solenoid valves are closed for more than 120 seconds in the adult mode or 60 seconds in the neonatal mode. A high output signal from the timer circuit causes the latch IC110 to output a low signal that finally causes the output of pin-9 of IC117 to go low. A low signal at pin-9 of IC117 switches off the relay RY101, which in turn stops the +7 V power supply to the pump and solenoid valves in the AIR unit.

The reset signal from the main unit and the power on reset signal from the power on reset detector circuit can also set the pin-9 of IC117 low through latch IC110.

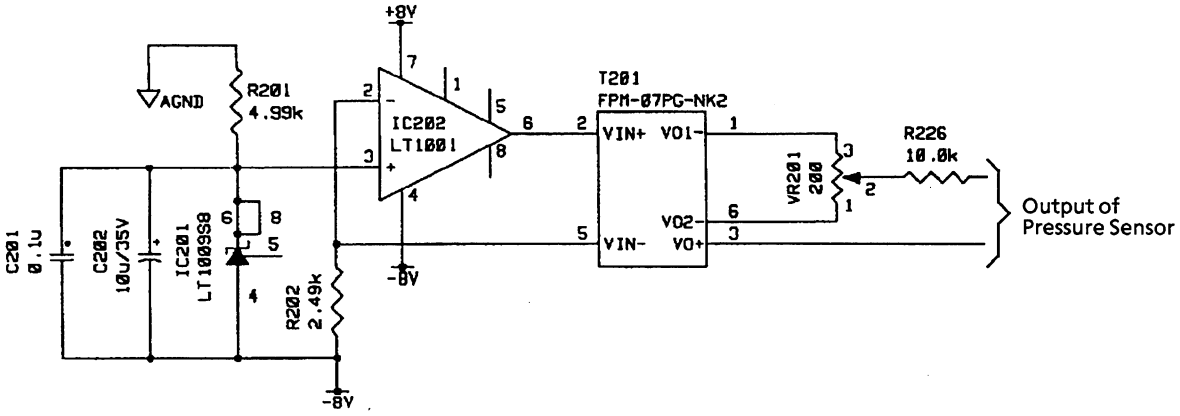
The status of this safety circuit is output to pin No. 6 of connector CN104 to the NIBP Sub board through analog switch IC106. A low output from the pin No. 6 of connector CN104 shows that the safety circuit is in operation.

◆ PARA Signal (NIBP Main board, UP-0629)



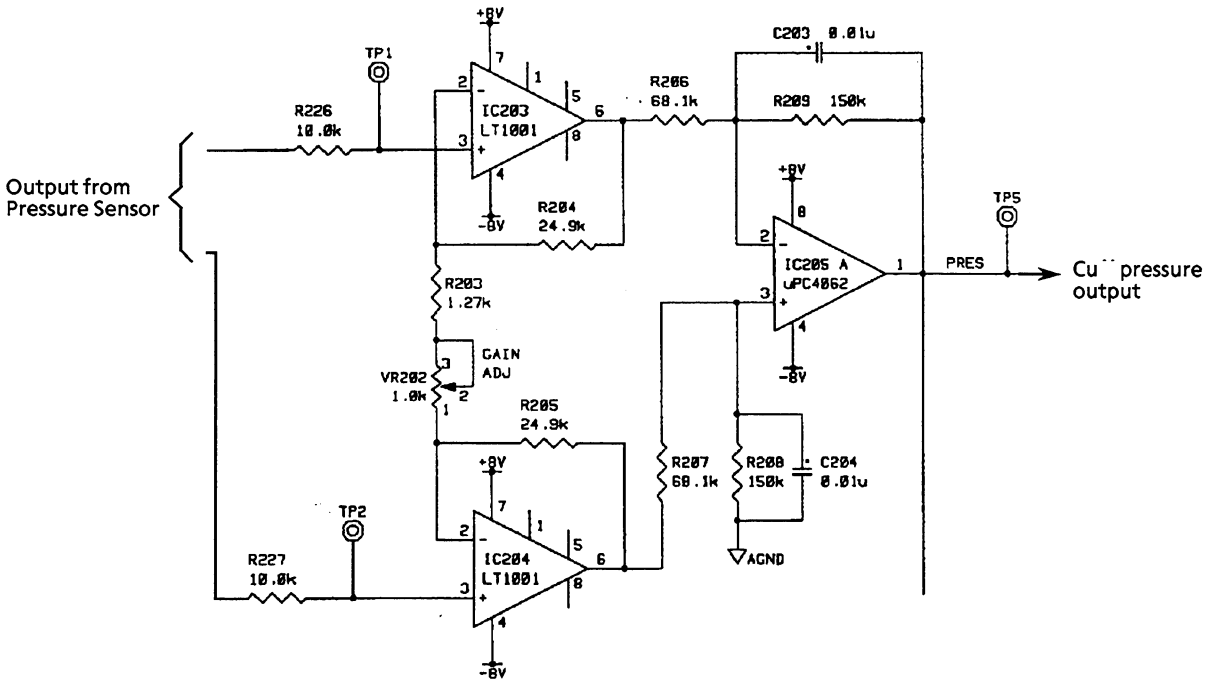
The PARA signal for the NIBP head amplifier has a fixed voltage of 4.55 V. This PARA signal is the NIBP head amplifier AP-860PA's identification signal for the main unit of the bedside monitor.

◆ Cuff Pressure Sensor Circuit (NIBP Sub Board, UP-0630)



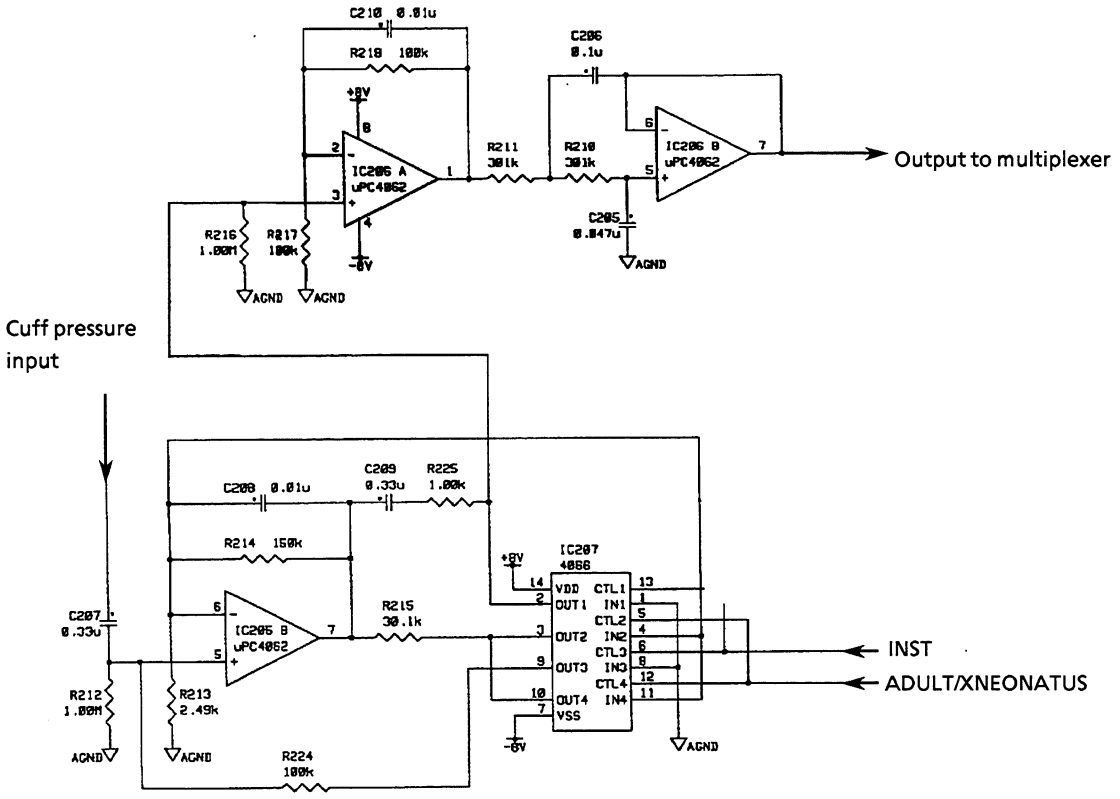
This circuit is based around the cuff pressure sensor T201. A 2.5 V Zener diode IC201, OP amplifier IC202, and resistor R202 supply a constant regulated current to the cuff pressure sensor T201. The cuff pressure sensor T201 varies the output voltage according to the pressure in the cuff. The variable resistor VR201 is used to zero adjust the cuff pressure sensor T201.

◆ Cuff Pressure Voltage Amplification Circuit (NIBP Sub Board, UP-0630)



This circuit, consisting of IC203 ~ 205, amplifies the cuff sensor output voltage about 60 times and outputs the amplified signal to the oscillating cuff sensor output voltage amplification and filtering circuit. It adjusts the sensitivity of the cuff sensor output voltage to 100 mmHg/1 V through sensitivity volume of the variable resistor VR202.

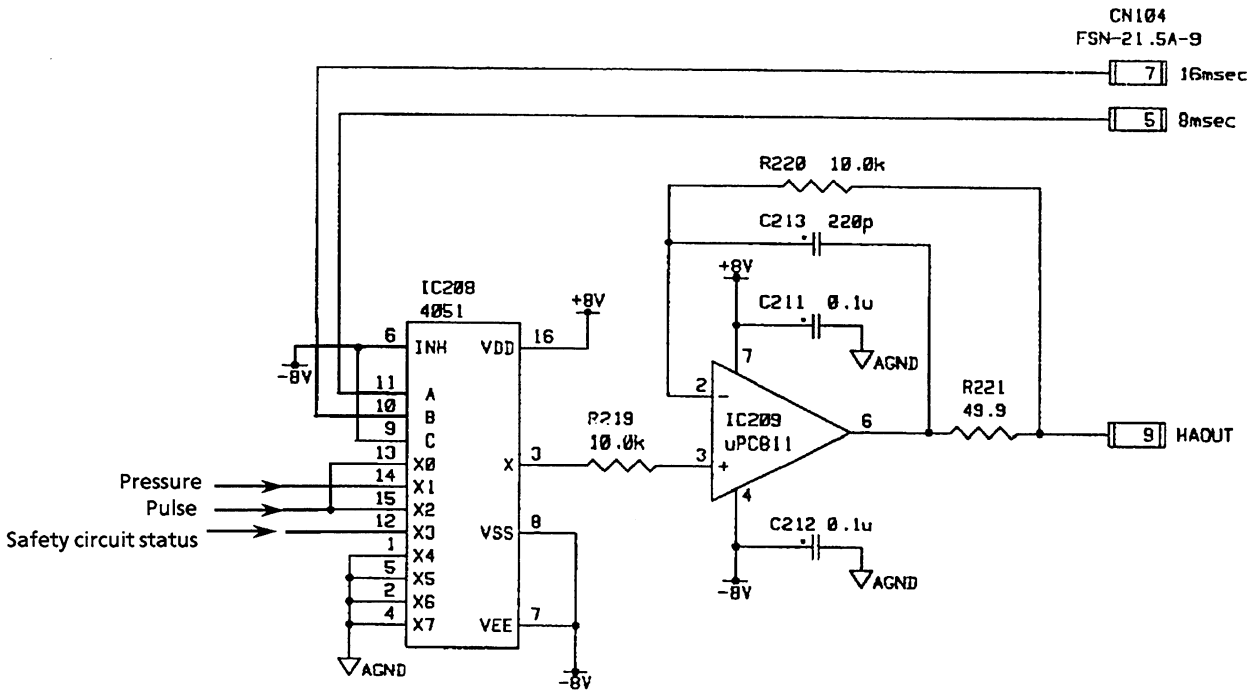
◆ Oscillating Cuff Sensor Output Voltage Amplification and Filtering Circuit (NIBP Sub Board, UP-0630)



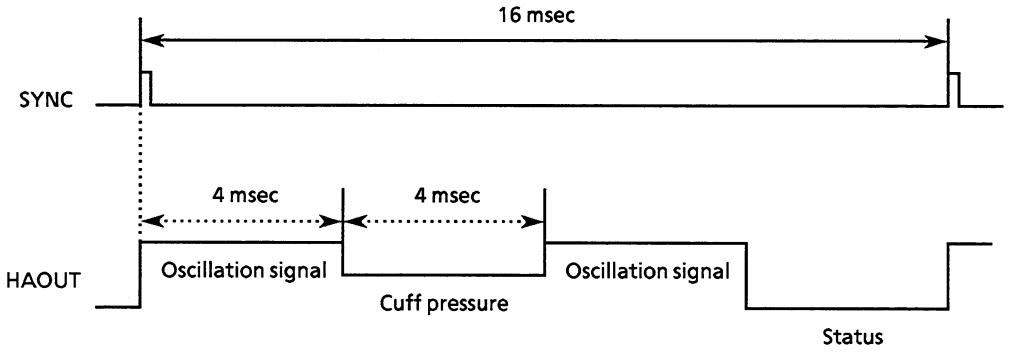
NIBP measurement using the occlusive-oscillometric method gives an oscillating pressure reading during the measurement. This circuit amplify and filter this oscillating cuff sensor output voltage signal and output the final signal to the multiplexer IC208.

This circuit consists of two level low cut filter with 0.3 second time constant block (C207, R212, C209, and R216) and a 7.5 Hz high cut filter block (R210, R211, C205, C206, and IC206). In the adult mode, IC205 and 206 amplify the signal about 22 times, and in the neonatal mode, IC205 and 206 amplify the signal about 122 times.

◆ Multiplexer Circuit (NIBP Sub Board, UP-0630)



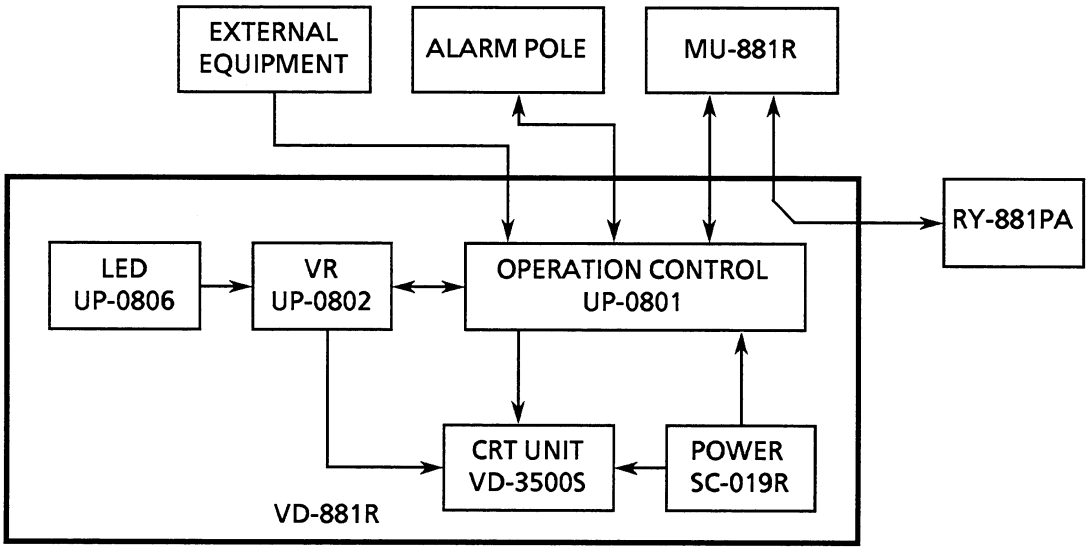
This multiplexer circuit IC208 uses the timing signals (8 msec and 16 msec) from the NIBP Main board to time-share the cuff pressure output voltage signal, oscillation signal, safety circuit status signal into the HAOUT signal. The timing of the final output signal is shown below.



3-5 Display Unit, VD-881R

3-5-1 General

◆ **Block Diagram**



The Display unit consists of the following sub-unit:

• OPERATION CONTROL Board, UP-0801

The two 1 chip CPUs (IC201, 204) on this board control the display unit. They communicate with the bedside monitor main unit via the RS-232C interface. This board also controls the sound, video, power supply, and alarm pole. The signal from the remote control is processed on this board too.

• OPERATION (VR) Board, UP-0802

This controls the sound volume, brightness, and contrast.

• LED Board, UP-0806

This board receives the remote control signal and relay it to the OPERATION CONTROL board via the OPERATION (VR) board.

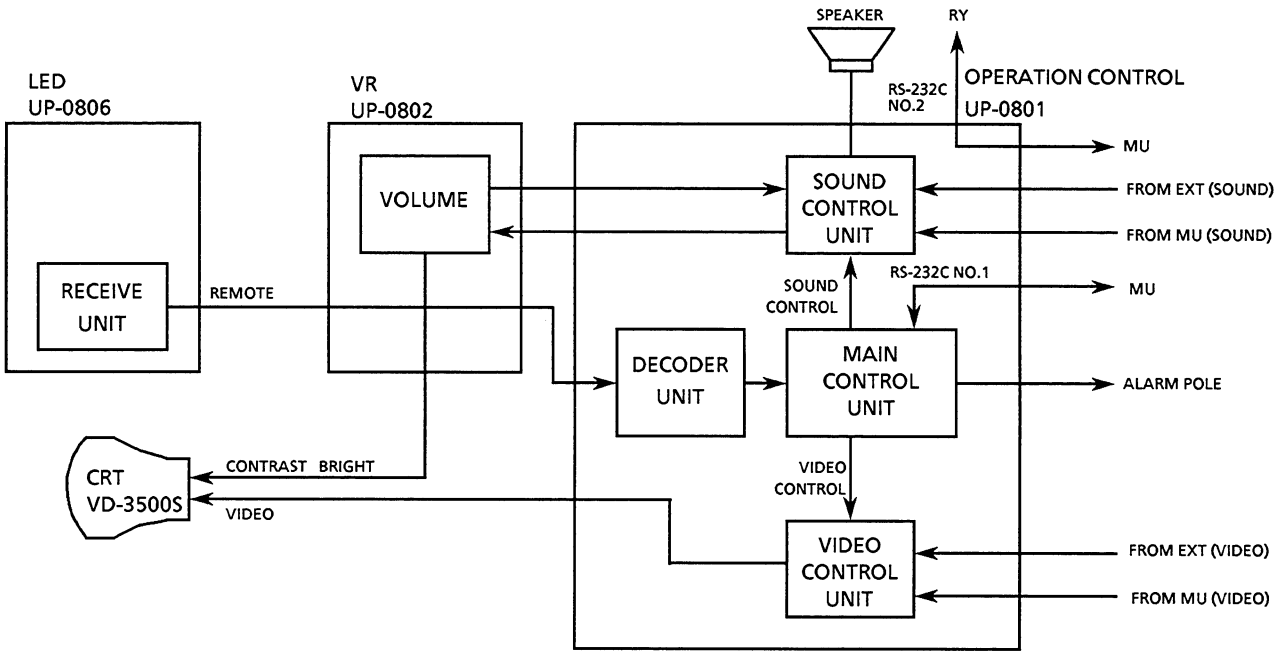
• CRT Unit, VD-3500S

This is a 14 inches three mode scanning color monitor.

• Power Supply Unit, SC-019R

This supplies the power for the video display unit.

◆ Signal Flow



• Remote Control Signal

The light sensor on the LED board receives the light signal from the remote control. The sensor sends the signal to the OPERATION CONTROL board via the OPERATION (VR) board. The OPERATION CONTROL board decodes the signal and then sends it to the bedside monitor main unit via the RS-232S.

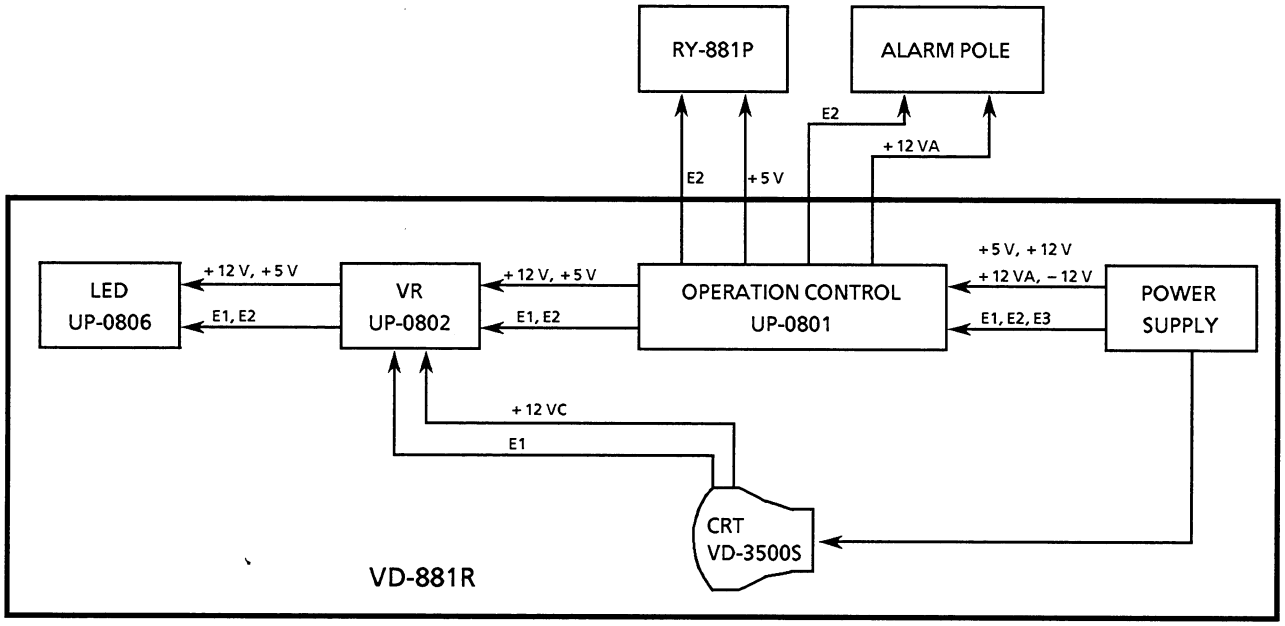
• SOUND Signal

The OPERATION CONTROL board receives and selects the sound signal from the bedside monitor main unit or the external unit. The OPERATION CONTROL board then sends the SOUND signal to the VR board for processing before returning it to the OPERATION CONTROL board. The processed SOUND signal is inputted into the speaker unit via the power amplifier.

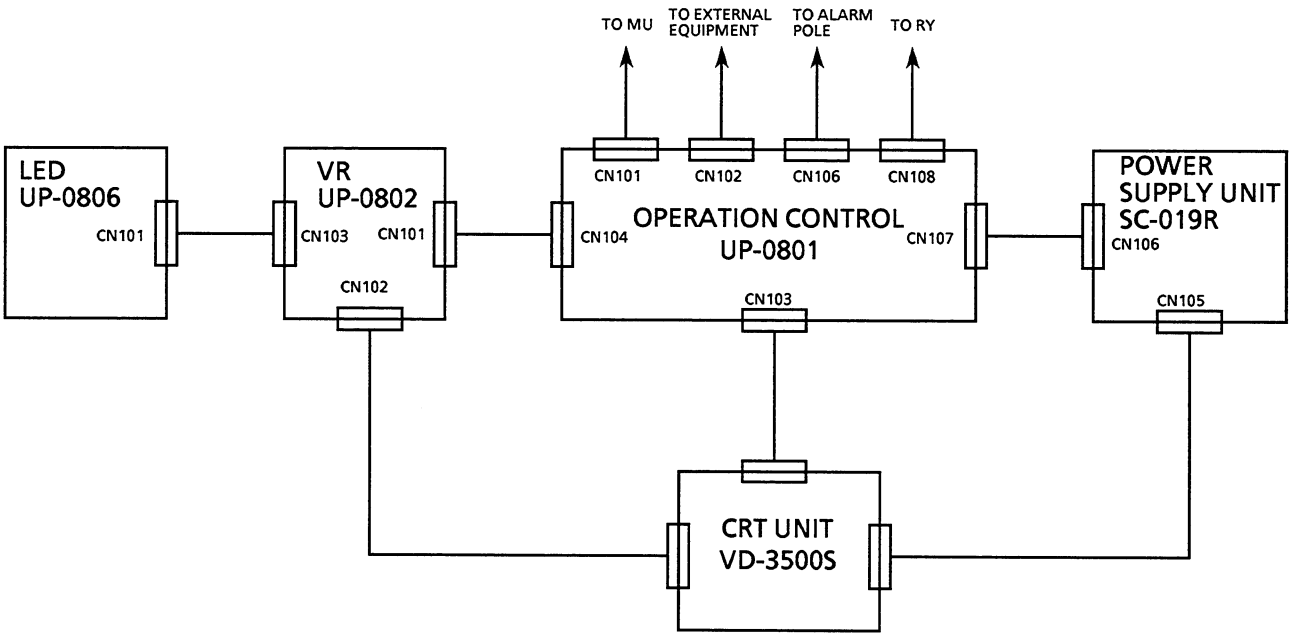
• VIDEO Signal

The OPERATION CONTROL board receives and selects the VIDEO signal from the bedside monitor main unit or the external unit.

Display Unit Power Supply Block Diagram

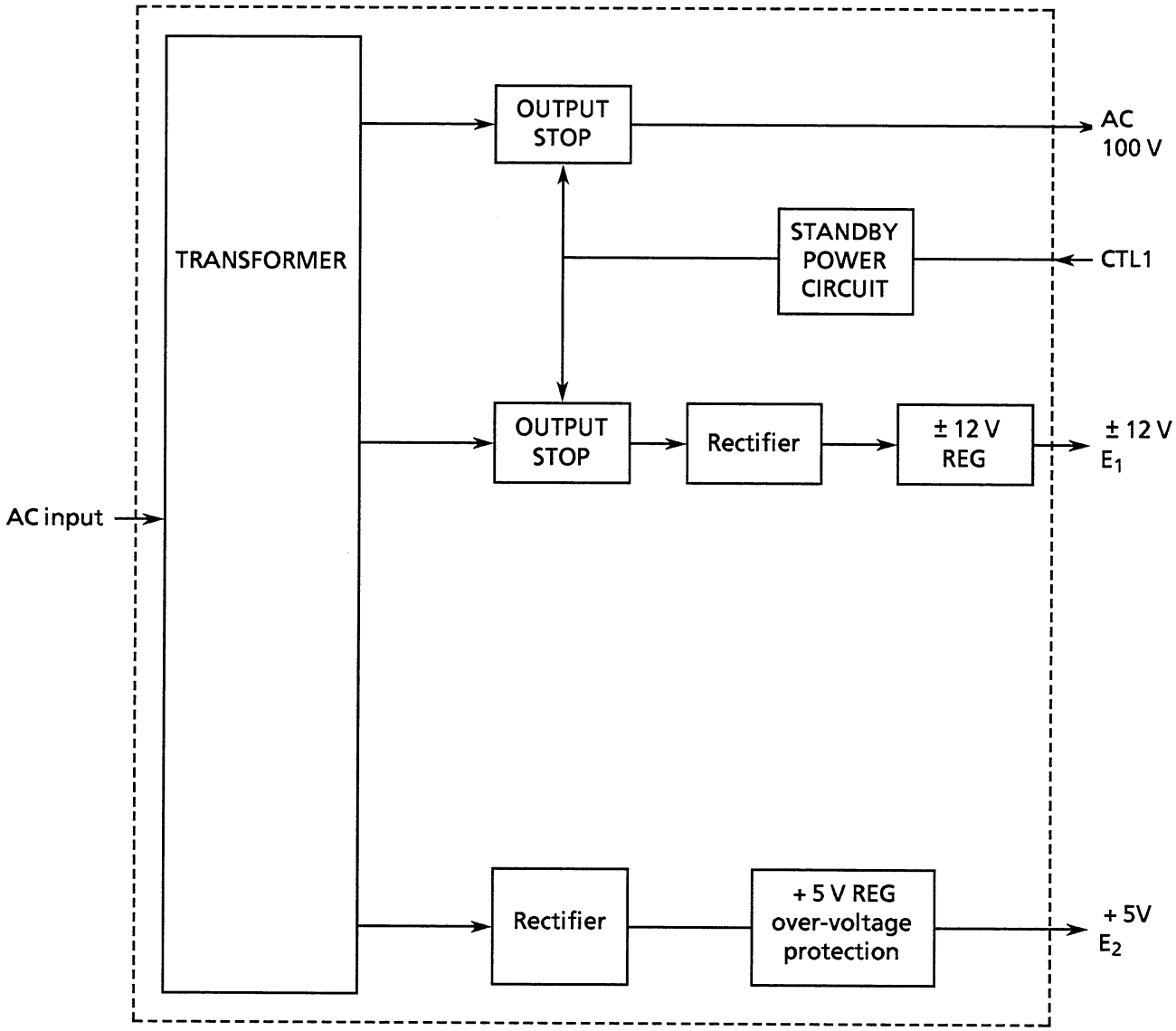


Display Unit Connection Diagram



3-5-2 Power Supply Unit, SC-019R

Block Diagram



◆ General

This unit consists of the transformer sub-unit and the regulator sub-unit. The regulator sub-unit also performs as a rectifier as well as an overvoltage protector.

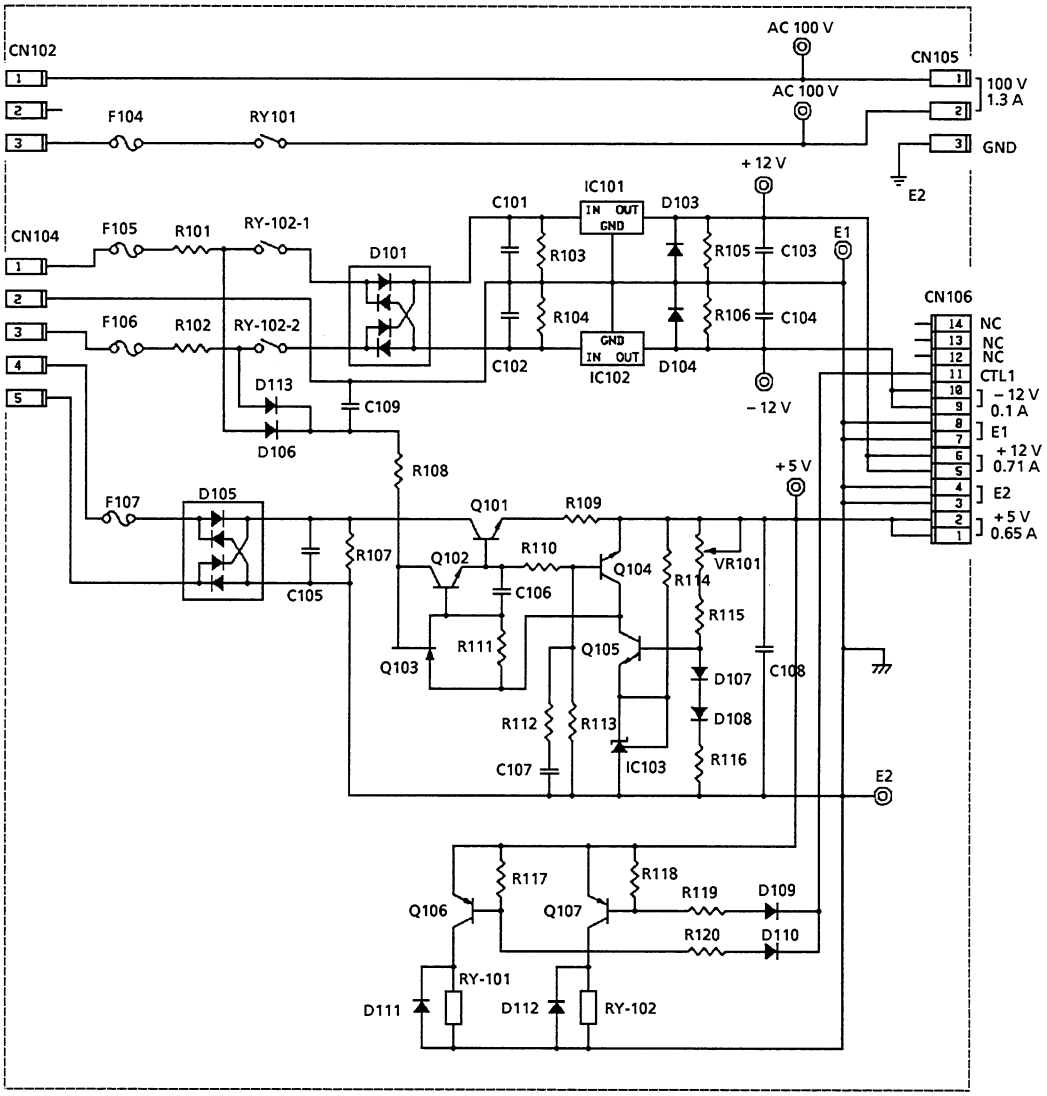
This regulator sub-unit consists of the following circuit:

* +5 V Regulating Circuit
* CTL1 Signal Circuit
* ±12 V Regulating Circuit
* AC 100 V Output

The various power voltage are used and processed as follow:

Voltage	Processing Method	Use
+5 V	Dropper	Digital circuit
±12 V	3 point regulator output	Analog circuit
AC 100 V		CRT unit

◆ Circuit Description



◆ + 5V Regulating Circuit

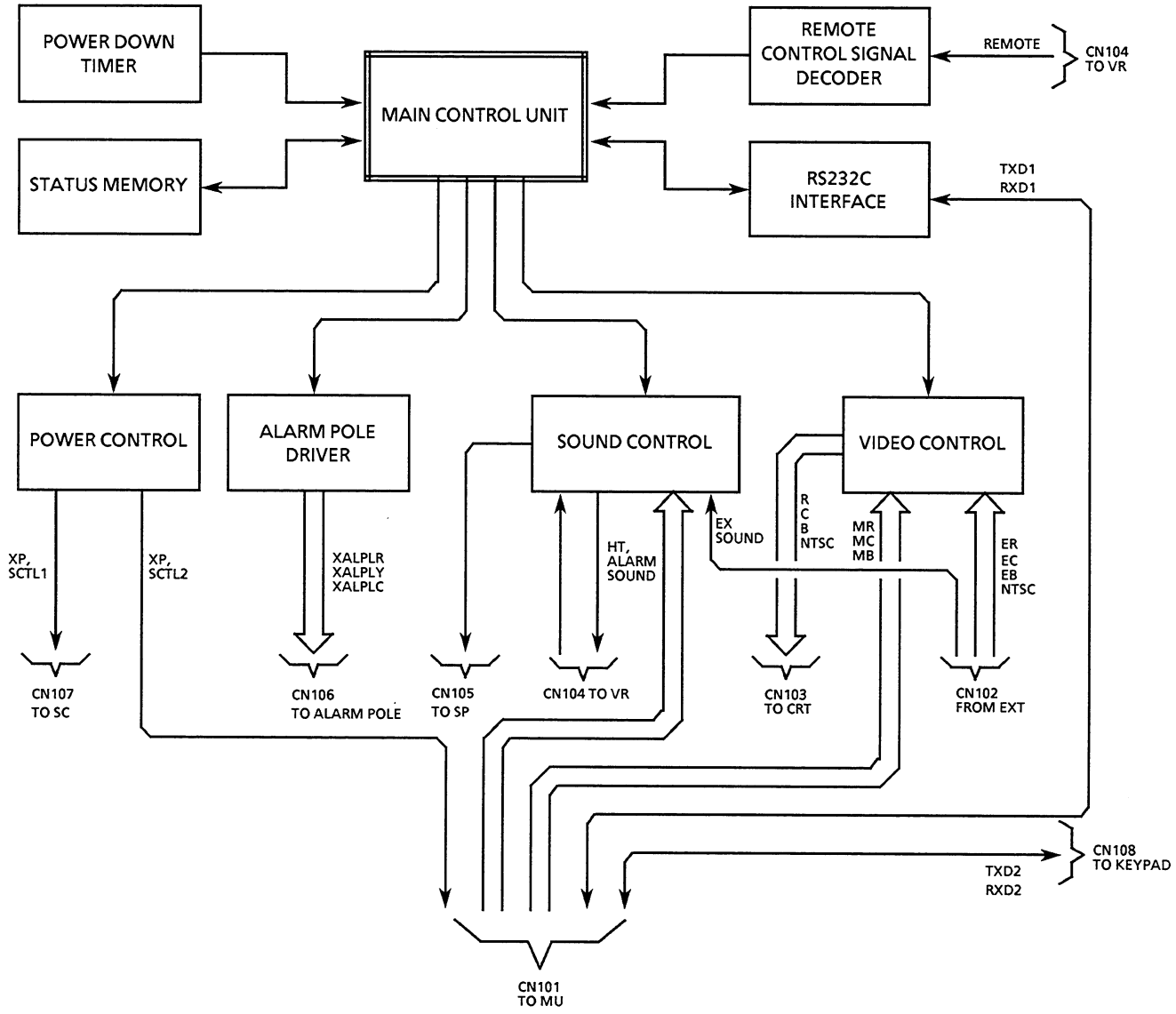
The transistor Q104 is the overvoltage protector. When the output voltage exceeds +5V, Q104 starts to operate since there is a voltage drop across the resistor R109. This decreases the bias of transistor Q101, which in turn decreases the output volatage.

◆ CTL1 Signal Circuit

When the voltage of terminal CTL1 reaches +5V, it switches off the relay RY101 and RY102. This stops the output of the AC 100V and ±12V.

3-5-3 OPERATION CONTROL Board, UP-0801

Block Diagram

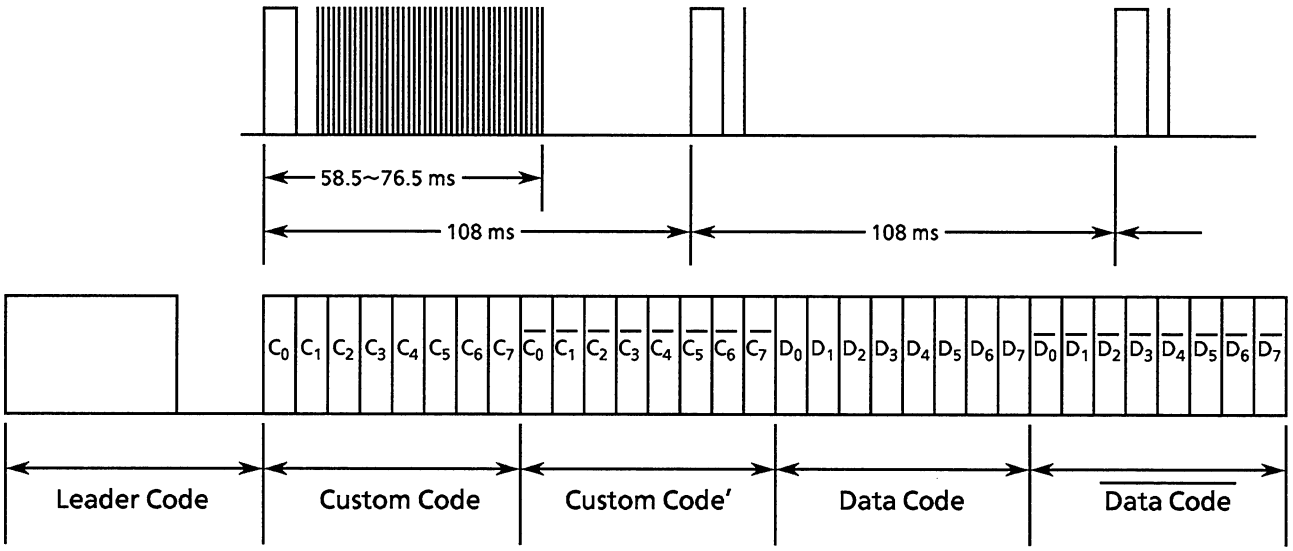


◆ Infra-red Remote Control Receiver Unit

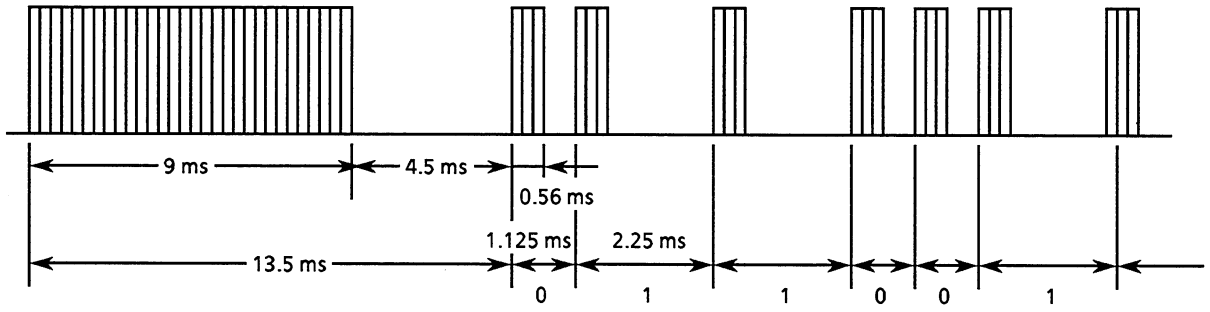
• Format of Remote Control Signal

The remote control signal consists of the leader code, 16 bits custom code, 8 bits data code and 8 bits complement data code. The 16 bits custom code contains the code for the type of the remote control sending the signal. The data code contains the information of the pressed key on the remote control.

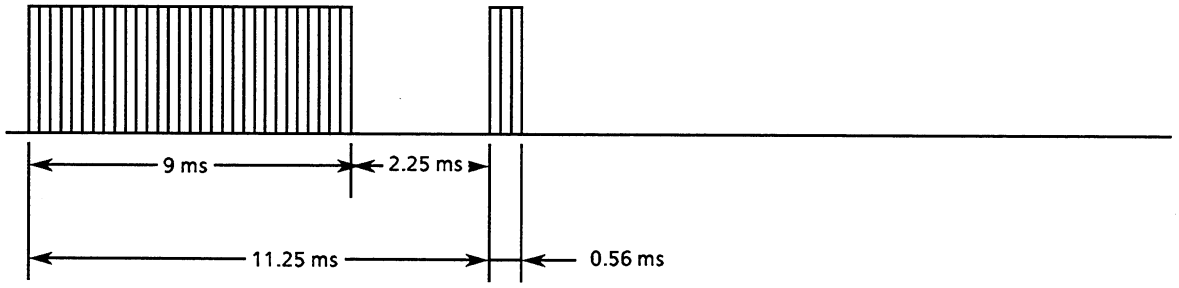
The infra-red remote control signal is transmitted by PPM modulation.



1st time



2nd time (When the key is continuously pressed)



• Remote Control Signal Demodulating Circuit

The 4 bit slave CPU (IC204) demodulates the received signal. If the custom code is correct, the accompanying data of the pressed key is sent, via the serial bus, to the display unit 8 bit master CPU (IC201) for processing.

• Serial Bus Interface

The serial bus interface consists of one serial bus line (SB0) and one serial clock (XSCK) line. The clock frequency is 187.5 kHz.

◆ Power Supply Control Circuit

The function of this circuit is to switch on/off the display unit. This switch is based on the status of the XP.S CTL1 output signal of IC201. The table below shows the logic of the switch.

Selection	XP.S CTL1
Display Power Source OFF	0
Display Power Source ON	1

The XP.S CTL1 exits the OPERATION CONTROL board via Pin No.11 of connector CN107 to the power supply unit. When the terminal becomes LOW, the voltages ±12 V/ +12 V AC, and +5 V are turned on. When the terminal becomes HIGH, only +5 V is turned on.

• Display Unit Power Supply Control

The power supply in the display unit can be controlled by the bedside monitor main unit and the display unit itself. Hence, instructions received from the keypad on the control of the power supply can either be processed in the main unit or the display unit. The operating status of IC201 determines the unit that control the power supply.

The bedside monitor decides the status of the IC201 of the display unit by asserting/negating IC201's status port via its M/S SEL signal. The table below shows the switching process of this decision.

Status port (P23, 30PIN) Input	Operating mode
1 (HIGH)	MASTER
0 (LOW)	SLAVE

–Display Unit as the Controller

The display unit functions as the controller when its IC201 is in the master operating mode. The keypad outputs the power supply control output signal, XP.S CTLIN. IC201 receives the XP.S CTLIN, via its port P21 (pin No. 29) and outputs the power supply control output 1 signal, XP.S CTL1, to the power supply unit via the OPERATION CONTROL board connector CN107.

–Bedside Monitor Main Unit as Controller

When the IC201 of the display unit is in the slave operating mode, it relays the signal to the bedside monitor main unit for further processing. The IC201 receives the XP.S CTLIN via its port P21, but now it outputs the power supply control output 2 signal, XP.S CTL2, to the bedside monitor main unit via the OPERATION CONTROL board connector CN101.

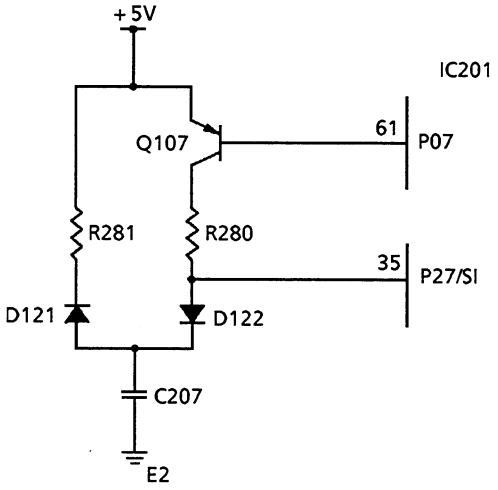
◆ Status Memory

The status memory is based on a Serial In/Serial Out EEPROM (IC206). The function of this status memory is to set the CPU setting back to its last setting prior to any unintentional resetting or power down, software malfunction, and others.

The status memory contains the following information.

* Video input and output switching (INTERNAL/EXTERNAL)
* Video output switching (Separate Sink/Composite Sink)
* Display power supply output control (ON/OFF)

◆ Low Voltage Monitor Timer



This timer monitors the instantaneous loss of power supply in the display unit. During power down condition, the capacitor C207 supplies the back-up power when there is a drop in the +5 V voltage. If the voltage drops to +0 V, the capacitor will discharge its stored electricity for a period determined by resistor R281 and capacitor C207.

When the system is reset after a power down condition, the CPU reads the value of voltage at port P35. If the value is "1", the CPU interprets that the power was on prior to reset, and therefore switches the display power on.

After the power is restored, the CPU writes the instruction to recharge the capacitor. The transistor Q107 redirect the current to the capacitor.

◆ Serial Communication

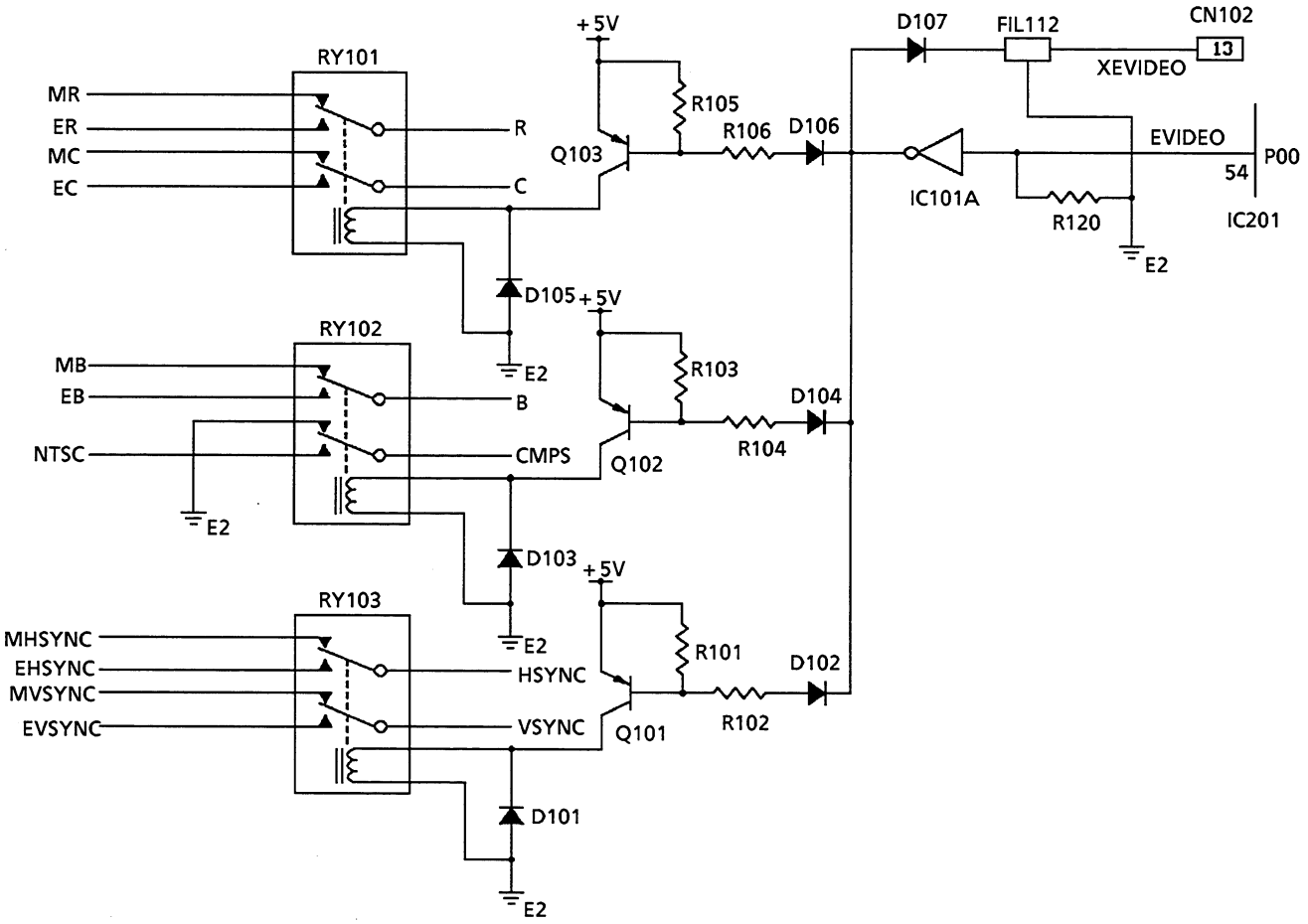
The communication format is as follow:
* RS-232C Communication
* Baud Rate : 4800/9600 BPS (hardware switch)
* Character Length : 8 bits
* Stop Bit Value : 1 bit
* Operation Mode : ASYNC
* Parity : None

The baud rate depends on the value of the CPU input port (P25). When the value is "1", the baud rate is 4800 BPS; when the value is "0", the baud rate is 9600 BPS.

The CPU will begin sending its data when the READY signal is asserted (HIGH).

◆ Video Signal Control

Video Signal Control Circuit



• Main Unit/External Unit RGB Signal Selection

– Software Control

The IC201 on this OPERATION CONTROL board can select the source of the RGB signals. The source can be from the main unit or an external unit. The status of the IC201's EVIDEO signal output determines the selection. The switching process is based on transistors Q101 - 103 and relays RY101 - 103.

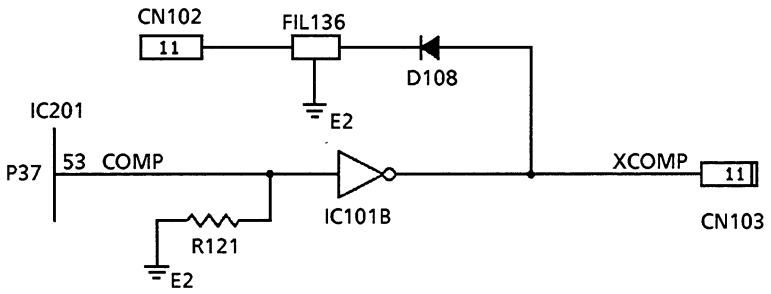
The table below shows the statuses of the EVIDEO signal output and their selections.

Selection	EVIDEO
RGB signal from the main unit	0
RGB signal from external units	1

– Hardware Control

Switching to received the RGB signals from the external unit can also be done through the connection between the OPERATION CONTROL board and the external unit. If the pin No. 13 of connector CN102 is LOW, the same transistor Q101 - 103 and relays RY101 - 103 select the RGB signals from the external unit.

• CRT Unit Operation Mode Selection Circuit



The CRT unit can operate in the RGB mode as well as the NTSC mode. The selection is again by software or hardware control. The status of the XCOMP signal sets the operating mode of the CRT unit. The table below shows the status of the XCOMP and its operating mode settings.

Operation mode	XCOMP
RGB IN	1
NTSC IN	0

– Software Control

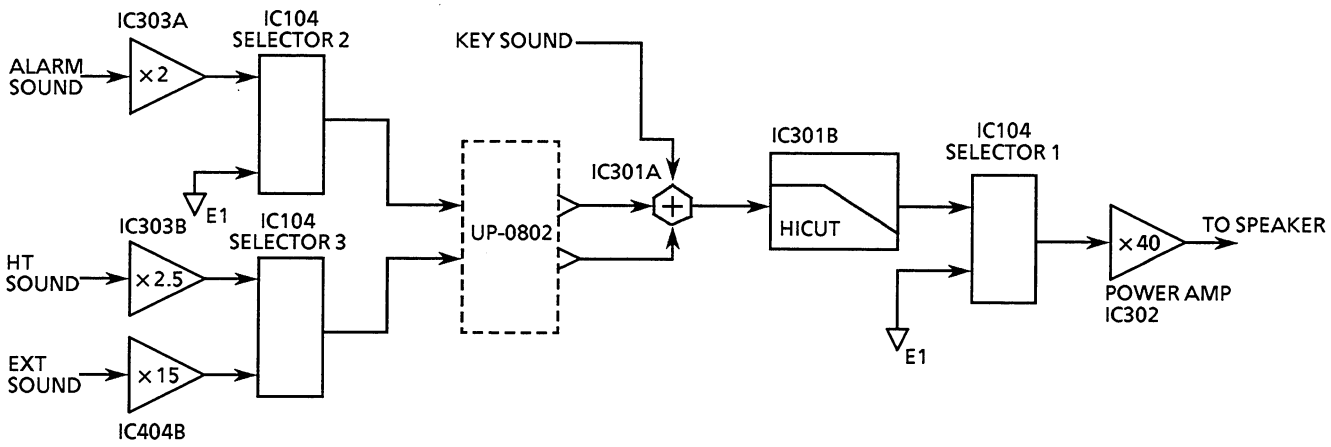
The IC201 outputs the COMP signal through its port P37. The COMP signal is inverted by IC101B, and the resulting signal XCOMP is outputted to the CRT unit via the OPERATION CONTROL Board connector CN103.

– Hardware Control

The status on pin No. 11 of the external unit connector CN102 informs the CRT unit whether to display under the RGB mode or the NTSC mode. When the pin No. 11 is LOW, the CRT is to operate on the NTSC mode, and when it is HIGH, the RGB mode.

◆ Sound Signal

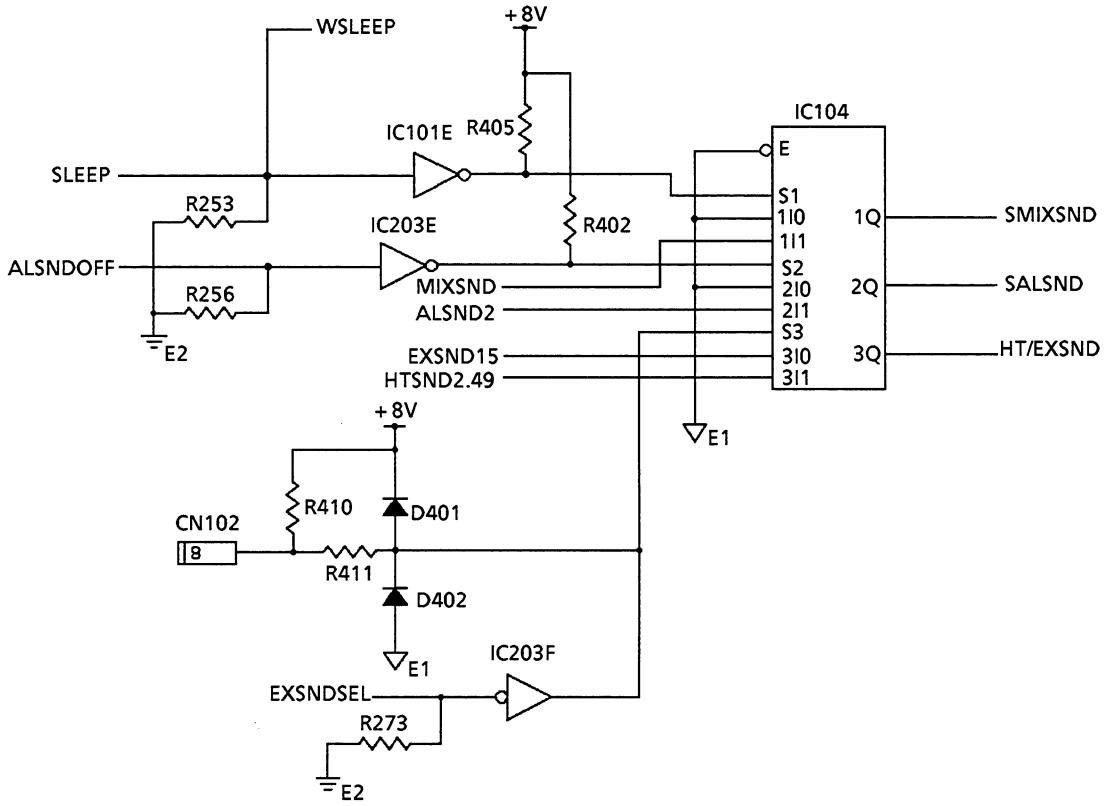
• Sound Signal Flow



There are three kinds of sounds, alarm sound, QRS sound, and external sound. The alarm sound and the QRS sound originate from the bedside monitor main unit. The external sound originates from the external unit. These sound signals undergo amplification, selection, volume adjustment, key sound addition, noise filtering, final selection, power amplification before outputted to the speaker.

• Sound Signal Control

Sound Signal Control Circuit



– Software Control

The IC201 outputs the sound control signals (SLEEP, ALSNDOFF, EXSNDSEL). The IC104 reads the statuses of these signals and determines the selection. The status of EXSNDSEL signal determines the selection between the QRS sound mode or external sound mode. The status of ALSNDOFF signal determines the ON/OFF mode of the alarm. The status of SLEEP signal determines the ON/OFF of the whole sound unit.

The tables below show the statuses of the signal outputs and their selections.

Selection	EXSNDSEL
QRS sound output mode	0
External sound mode	1

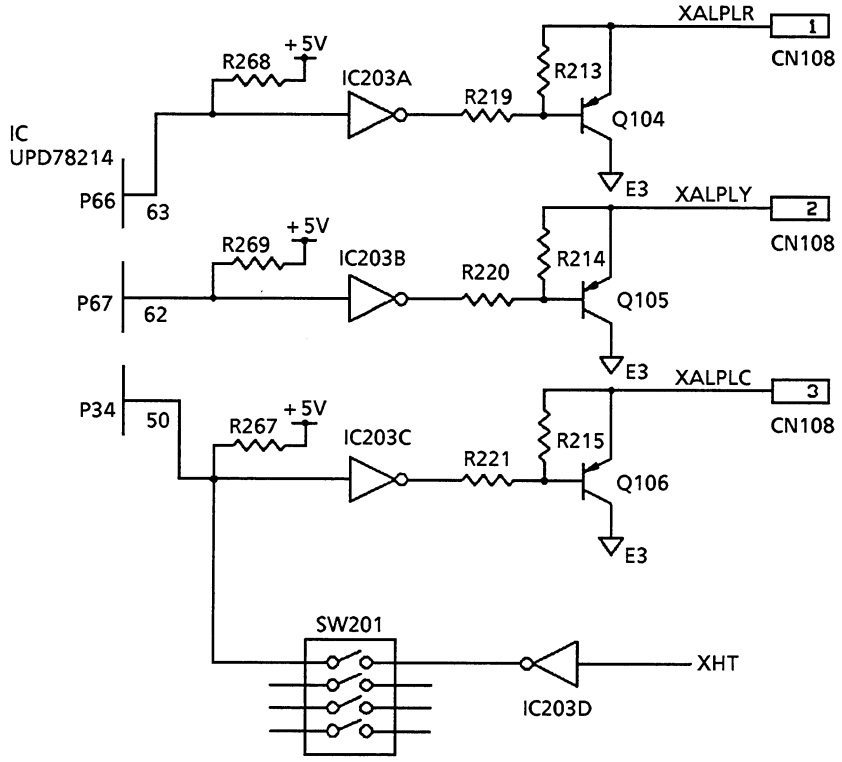
Selection	ALSNDOFF
Alarm ON	0
Alarm OFF	1

Selection	SLEEP
Whole sound unit ON	0
Whole sound unit OFF	1

– Hardware Control

The external unit can only control the selection between the QRS sound output mode or external sound mode. When the pin No. 8 of the external unit connector CN102 is LOW, the sound unit outputs the external sound; when OPEN, the sound units outputs the QRS sound.

◆ **Alarm Pole Control**



- **Software Control**

The IC201's PIN63 switches the alarm pole's red light on/off. The IC201's PIN62 switches the alarm pole's yellow light on/off. The IC201's PIN50 switches the alarm pole's green light on/off.

- **XHT Signal**

The XHT signal only controls the alarm's pole green light. When the active-low XHT signal is asserted, the alarm pole's green continues to light up. When the active-low XHT signal is negated, it switches off the alarm pole's green light.

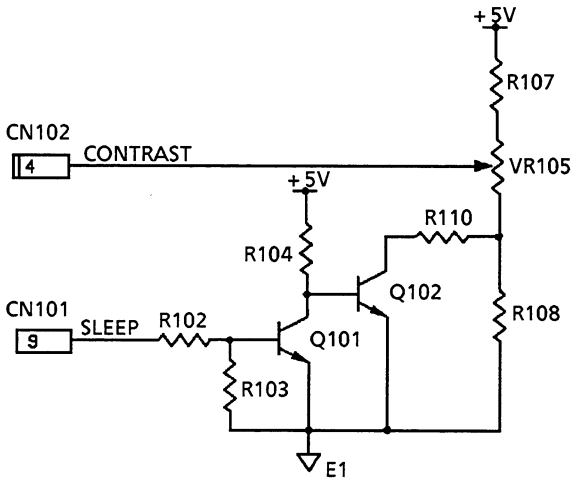
3-5-4 OPERATION (VR) Board, UP-0802

◆ Brightness and Contrast Adjustment

For brightness adjustment, adjust the variable resistor VR103 until the voltage on pin No. 1 of the OPERATION (VR) board's connector CN102 reach a certain value. For contrast adjustment, adjust the variable resistor VR105 until the voltage on pin No. 4 of the OPERATION (VD) board's connector CN102 reach a certain value.

◆ Sleep Control

Sleep Control Circuit



The active ("0") SLEEP signal on pin No. 9 of the OPERATION (VR) board's bedside monitor main unit connector CN101 causes the impedance between the variable resistor VR103 and pin E1 to drop. This in turn causes the voltage of the CONTRAST signal output of pin No. 4 of the OPERATION (VR) board's CRT unit connector CN102 to drop.

◆ Sound Adjustment

Adjustment on the variable resistors VR101 and VR102 attenuate the sound signal on pin Nos. 1 and 3 respectively of the OPERATION (VR) board's OPERATION CONTROL board connector CN101.

3-5-5 LED Board, UP-0806

The LED board has one LED that goes off during the standby mode, one LED that lights up when power is switched on, and an infra-red sensor for the remote control. The infra-red sensor circuit has a noise filter. This circuit outputs the TTL level signal.

Section 4 SELFCHECK

4-1 General

The following SELF CHECK programs are provided.

1. POWER-ON INITIAL SELF CHECK
2. MANUAL SELF CHECK

Each SELF CHECK PROGRAM consists of the following check items.

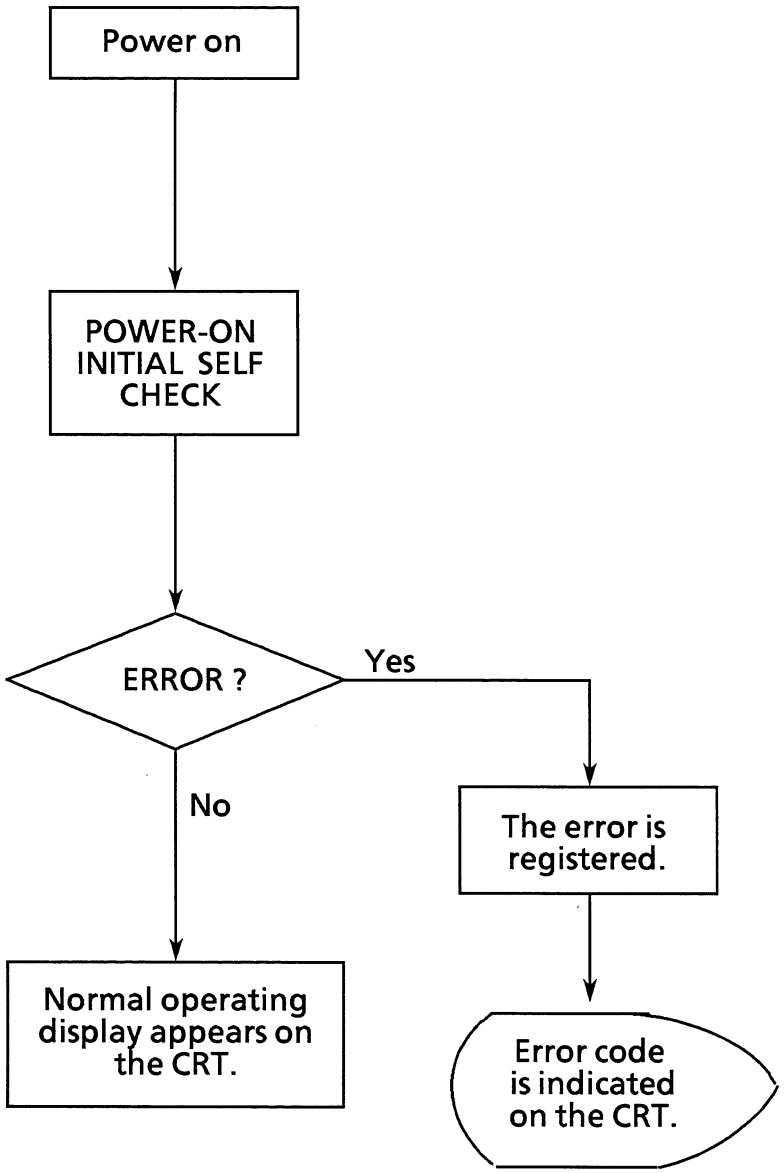
	POWER-ON INITIAL SELF CHECK	MANUAL (SELF) CHECK
CPU	ROM RAM 8279 (I/O) 71051 (I/O) 72001 (I/O) E^2PROM Global Memory (GLB.RAM) DPU Communication COM Communication [on DPU & COM board]	ROM RAM Global Memory (DPU) KEY (8279) SOUND (8279) RS232C (71051) RY/VD COM MEMORY CARD ALARM POLE DIP SW/LED/STATUS OTHER
CRTC		WAVE RAM CHARACTER RAM GRAPH RAM PALLET RAM Wave Display Character Display Graph Display
DPU	ROM RAM Global Memory (GLB.RAM) A/D-D/A Loop (A/D) Timing Port (RTC)	ROM RAM Global Memory (DPU) A/D RAM D/A-A/D Loop JA NIBP AMP (AP-851P) NIBP AMP (AP-860P) $tcPO_2$/$tcPCO_2$ AMP (AG-810P) CO_2 AMP (AG-830P) D/A WAVE D/A-A/D HEAD AMP CONTROL DIP SW/LED OUTPUT OTHER FIELD STRENGTH
COM3	ROM (from 8085) RAM (from 8085) 8251 (I/O) RTC	ROM RAM Global Memory (from COM3) Global Memory (from CPU) Communication WS RECORD DIP SW/LED INTERBED SELECT D/A Wave

NOTE

Global Memory: **The memory that can be accessed not only by the specific device but also by the other device.**

4-2 Power-On Initial Self Check

This check program is automatically executed whenever the power switch is turned on. If there is a problem, the display changes to DIAGNOSTIC CHECK AND SYSTEM SETUP display with the error indication while the error code is registered on ERROR HISTORY.



4-2-1 CPU Board

(1) ROM check
The ROM check is executed by comparing the value of the acquired sum of data except the value at the last address with the prestored checksum at the last address. If the values do not coincide, the error code is indicated on the CRT. Refer to ERROR CODE explanation (Section 5-3-2 & 3 at the page 5-6).

(2) RAM check (including Global Memory check on DPU, COM board)
The RAM check is executed by comparing each word after being written into the memory area of the RAM with "5555"H to be written as a test pattern. If a word is not "5555"H, the error code is indicated on the CRT.

(3) 8279 (Programmable keyboard/display controller) check
The check is executed by comparing each byte after being written into the memory area of the internal RAM (LED DISPLAY RAM) with "FF"H or "55"H to be written as a test pattern.

(4) 71051 (Programmable communication controller interface) check
Two bits of the status register of 71051, "Tx" and "Rx", are checked.

(5) 72001 (Advanced multi protocol controller)
Read and write return loop check.

(6) EEPROM, 58C65 check
The check is executed by means of Cyclic Redundancy Check (C.R.C.).

(7) Communication check between CPU board and DPU board
The MPU on the DPU board inverts all the words after the MPU on the CPU board writes a test pattern "5555"H into the memory area of the Global Memory on the DPU board. The check is executed by comparing each word with "AAAA"H.

(8) Communication check between CPU board and COM board
The MPU on the COM board inverts all the words after the MPU on the CPU board writes a test pattern "5555"H into the memory area of the Global Memory on the COM board. The check is executed by comparing each word with "AAAA"H.

4-2-2 DPU (Data Processing Unit) Board

(1) ROM check
The check is the same as the ROM check on the CPU board.

(2) RAM check (including Global Memory check on DPU board)
The check is the same as the RAM on the CPU board.

(3) A/D - D/A Loop check
The check is the same as "A/D - D/A Loop check" in MANUAL (SELF) CHECK.

(4) Timing Port check
The check is executed by verifying that the data acquires a increment after reading a stored data of the TIMING PORT every 1 millisecond.

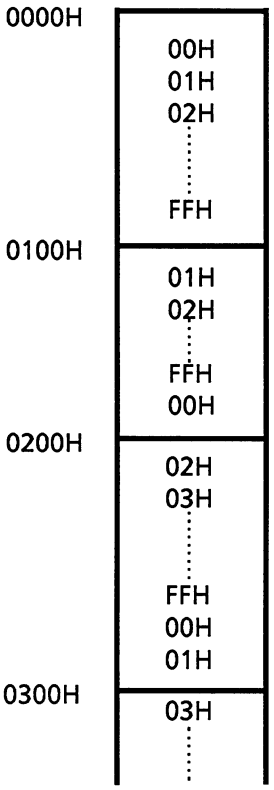
4-2-3 COM3 (Communication) Board

(1) RTC (Real Time Clock) check
The check is executed by comparing the interval time of the periodic interrupt with the value counted by the software counter.

(2) 8251 (for Central Monitor Interface) check
Two bits of the Input /Output (I/O) Port, "Tx" and "Rx", are checked.

(3) RAM check (from COM3)

The following test pattern is used to be written into the RAM. The check is executed every 256 byte by comparing the data after being written into the RAM with each data of the test pattern.



(4) Global Memory check (from CPU)

Same procedure as RAM Check.

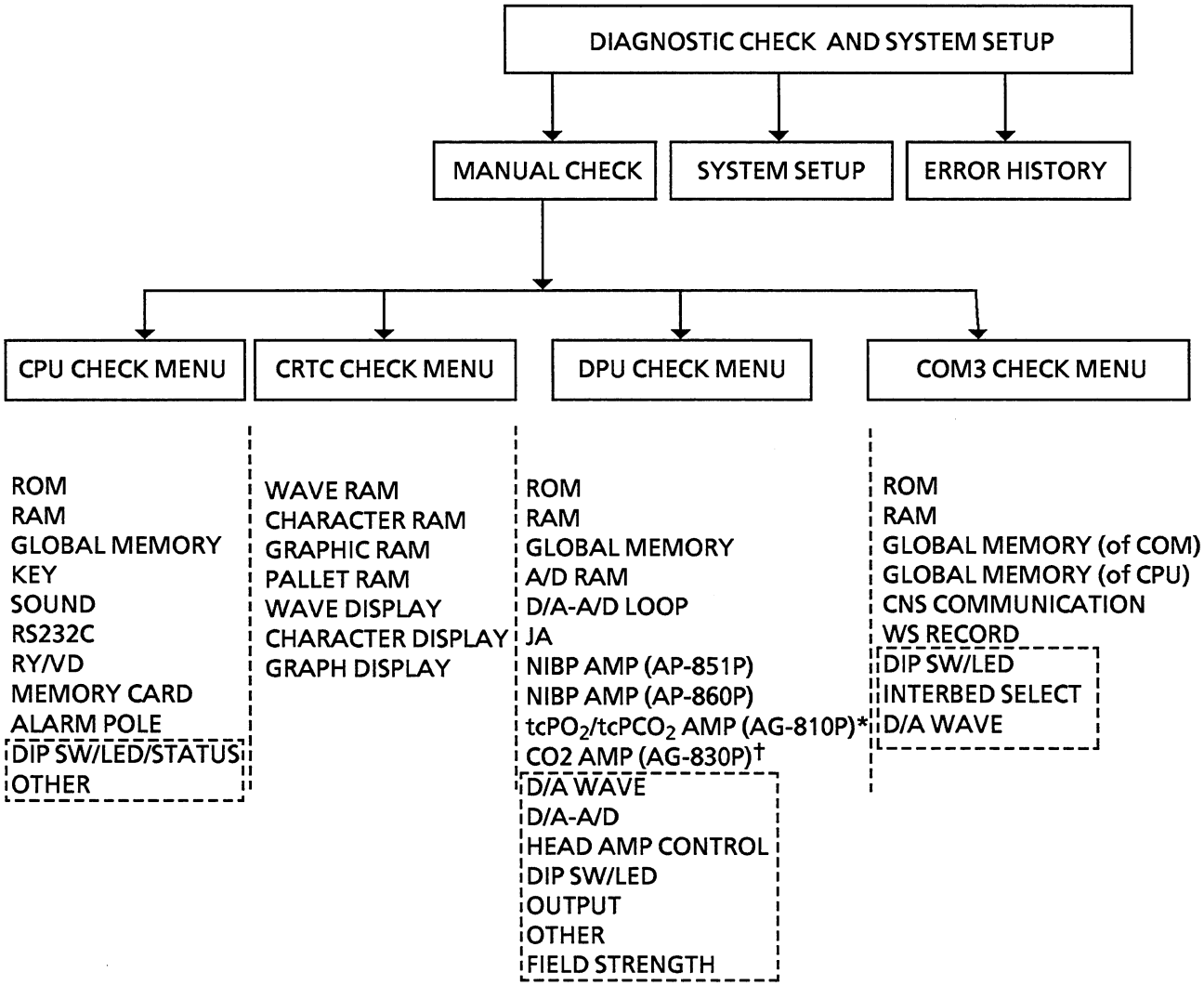
(5) ROM check (from CPU)

The check is the same as the ROM on the CPU board.

4-3 Manual (Self) Check

The Manual (Self) check program [CHECK MENU] is included in "Diagnostic Check and System Setup" display as follows:

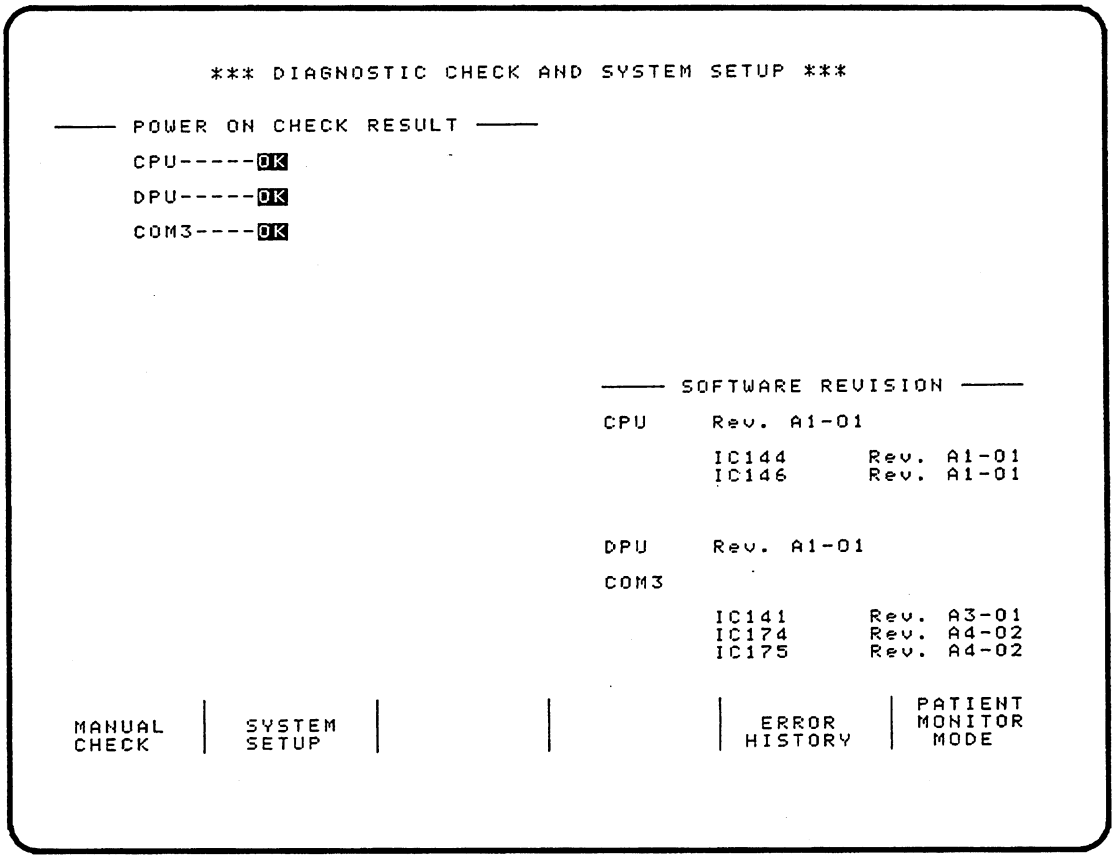
[PROGRAM HIERARCHY STRUCTURE]



: Press the REVIEW key first before pressing the "MANUAL CHECK" multifunction key to display the check items in the dotted rectangle.

*** Available in Japan only.**
† Not available in the U.S.

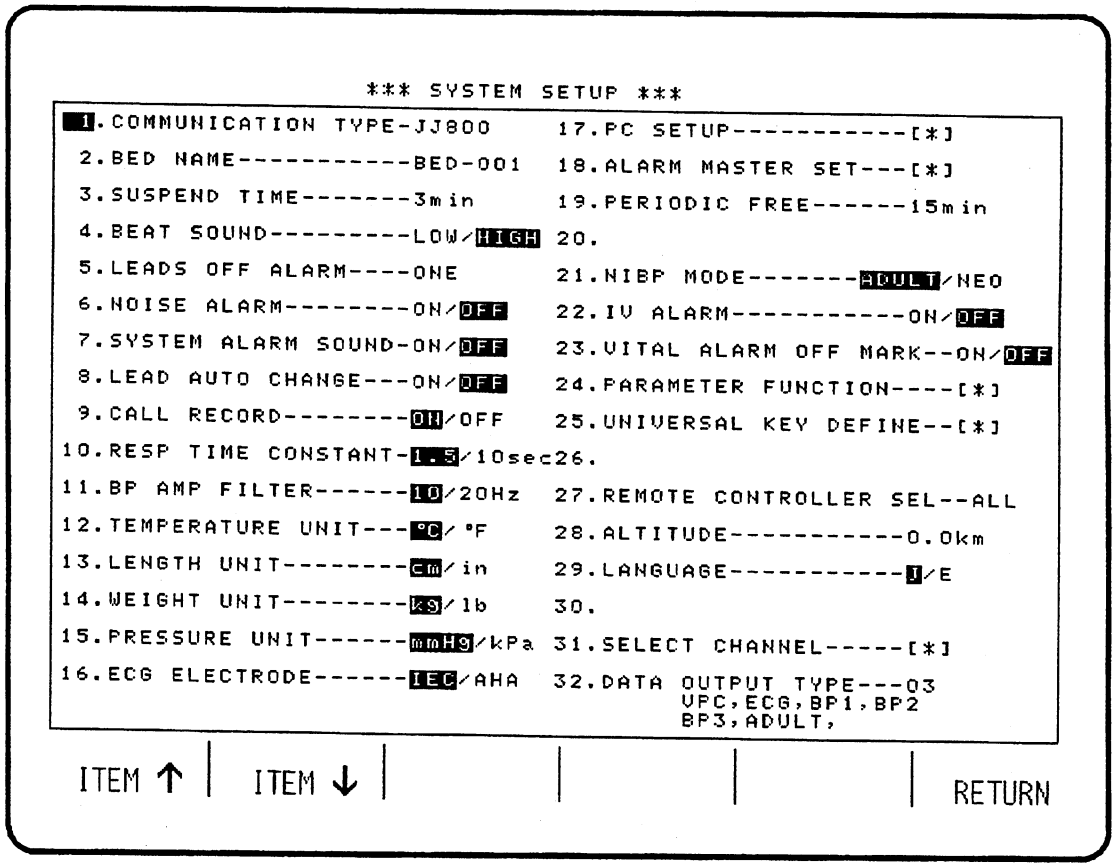
The following "Diagnostic Check and System Setup"display appears on the CRT by pressing the SELF CHECK key on the operation panel for three seconds, or switching on the main power switch while pressing the SUSPEND key.



On the above display, MANUAL CHECK, SYSTEM SETUP, ERROR HISTORY or PATIENT MONITOR MODE (Normal Operating mode) can be selected by pressing a multifunction key related to each mode.

4-3-1 System Setup

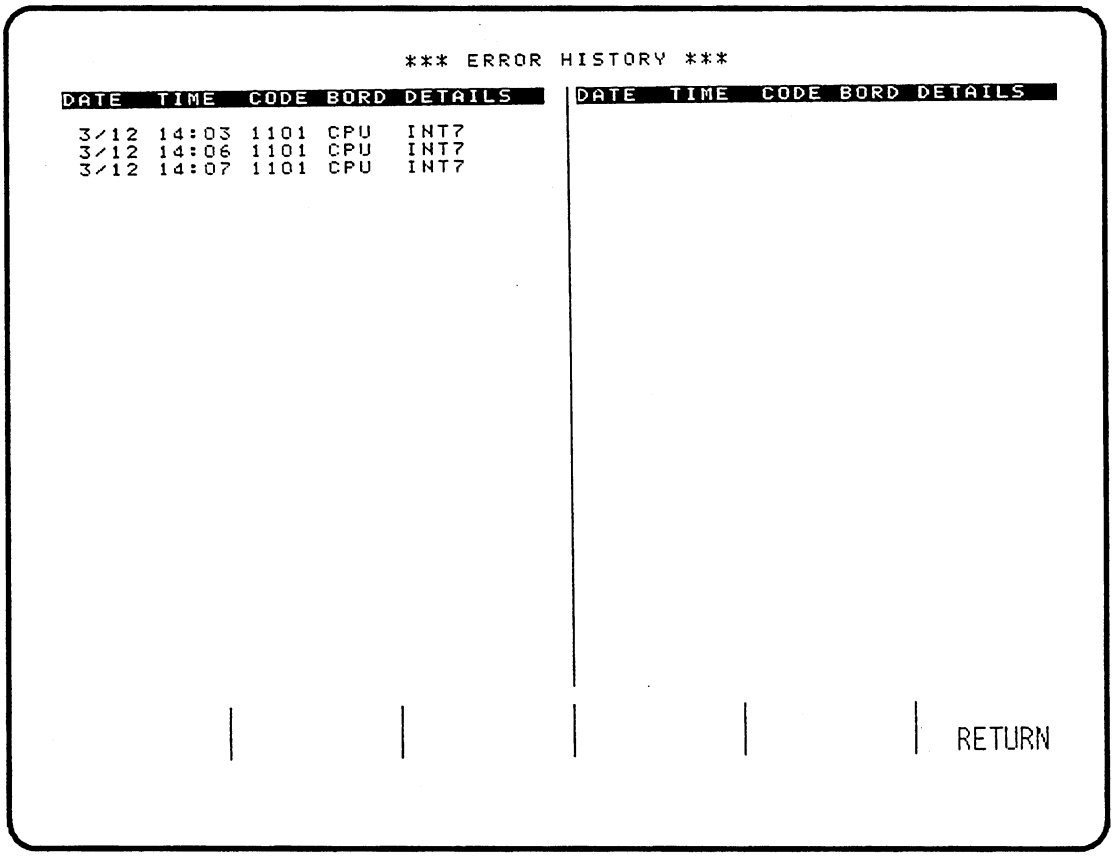
When SYSTEM SETUP is selected by pressing the SYSTEM SETUP key, the display changes to the following display.



All the above conditions can be modified by pressing multifunction keys related to the up/downward key or right/leftward key after selecting a item by pressing the "ITEM ↑" or "ITEM ↓" multifunction key.

4-3-2 Error History

When ERROR HISTORY is selected by pressing the ERROR HISTORY key, the display changes to the following display.



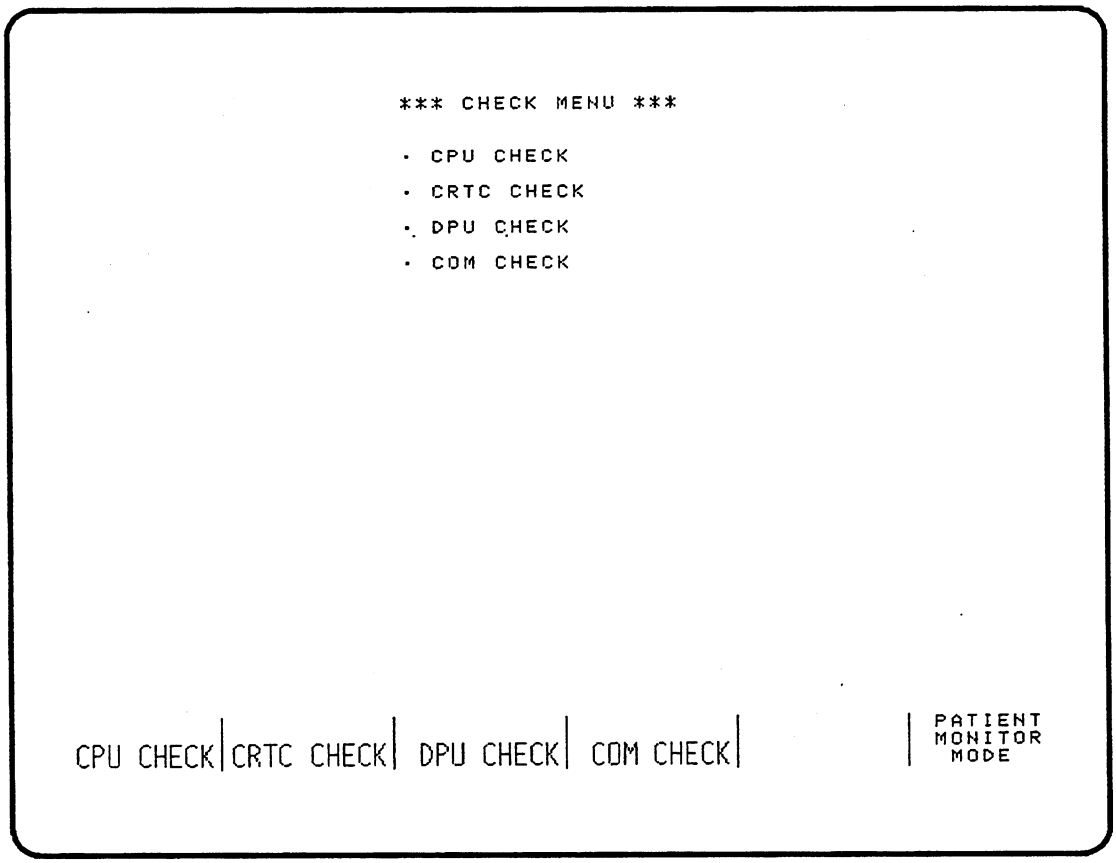
If an error is found, the date, time, code, board concerned and details are shown. Concerning the error code, refer to ERROR CODE (Section 5-3-2 & 3).

4-3-3 Patient Monitor Mode

When PATIENT MONITOR MODE is selected by pressing the "PATIENT MONITOR MODE" multifunction key, a normal operating display appears on the CRT.

4-3-4 Check Menu

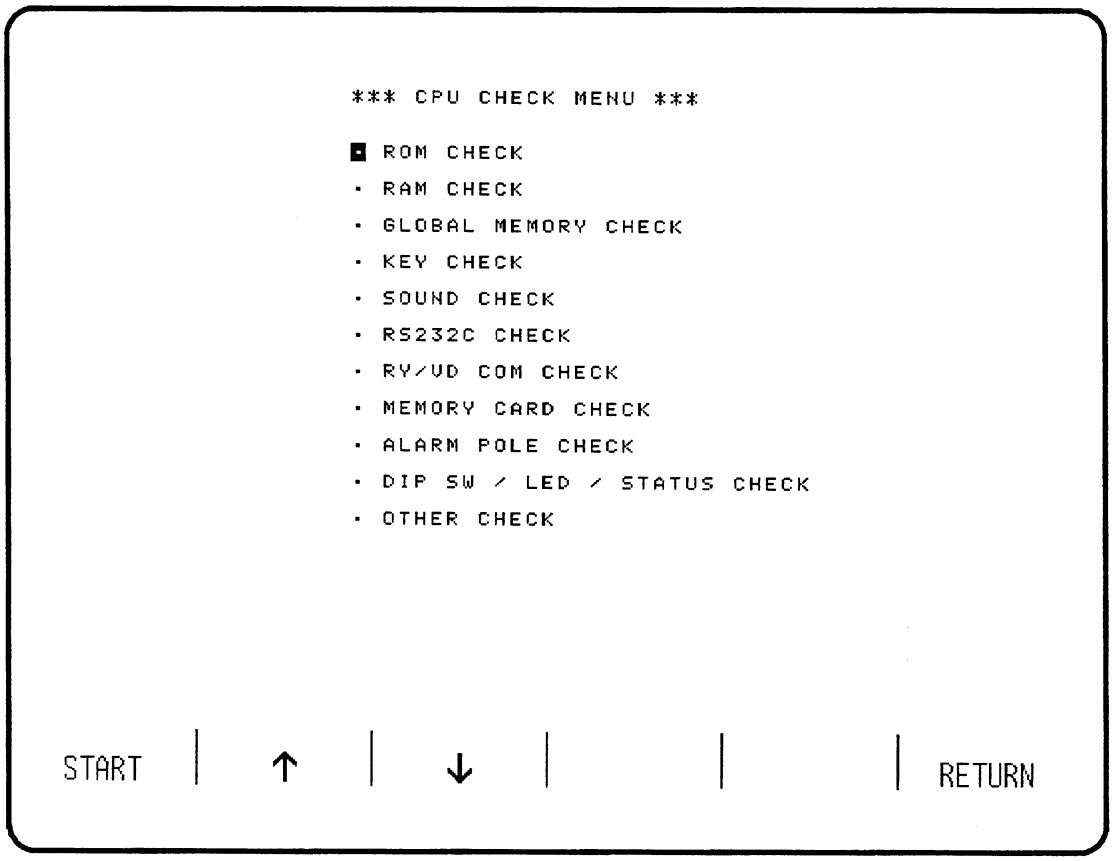
When MANUAL CHECK is selected by pressing the MANUAL CHECK key on the DIAGNOSTIC CHECK AND SYSTEM SETUP display, the display changes to the following display.



On the above display, the CPU, CRTC, DPU or COM board check can be selected by pressing the "CPU CHECK", "CRTC CHECK", "DPU CHECK" or "COM CHECK" multifunction key respectively.

◆ CPU (Central Processing Unit board) check

The following display appears on the CRT by first pressing the REVIEW key and then pressing the "CPU CHECK" multifunction key in the CHECK MENU display.



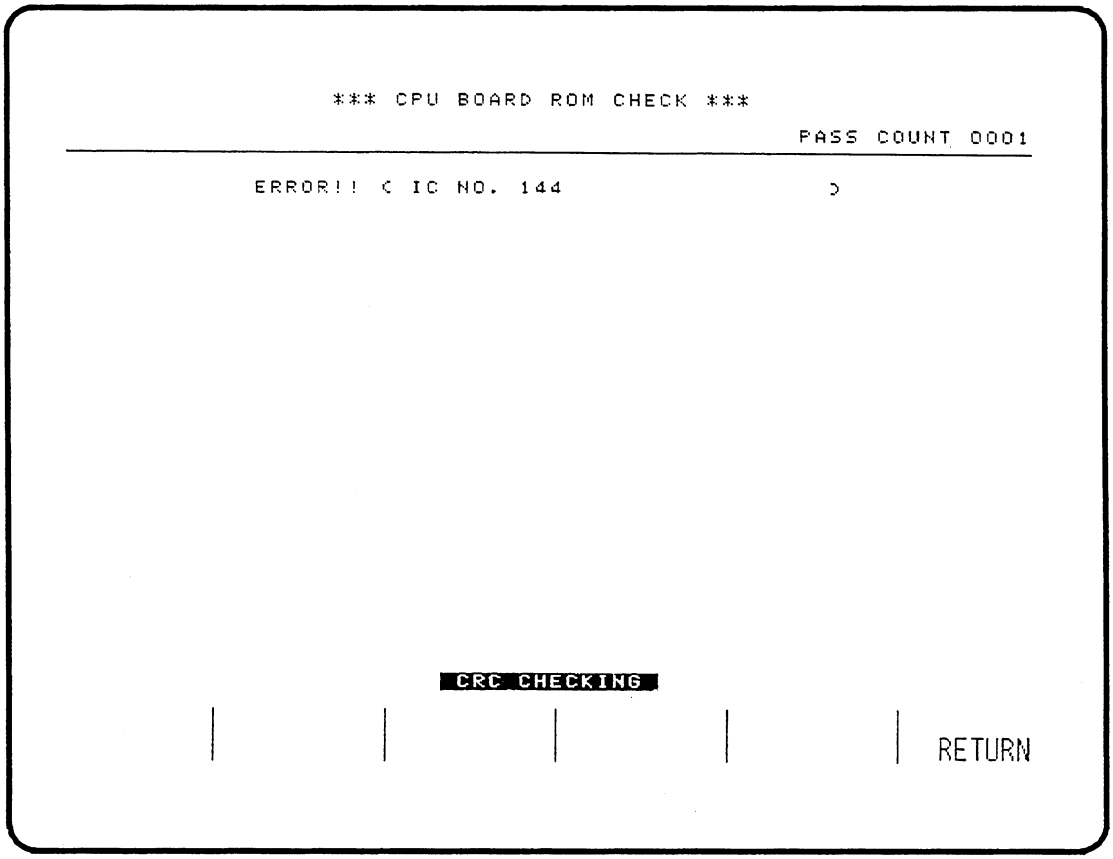
On the above display,

↑ ↓: to select a check item from the check items on the CRT

START: to execute the program for a selected check item while changing to the display for the check item

RETURN: to return to CHECK MENU display

- **ROM check**
  When ROM CHECK is selected, the display changes to the following display.



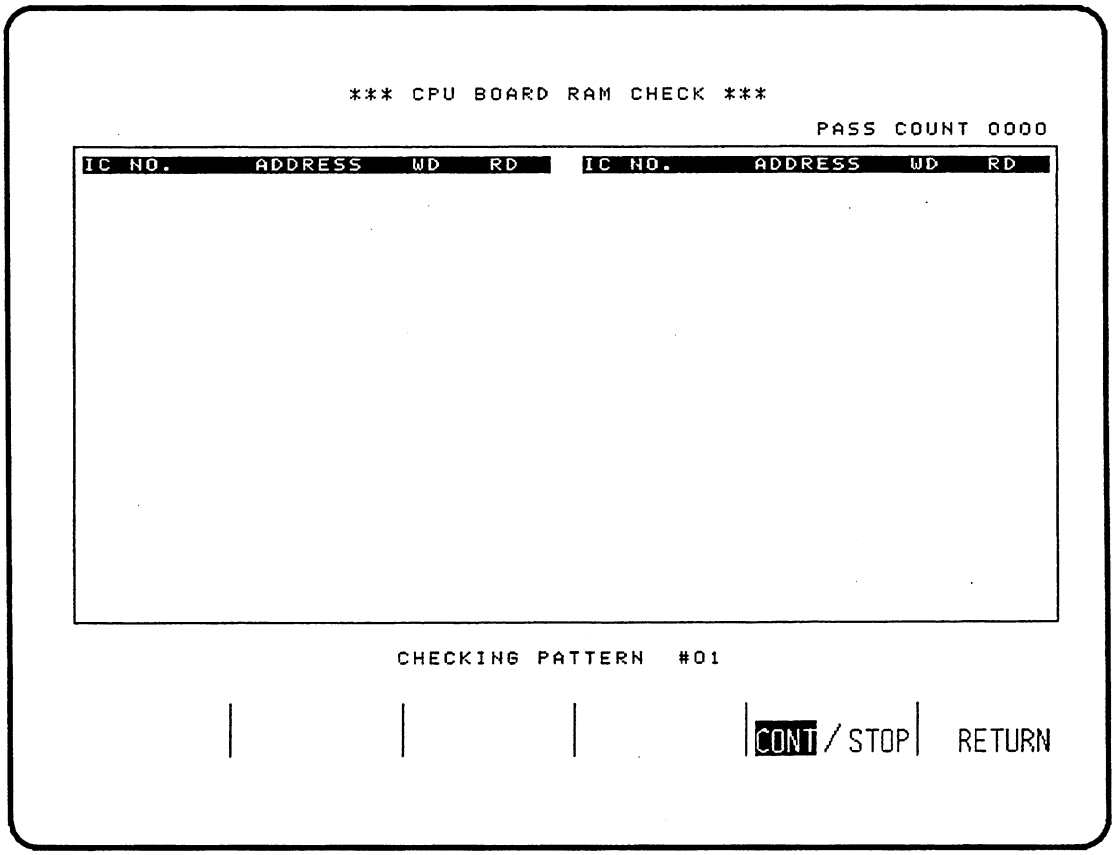
"CRC CHECKING" message is blinking while the check is executed with Cyclic Redundancy Check (C.R.C.). Whenever one cycle of the check is completed without an error, "PASS COUNT" increases by one. If there is an error, the error message appears on the display, as in the following example.

ERROR !! (IC No. 144, 146)

The check is stopped by pressing the "RETURN" multifunction key and the display returns to the CPU CHECK MENU.

- **RAM check**

  When RAM CHECK is selected, the display changes to the following display.



"CHECKING PATTERN #XX" message blinks during the checking.
The check is executed by comparing each data after writing one of the following check patterns (No.1 to 15) into the memory area with the check pattern.

[TABLE - 1]

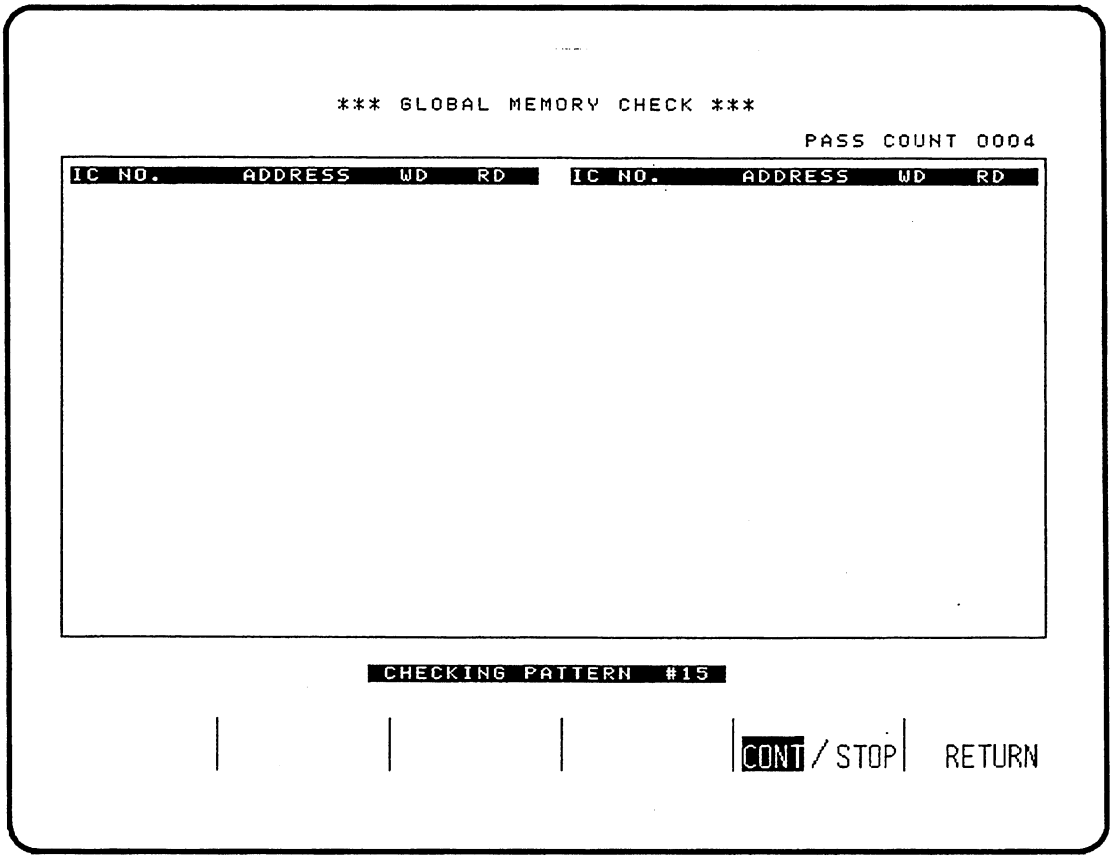
No.	PATTERN	No.	PATTERN
1	Decrement (BYTE)	9	Upper BYTE: FF, Lower BYTE: 00
2	55 (BYTE)	10	00 (BYTE)
3	0F (BYTE)	11	BIT SHIFT (WORD)
4	Alternating "00"H and "FF"	12	5555 (WORD)
5	Upper BYTE: 00, Lower BYTE: FF	13	AAAA (WORD)
6	AA (BYTE)	14	FFFF (WORD)
7	F0 (BYTE)	15	0000 (WORD)
8	Alternating "FF" and "00"		

Whenever one cycle of the check patterns (No.1 to 15) is completed without an error, "PASS COUNT" increases by one. If there is an error, the error message appears on the display as in the following example.

IC Number	Address	WD	RD	(WD: Data to be written)
IC 152, 153	08A000	5555	FFFF	(RD: Data to be read)

The check is continued until the CONT/STOP mode on the display is set to STOP by pressing the "CONT/STOP" multifunction key.
The display returns to the CPU CHECK MENU by pressing the "RETURN" multifunction key.

- **Global Memory check**

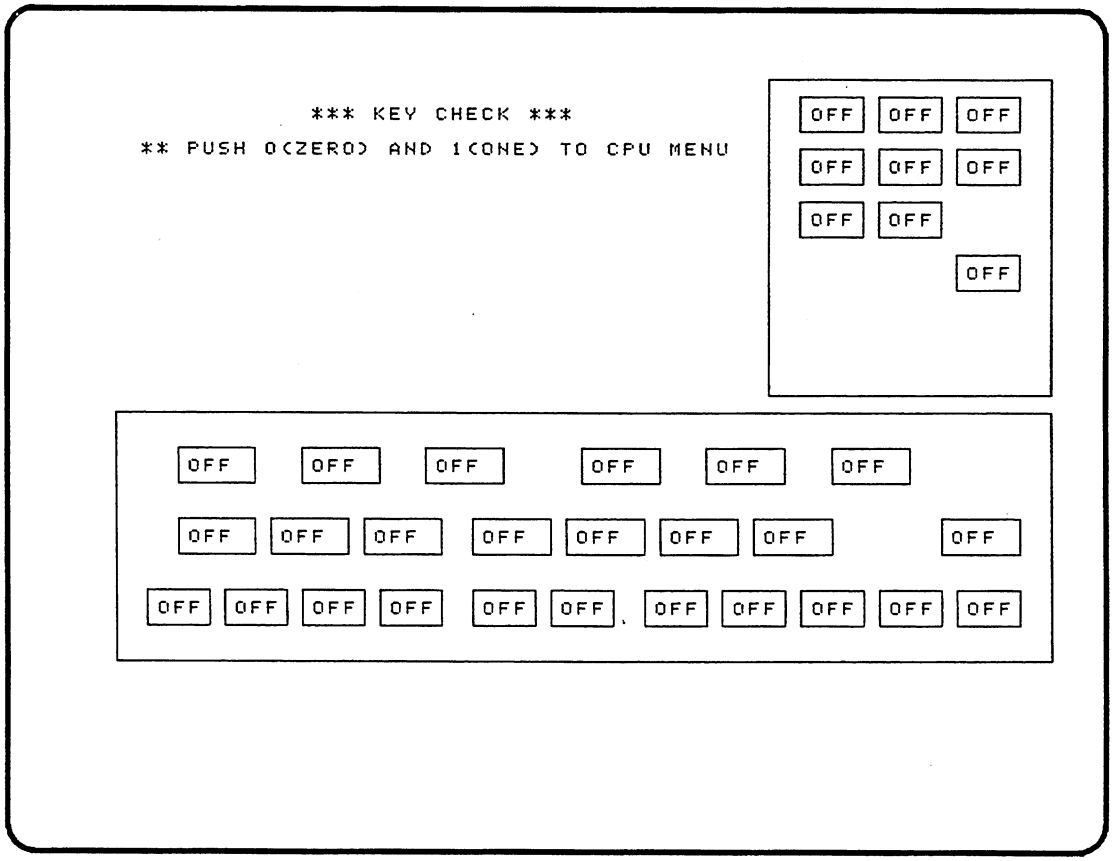


The check contents are the same as the TABLE-1 of the RAM CHECK. The checking area is the global memory on the DPU board. When the global memory can not be accessed, the following message appears on the CRT.

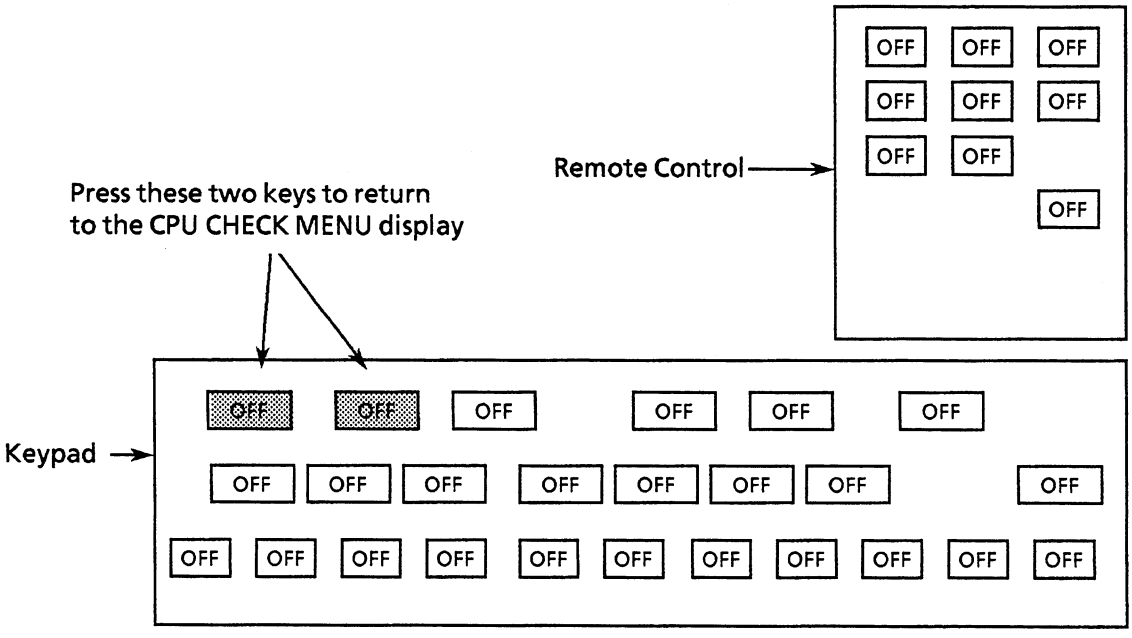
"DPU BOARD NOT INSTALLED"

The check is continued until the CONT/STOP mode on the display is set to STOP by pressing the "CONT/STOP" multifunction key.

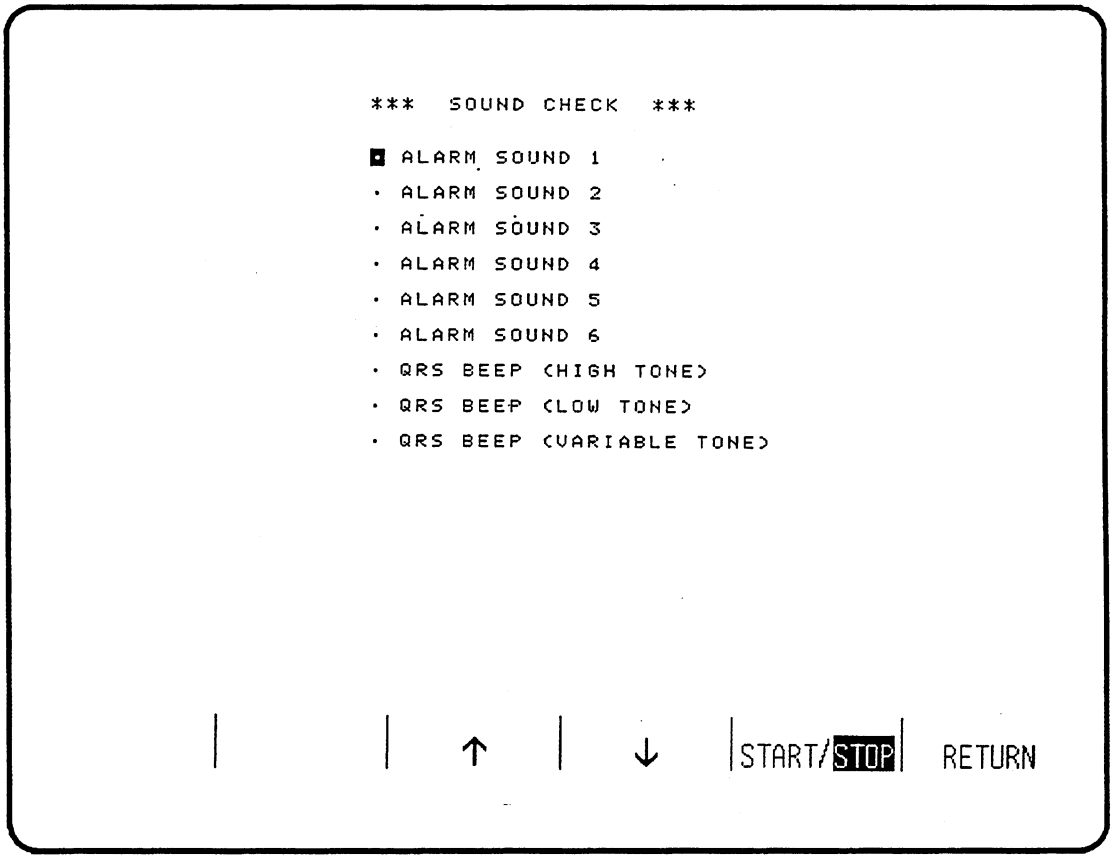
- **Key check**



"OFF" marks located according to keys on the keypad and the remote control appear on the screen. When a key switch is normal, the "OFF" mark concerned changes to a reverse lit "ON" while the key switch is pressed.
To return to the CPU CHECK MENU, press the shaded keys as shown below.



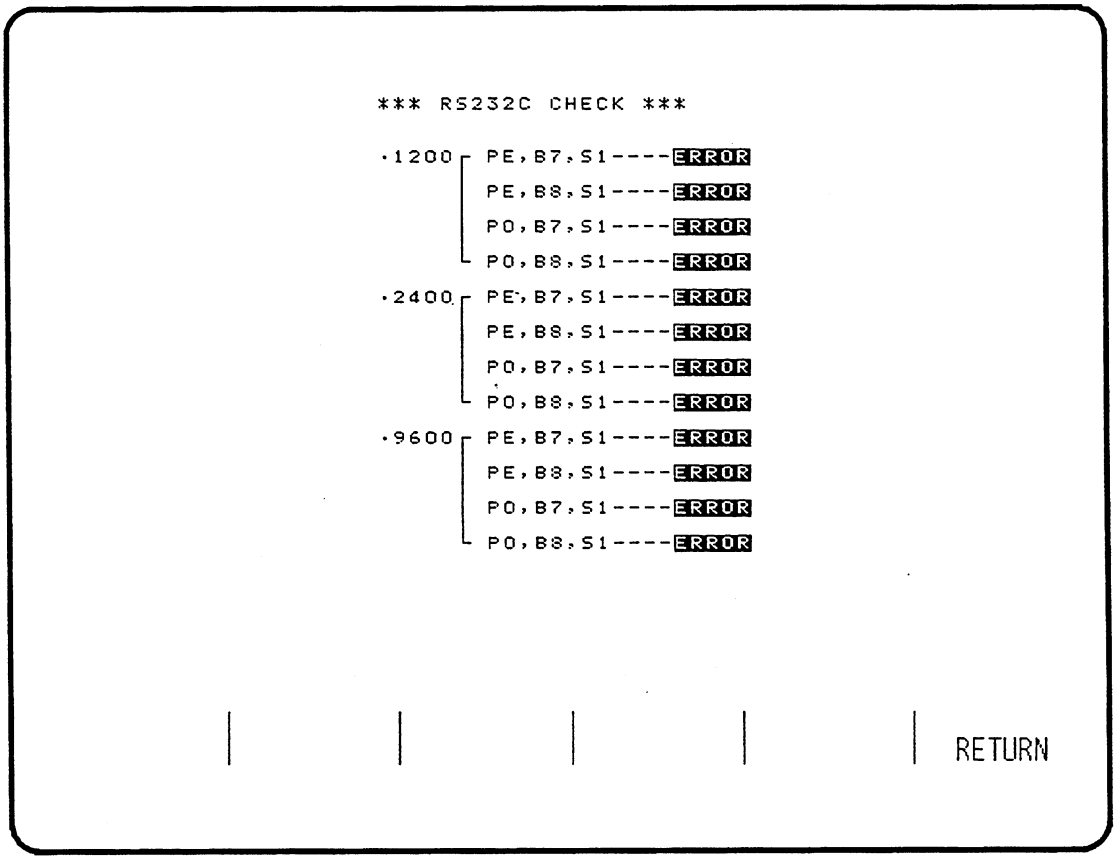
- **Sound check**



Each sound is generated by setting the START/STOP mode to START after selecting one of five check sounds on the display by pressing the " ↑ "or " ↓ " key.

SOUND MENU	TONE
ALARM SOUND 1	"Piro Piro"
ALARM SOUND 2	"Ping Pong"
ALARM SOUND 3	"Pon"
ALARM SOUND 4	"Pii Pii"
ALARM SOUND 5	"Pipi Pipi"
ALARM SOUND 6	"Pii"
QRS BEEP (High Tone)	"Pi" (High Beep)
QRS BEEP (Low Tone)	"Pock" (Low Beep), (Clack)
QRS BEEP (Variable Tone)	

- **RS232 check**

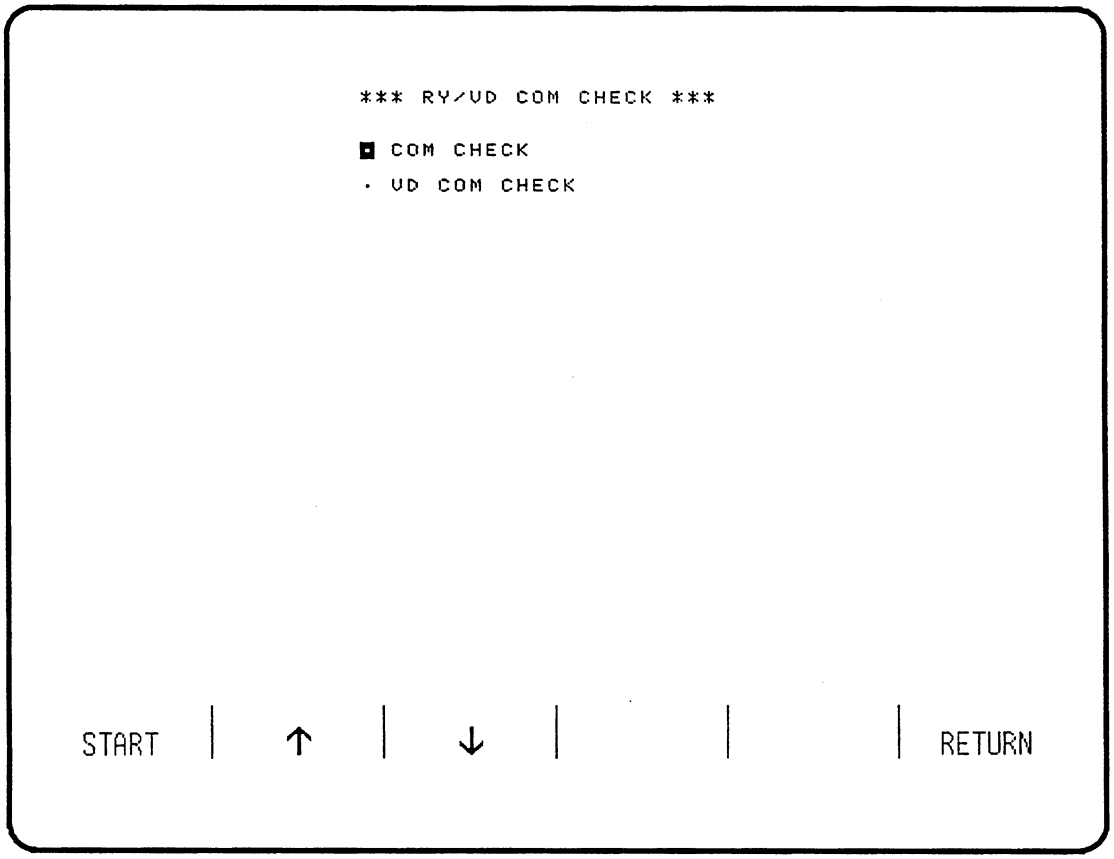


When the bedside monitor is not connected with external equipment which provides RS232C communication or when the following modification is not done to the receptacle for RS232C, the RS232C CHECK display appears with all the error indications on the CRT as in the above display.

[Modification]
pin 2 & 3: Short
Pin 4 & 5: Short
Pin 6 & 20: Short

1200, 2400, 9600: Baud rate (bits/sec.)
PE: Even Parity
PO: Odd Parity
B7: 7 Bits Data
B8: 8 Bits Data
S1: 1 Stop bit

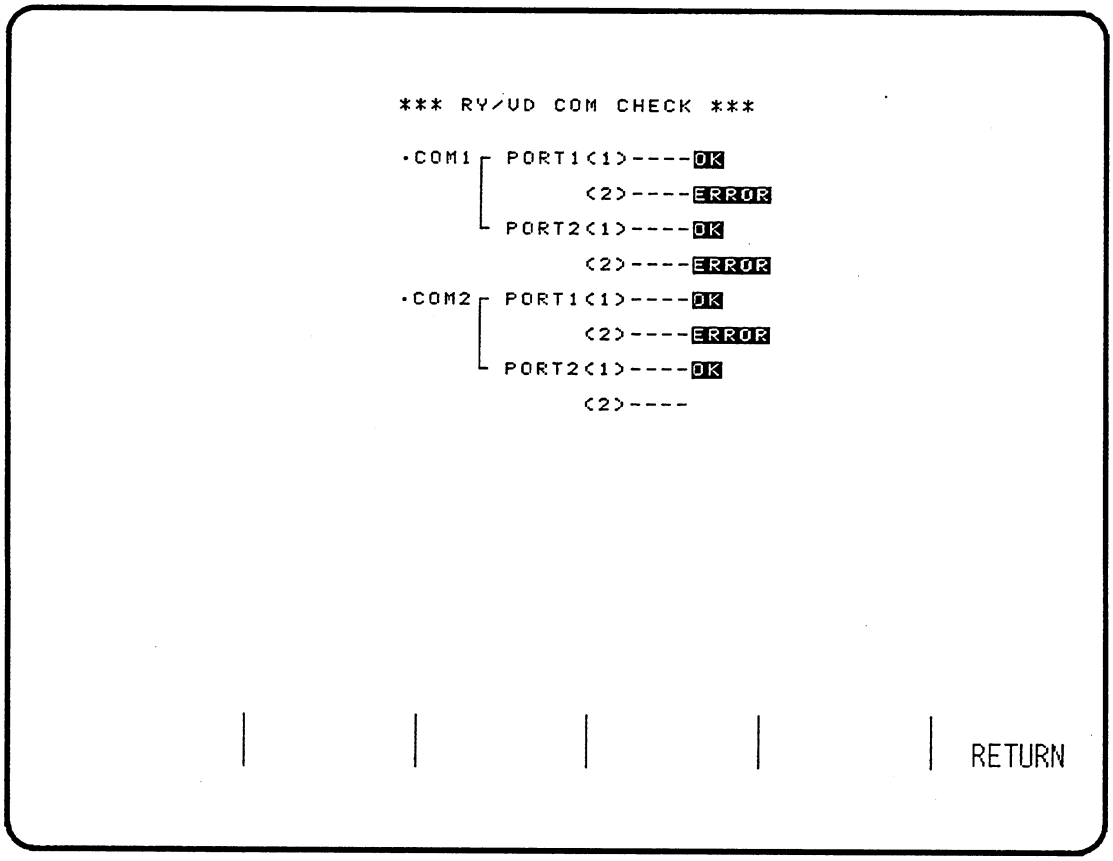
- **RY/VD COM check**



This checks the communication between the bedside monitor main unit and the keypad (COM CHECK) or the video display unit (VD COM CHECK).

↑/↓: To selects the check items.
START: To starts the check.
RETURN: To return to CHECK MENU display.

COM Check

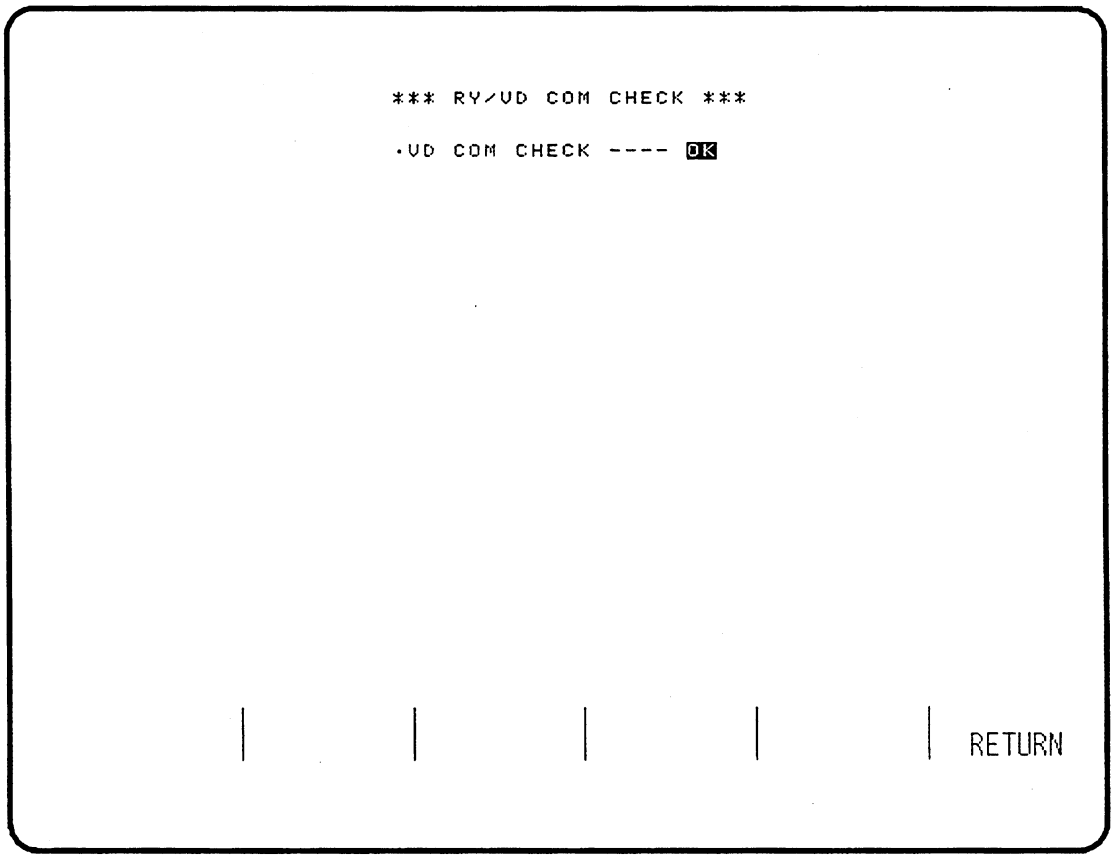


RETURN: To return to CHECK MENU display.

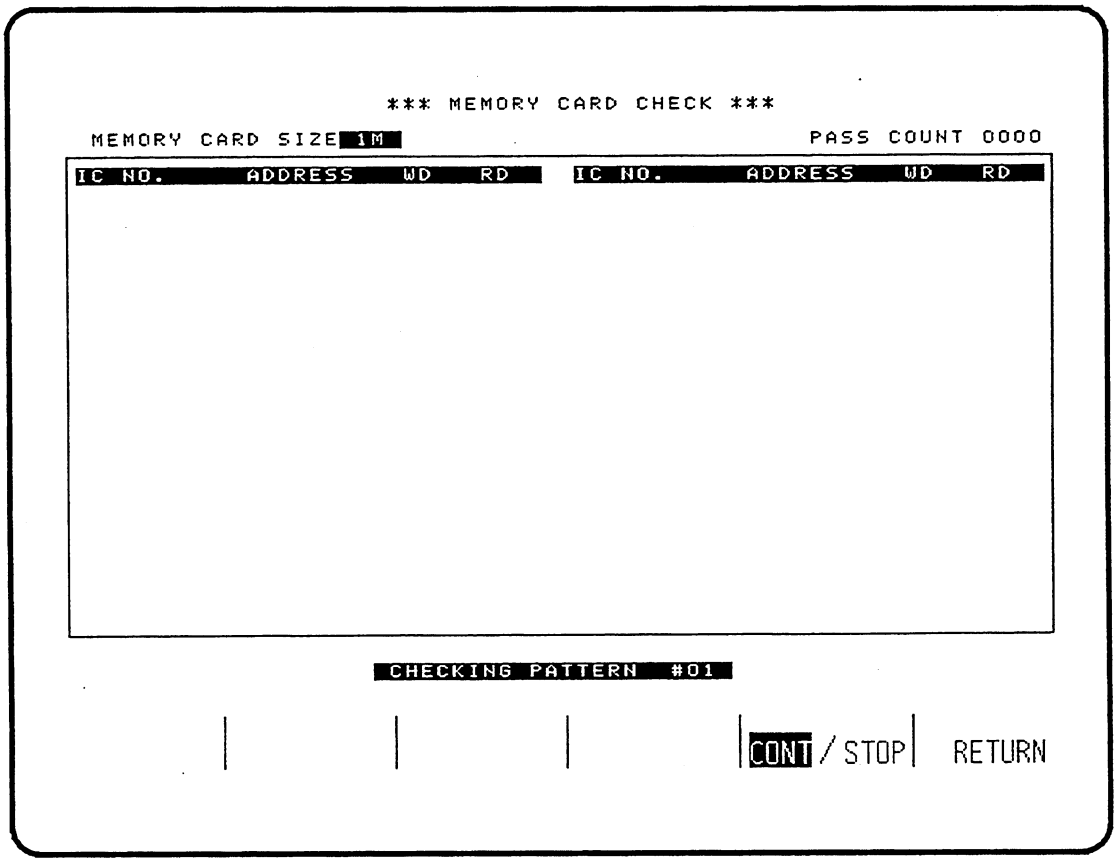
The table belowshows the communicating units and their pre–check run procedures (if, required)of the COM Check mode.

	PORT	COMMUNICATING UNIT	Pre–Check Run Procedures
COM1	PORT 1	Full-key board (Not used)	1) Not used 2) Not used
	PORT 2	Display unit	1) Not needed, IC's internal return loop check 2) Shot Pin No. 16 with Pin No. 17, and Pin No. 20 with Pin No21 of connector CN102 (UP-0795 Board)
COM2	PORT 1	Keypad (connected to display unit)	1) Not needed, IC's internal return loop check 2) Shot Pin No. 3 with Pin No. 4 of connector CN106 (UP-0801 Board)
	PORT 2	Keypad (connected to main unit)	1) Not needed, IC's internal return loop check 2) Shot Pin No. 3 with Pin No. 4 of connector CN104 (UP-0807 Board)

VD check



- **MEMORY CARD Check**



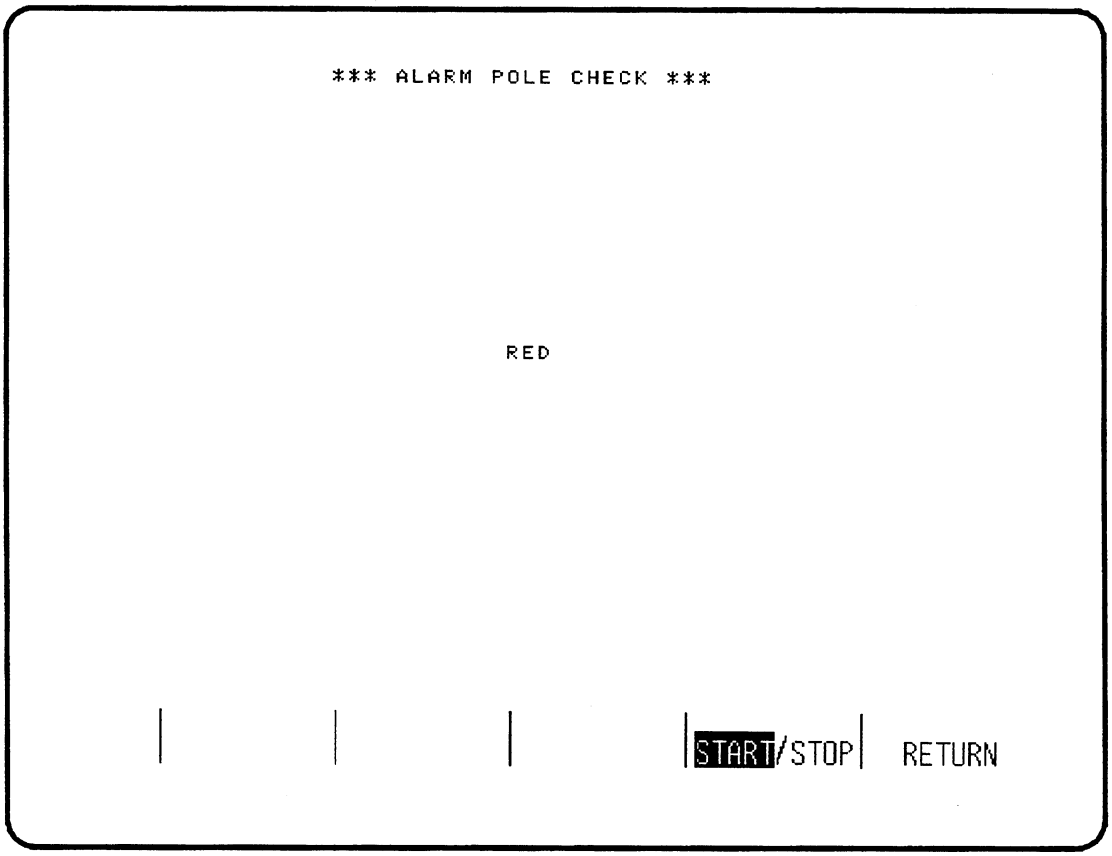
When the check mode is running "CHECKING PATTERN #01 " message blinks. If the MEMORY CARD is not inserted, the "MEMORY CARD NOT INSERTED" message is displayed. The "LOW BATTERY" message appears when the battery power of the memory card is low. The "WRITE PROTECT ERROR" message appears when data are written into a write protected memory card.

Checking pattern
The table below shows the 4 checking patterns.

No.	PATTERN	
1	Decrement	(BYTE)
2	5555	(WORD)
3	AAAA	(WORD)
4	FFFF	(WORD)

In the MEMORY CARD check, the checking pattern #1 to 4 are continuously written and read. To stop this, press the "STOP" multifunction key.

- **ALARM POLE Check**



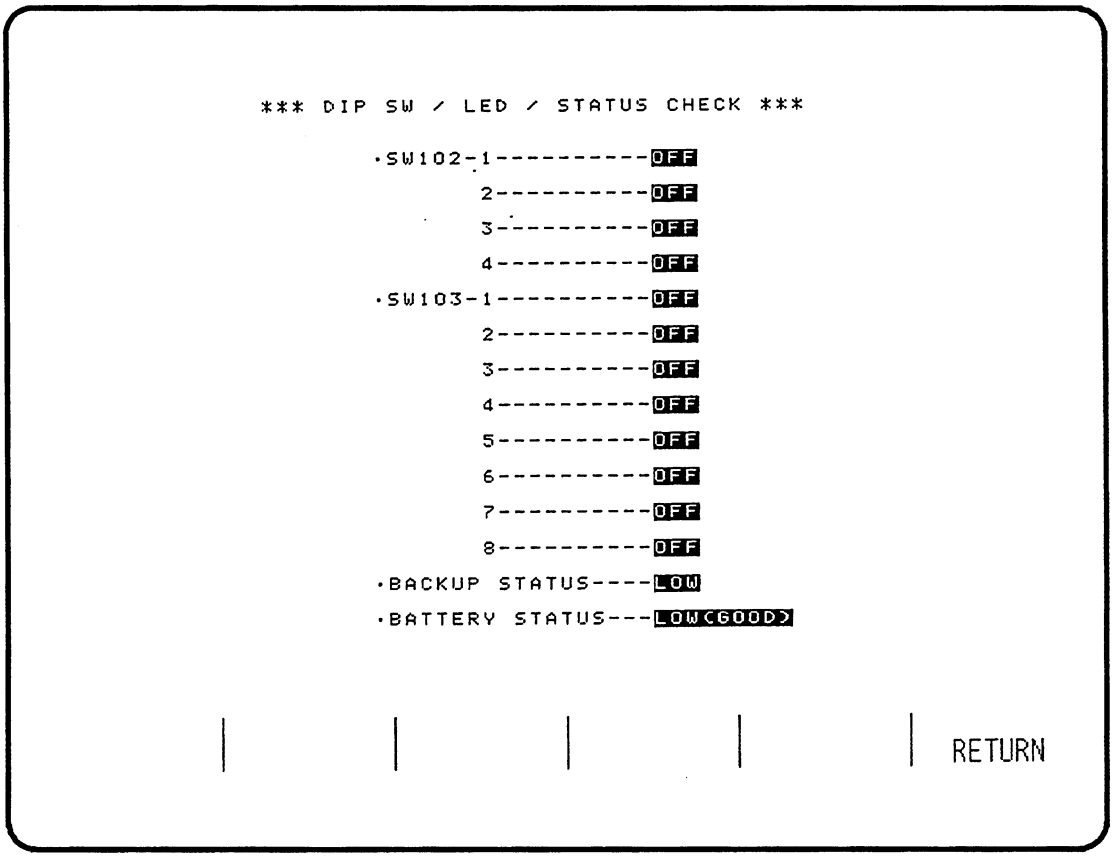
When the check mode is running the following messages appear repeatively.
RED → YELLOW → GREEN → RED → ...
At the same time the alarm pole flashes the above corresponding colors.

On the above display,
START/STOP: to start or stop this check program.

RETURN: to return to the CHECK MENU display.

The following sections are displayed by first pressing the REVIEW key and then "CPU CHECK" multifunction key on the DIAGNOSTIC CHECK AND SYSTEM SETUP display. These sections are for your reference since these check programs are for product inspection at the factory.

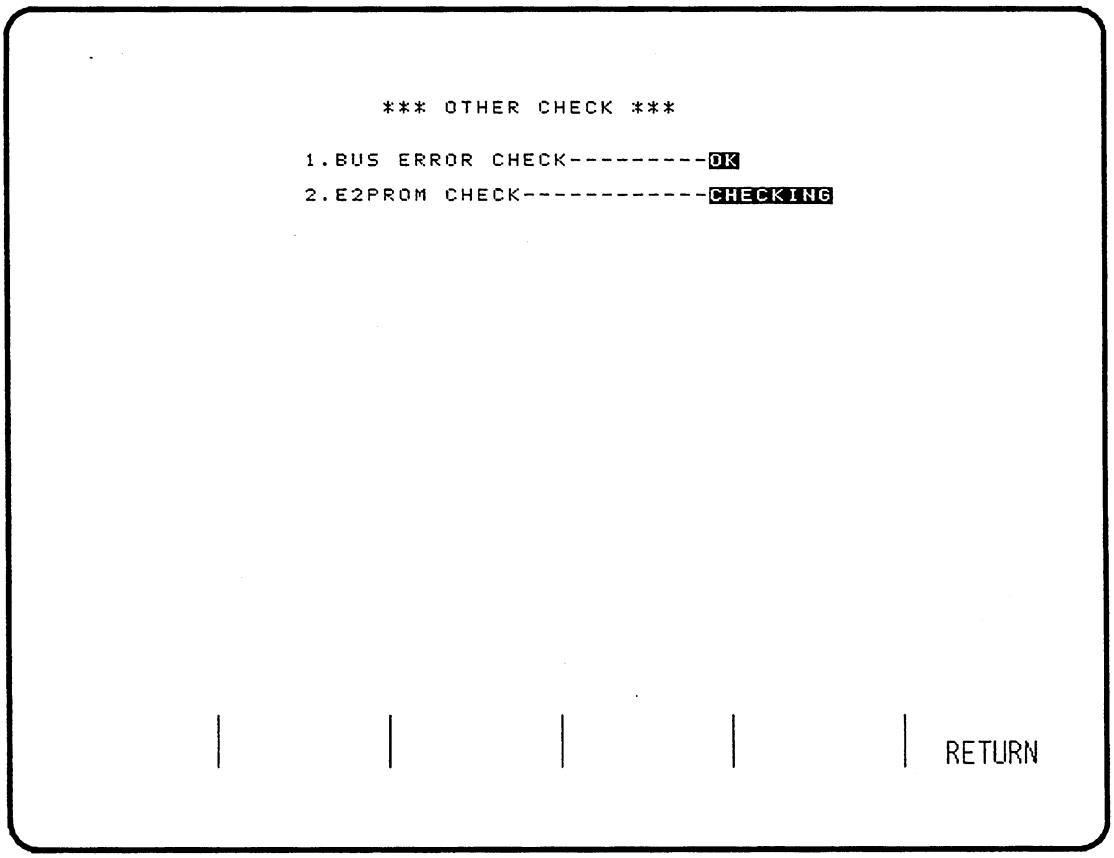
- **DIP SW / LED / STATUS check**



1) DIP SWITCH check
   The set condition of the dip switch on the CPU board, SW102 and SW103, appears on the CRT.
2) LED check
   Each LED (8 bits) on the CPU board sequentially lights and goes out one after another.
3) STATUS check
   "Backup Status" and "Battery Status" appear on the CRT as follows:

[Backup Status]		[Battery Status]	
Low:	Normal condition	Low:	Normal condition
High:	Super-capacitor must be charged	High:	Lithium battery must be replaced

- **Other Check**



"CHECKING" message blinks during the checking.

1) BUS ERROR check

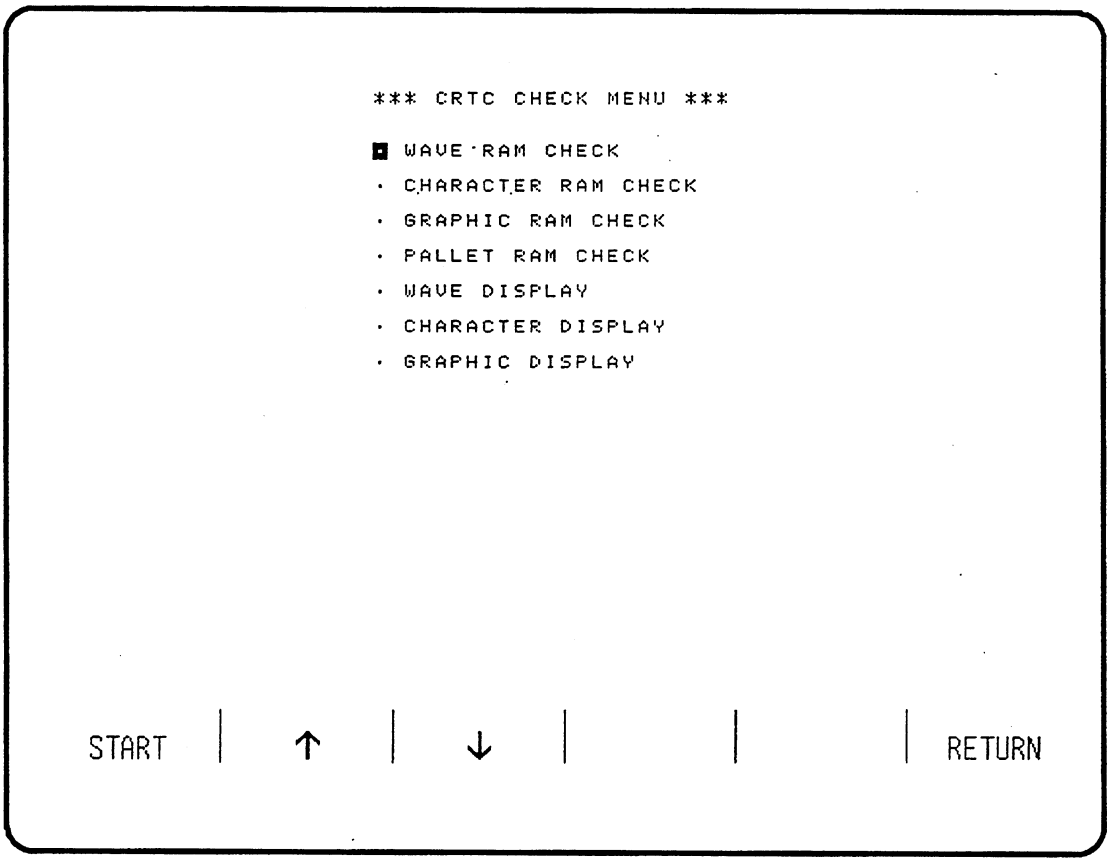
The check is executed by accessing an address at which memory area does not exist. A detection of a bus error signal is confirmed by indicating "OK."

2) EEPROM check

The check is executed by comparing each byte after being written into the EEPROM with check byte "55"H to be written. All data of EEPROM are stacked before "55" is written.

◆CRTC (CRT Control board) Check

When CRTC CHECK is selected by pressing the CRTC CHECK key on the CHECK MENU display, the following CRTC CHECK MENU appears on the display unit.



On the above display,

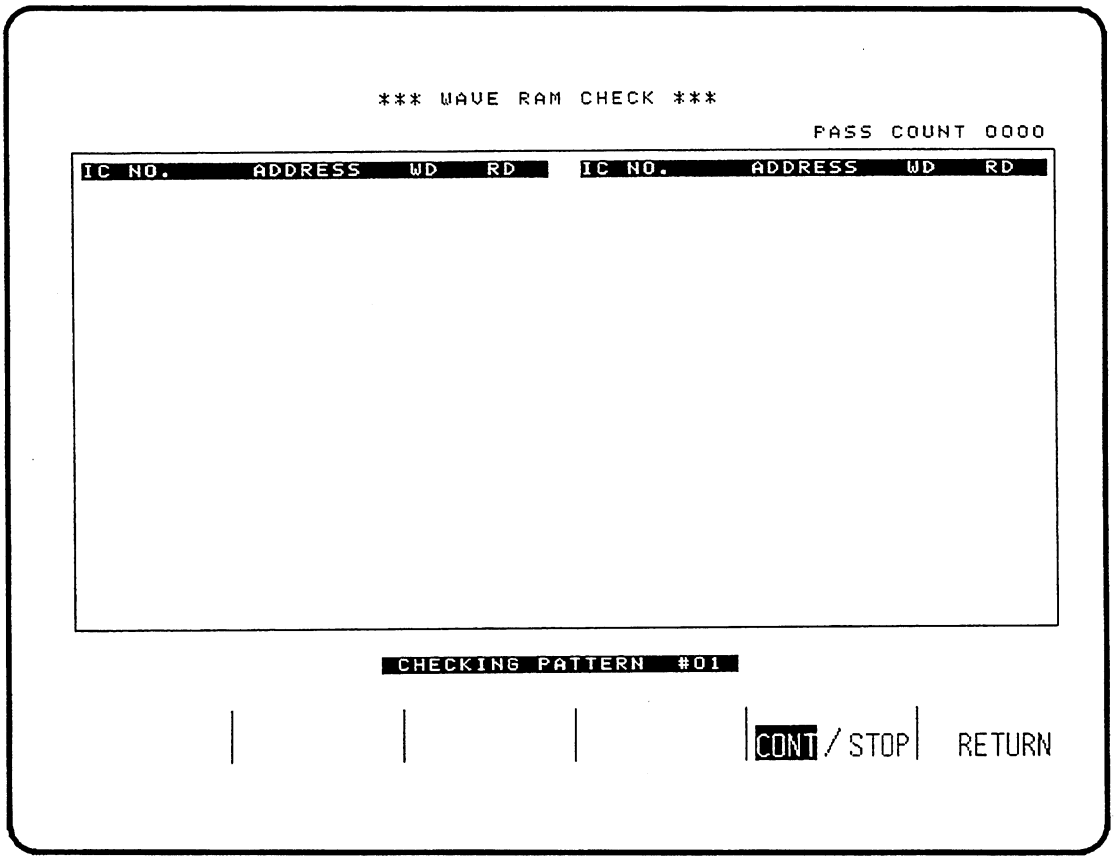
↑ ↓: to select a check item from the check items on the CRT

START: to execute the program for a selected check item while changing to the display for the check item

RETURN: to return to the CHECK MENU display

- **WAVE RAM check**

  When RAM CHECK is selected, the display changes to the following display.

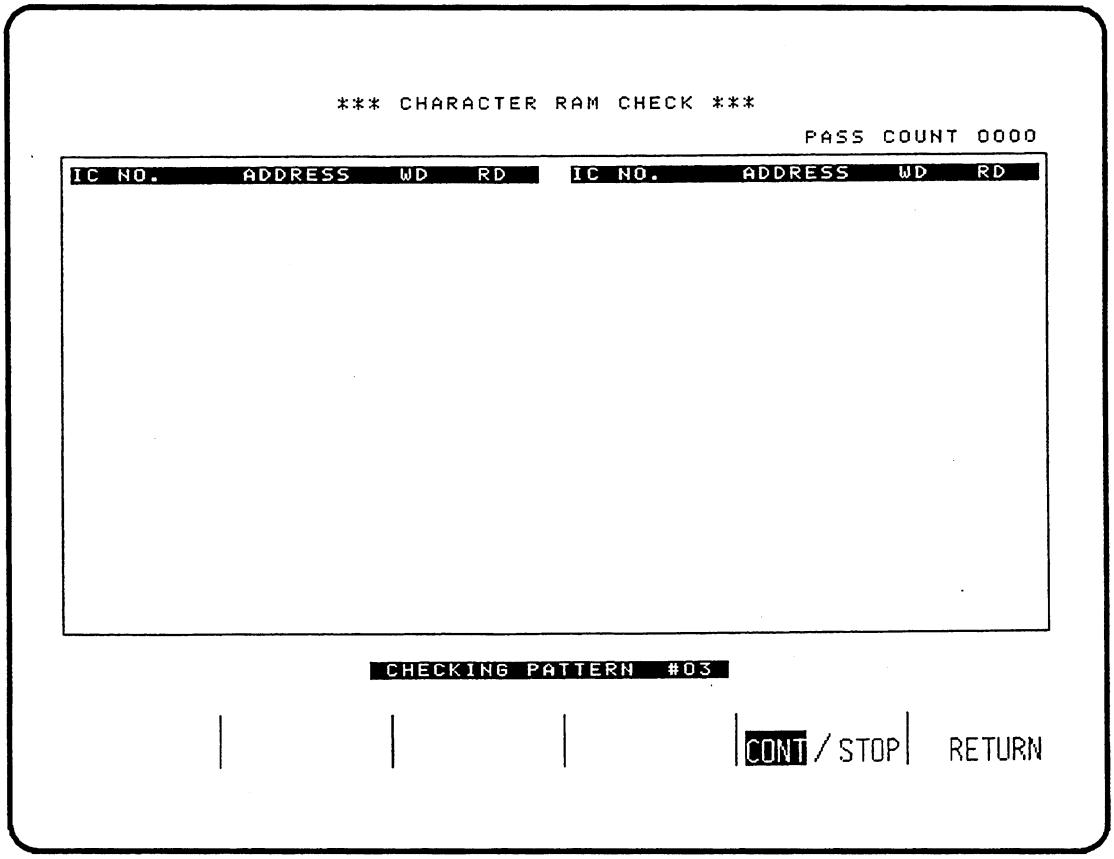


"CHECKING PATTERN #XX" message blinks during the checking.
The check is executed by comparing each data after writing one of the following check patterns (No.1 to 4) into the memory area with the check pattern.

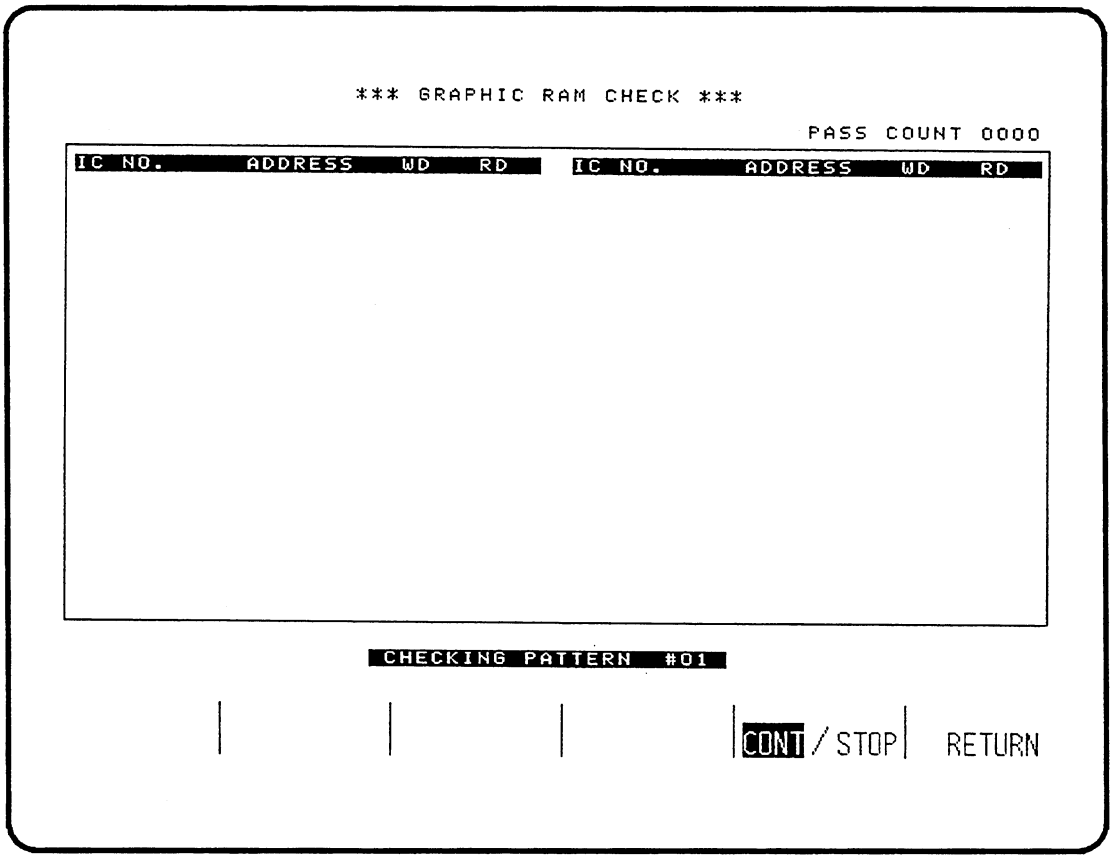
[TABLE - 2]

No.	PATTERN	
1	AAAA	(WORD)
2	5555	(WORD)
3	FFFF	(WORD)
4	0000	(WORD)

- **CHARACTER RAM check**
  Pattern No. 1 to 4 of Table-2 are used as the check pattern. The check is the same as the WAVE RAM CHECK on the CRTC board.

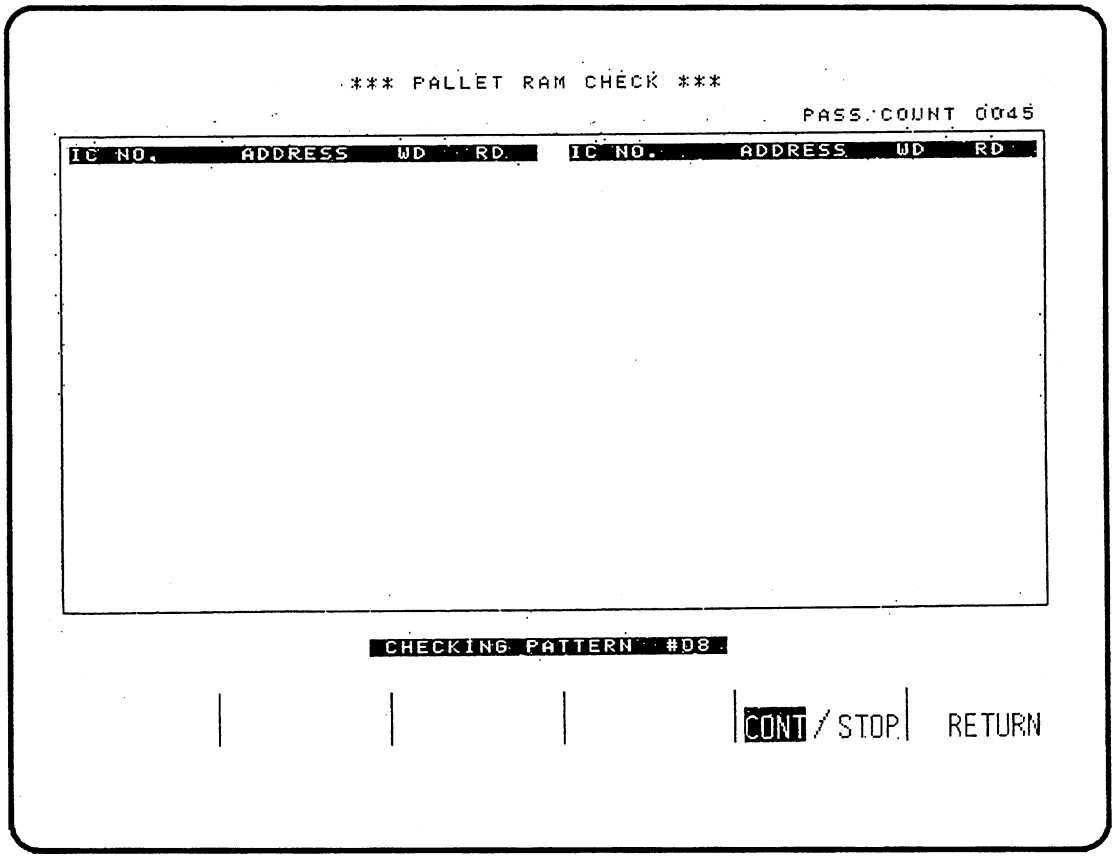


- **GRAPHIC RAM check**
  The check is the same as the CHARACTER RAM CHECK.



- **PALETTE RAM check**

  Pattern No.1 ~ 4 of Table -3 are used as the check pattern. The check is the same as the WAVE RAM CHECK on the CRTC board.

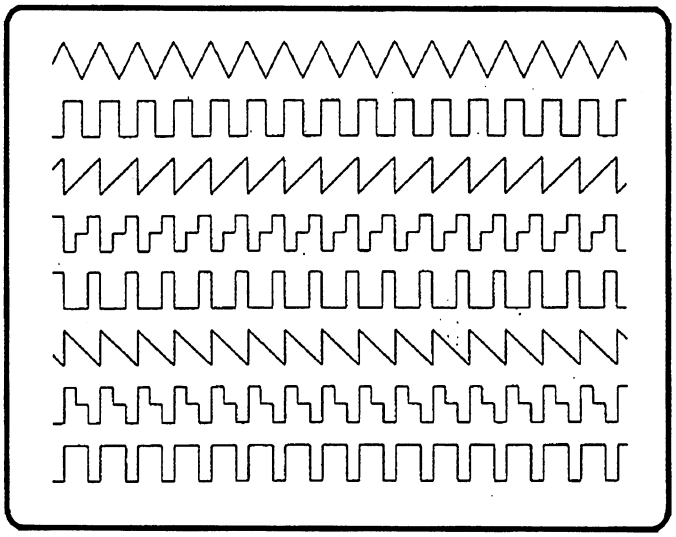


[TABLE - 3]

No.	PATTERN	
1	2A	(Byte)
2	15	(Byte)
3	3F	(Byte)
4	00	(Byte)

- **WAVE Display check**

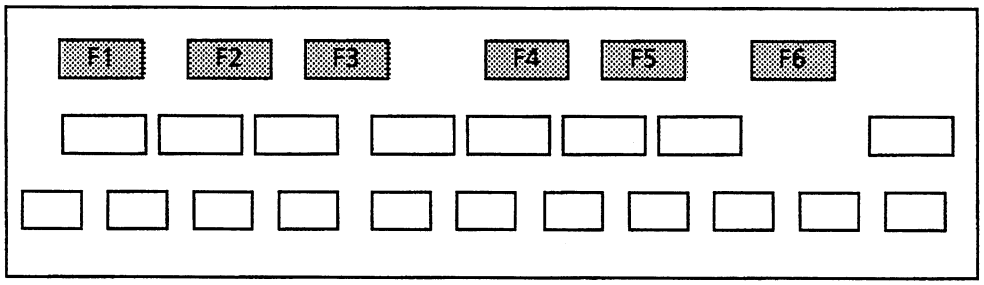
  8 traces of sweeping waveform appear on the display unit screen.



The following shaded keys on the keypad operate this check mode.

NOTE

To avoid confusion, the shaded keys are named from F1 ~ F6.

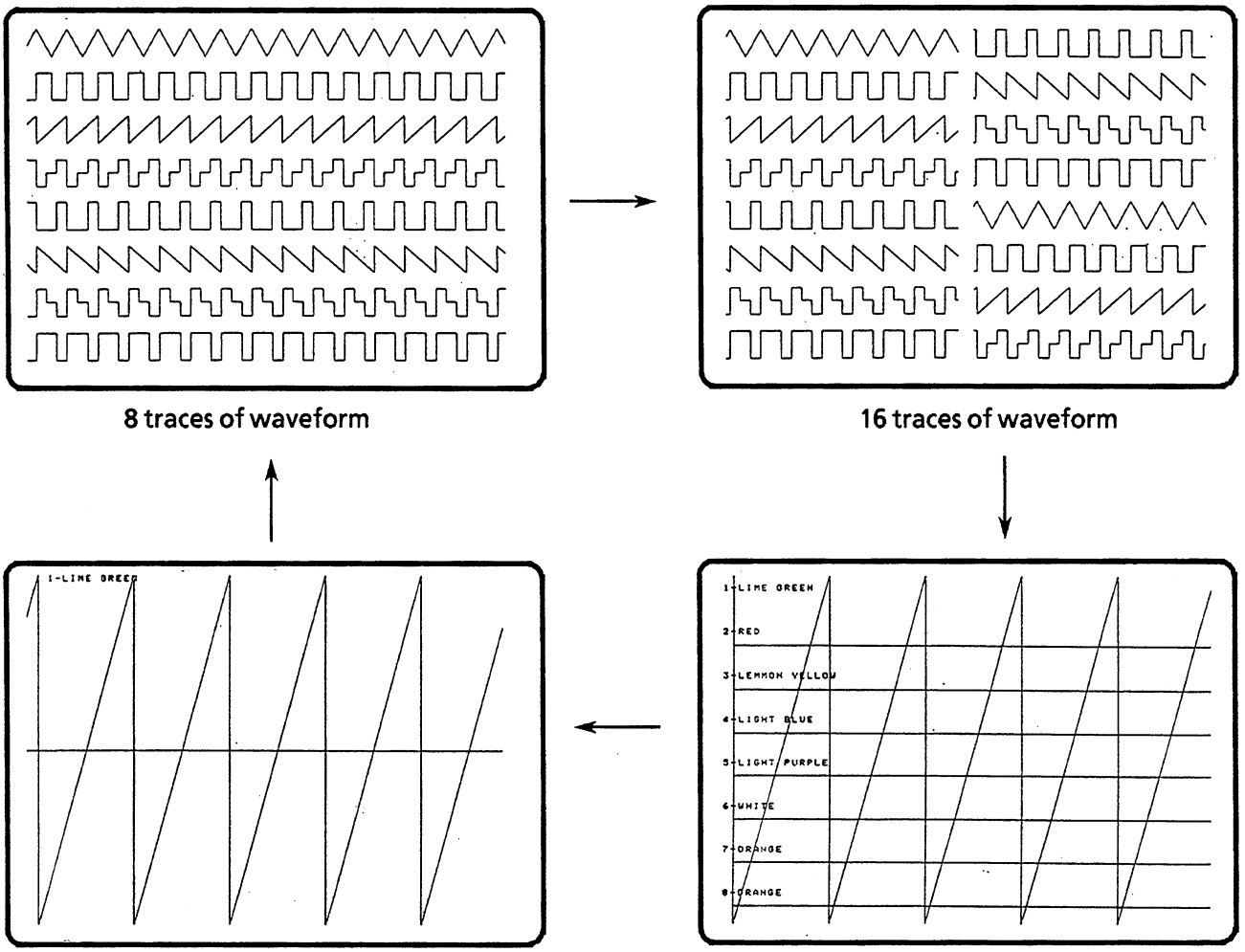


The Table-4 below shows the function of each shaded keys in this check mode.

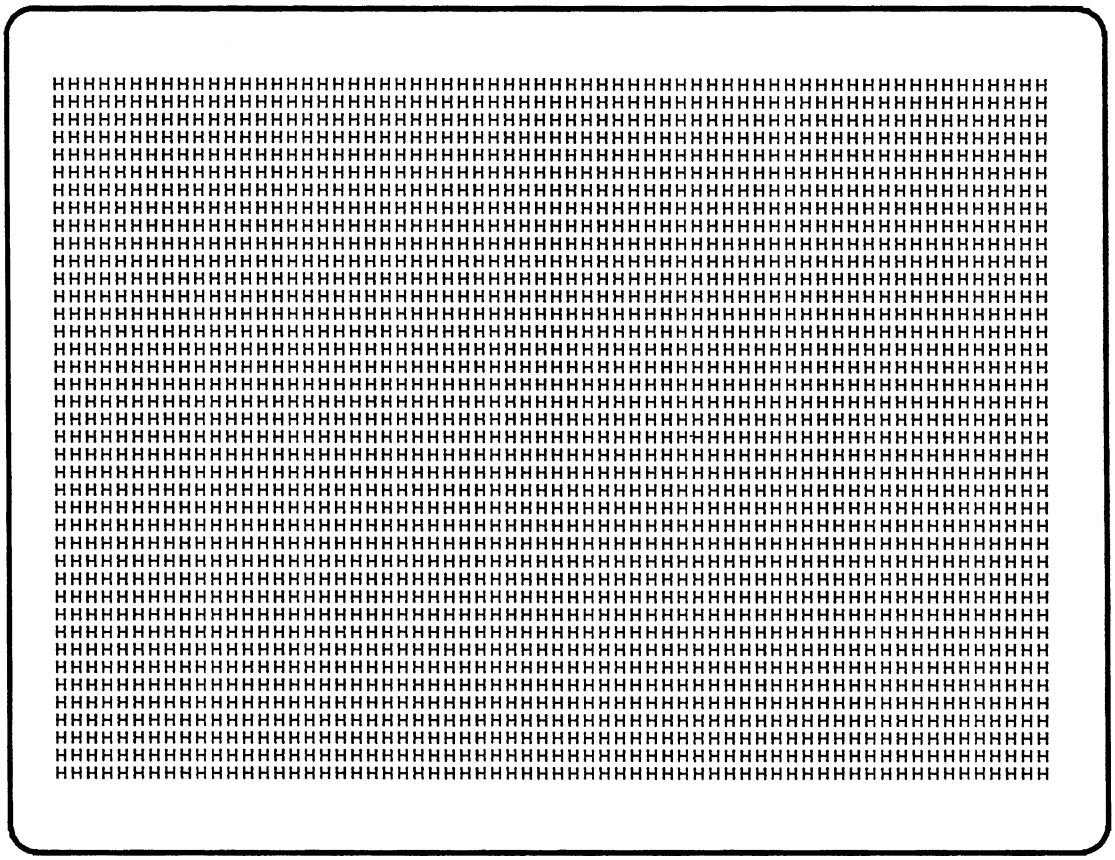
[TABLE - 4]

Key	Function
F1	Changes the wave display screen.
F2	Switches ON/OFF the trace waveform one by one.
F3	Sweeping /freezing the trace waveform.
F4	Changes the color of the trace waveform (only available when the wave display screen shows t8 traces of waveform).
F5	Not used.
F6	To return to the CRTC CHECK MENU

The wave display screen changes when the F1 key is pressed repeatedly.



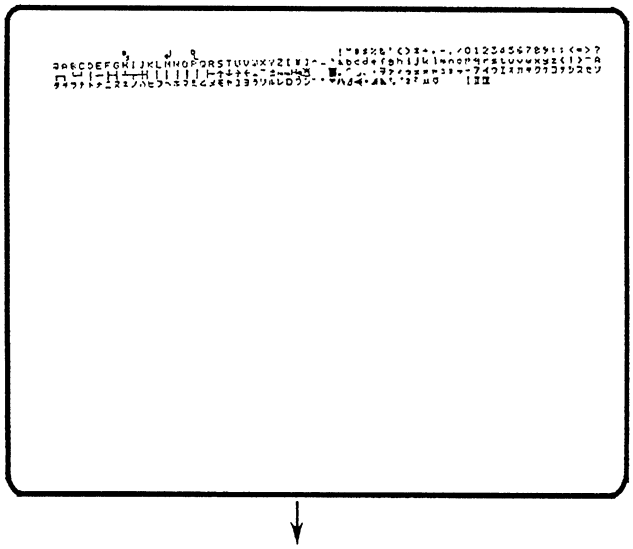
- **CHARACTER DISPLAY check**
  The following CHARACTER DISPLAY appears on the display unit screen.



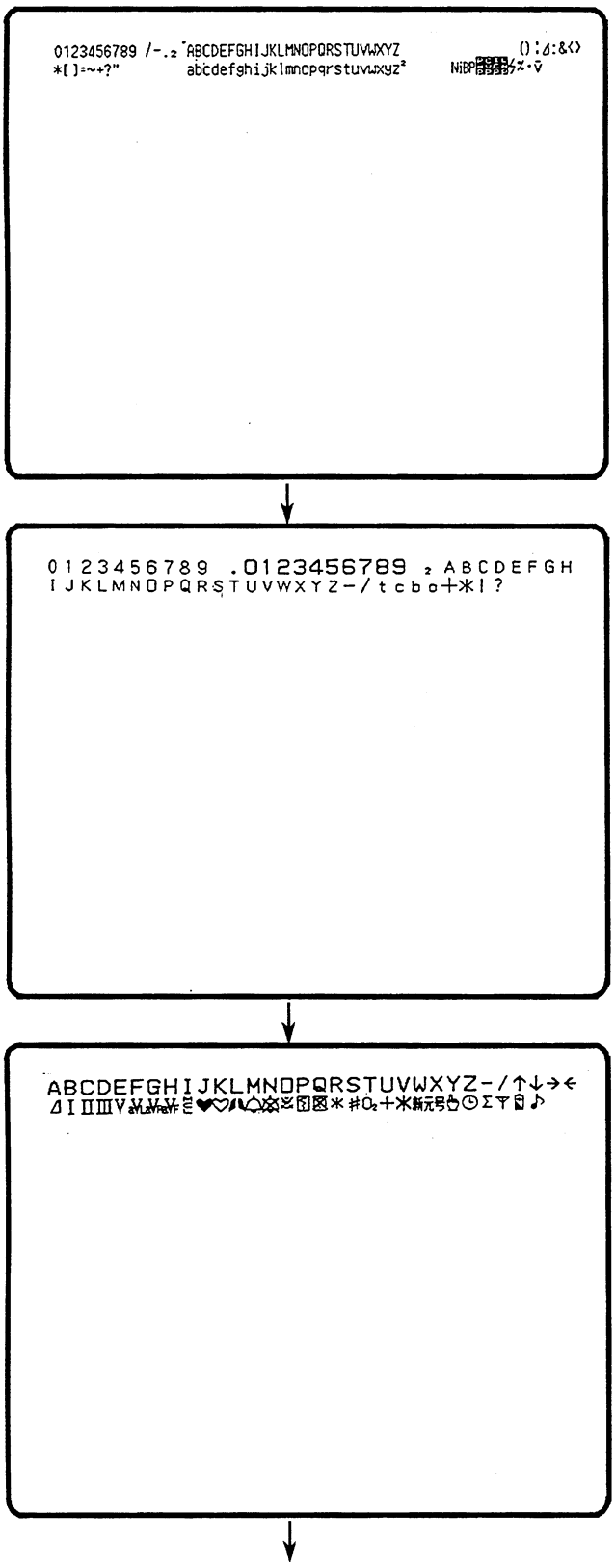
By pressing F2 key repeatedly, the display mode changes as follows:

1) Normal
2) Reversed light
3) Reversed blink

By pressing the F1 key repeatedly, the character pattern changes as follows:



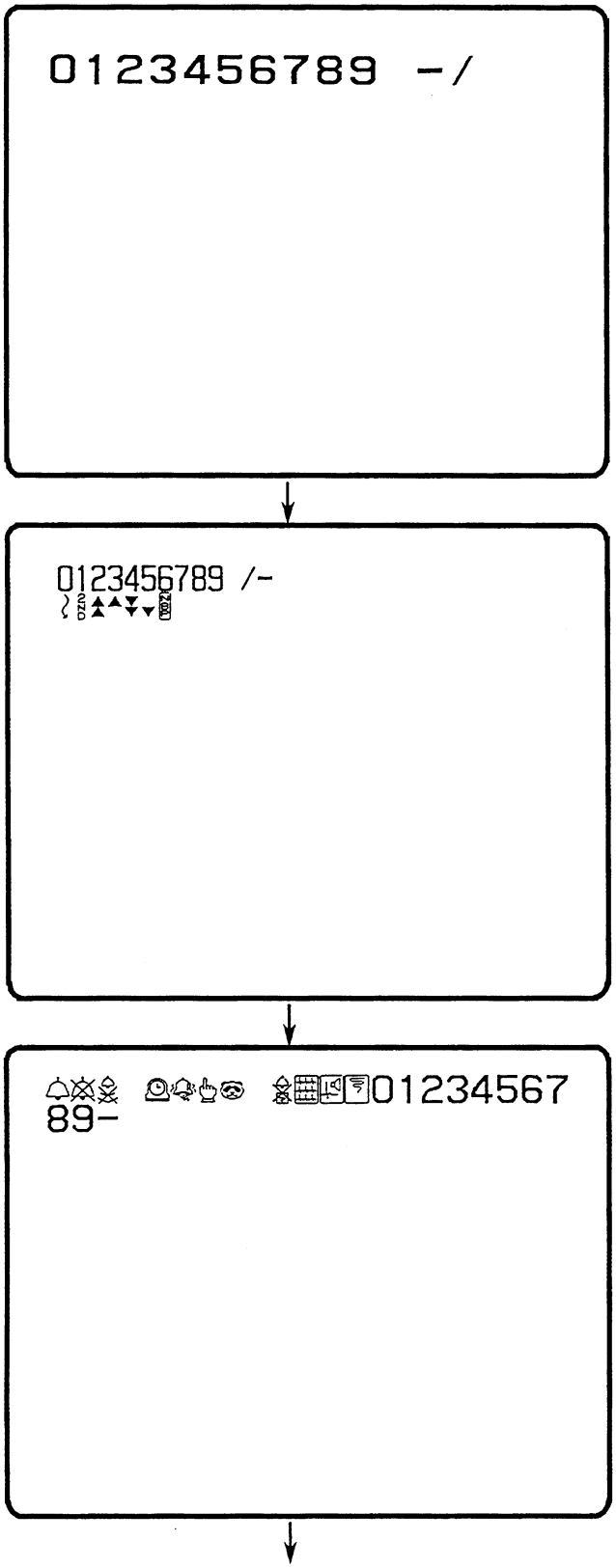
This display appears when the F1 key is pressed for the fifteenth times.



This display appears when the F1 key is pressed for the sixteenth times.
By pressing the F1 key from the seventeenth, the Japanese character display appears.

This display appears when the F1 key is pressed for the eighteenth times.
By pressing the F1 key from the nineteenth to the twenty-second times, the Japanese character displays appear.

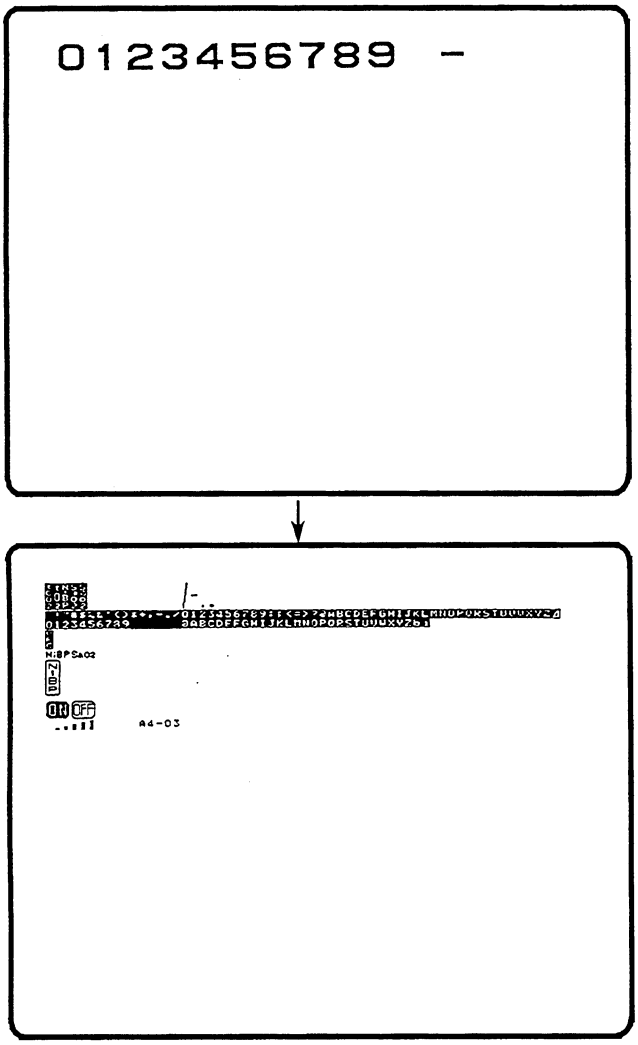
This display appears when the F1 key is pressed for the twenty-third times.



This display appears when the F1 key is pressed for the twenty-fourth times.

This display appears when the F1 key is pressed for the twenty-fifth times.

This display appears when the F1 key is pressed for the twenty-sixth times.
By pressing the F1 key from the twenty-seventh and twenty-eight times, the Japanese character displays appear.

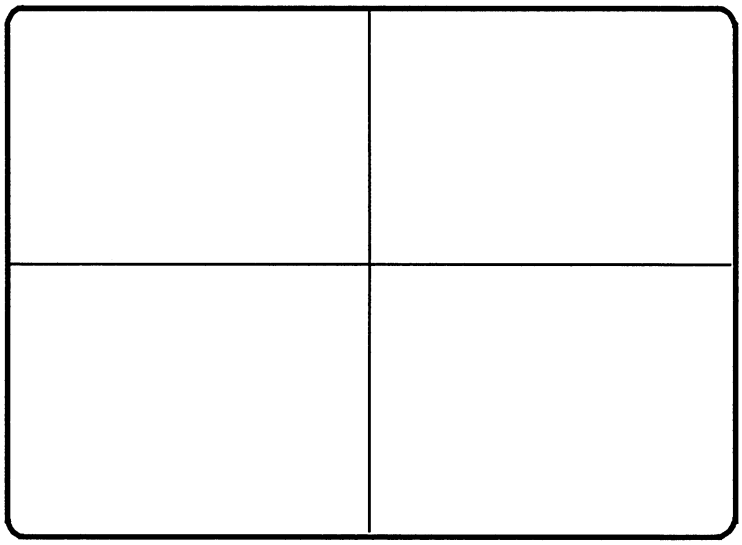


This display appears when the F1 key is pressed for the twenty-ninth times.

This display appears when the F1 key is pressed for the thirtieth times. This is the last of the character display screen. When the the F1 key is pressed for the thirty-first times, the display screen returns back to the display shown on page 4.32.

- **GRAPHIC DISPLAY check**

  The following graphic display appears on the CRT.

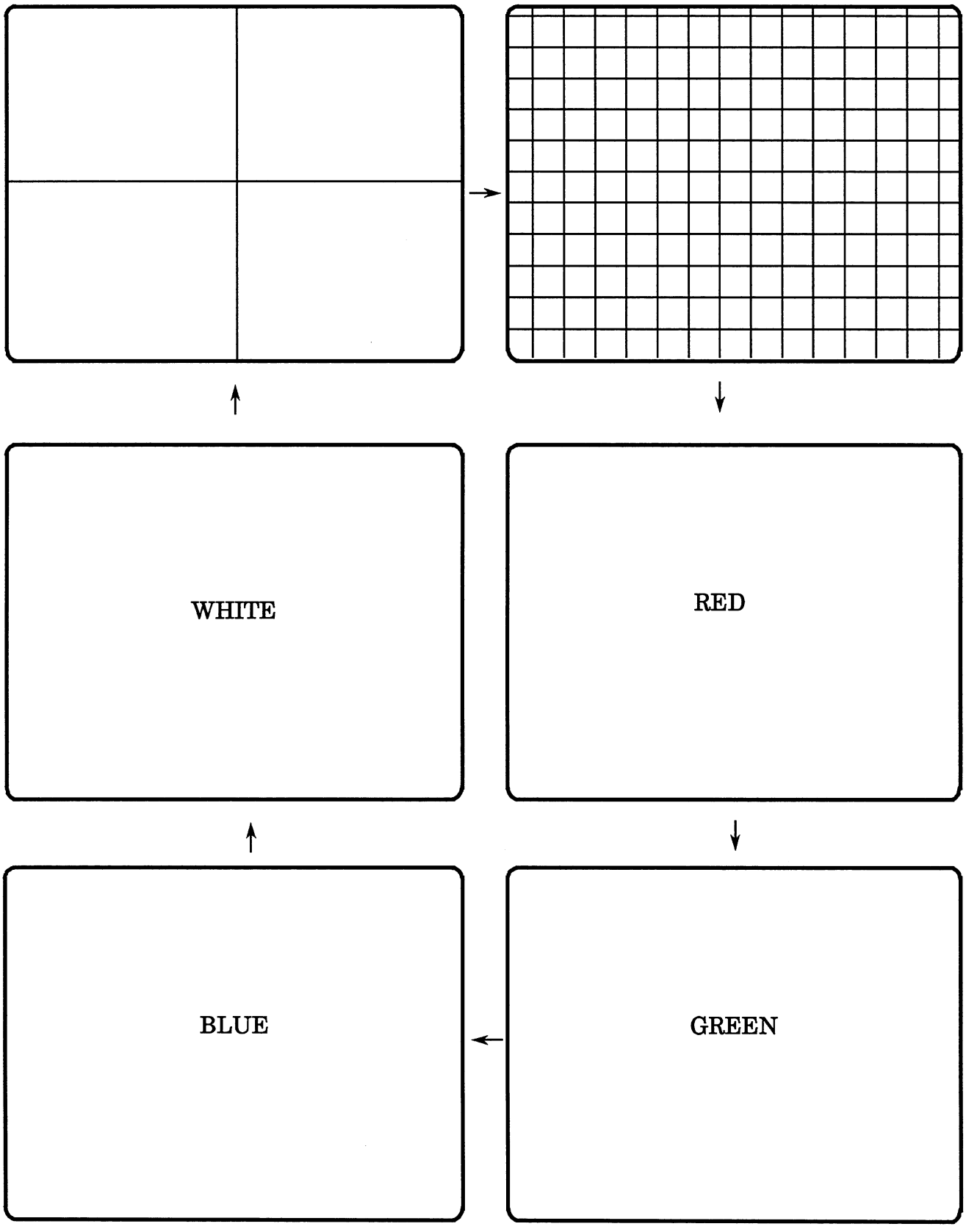


The Table-5 shows the function of the F1 ~ F6 keys in the GRAPHIC DISPLAY check mode.

[TABLE - 5]

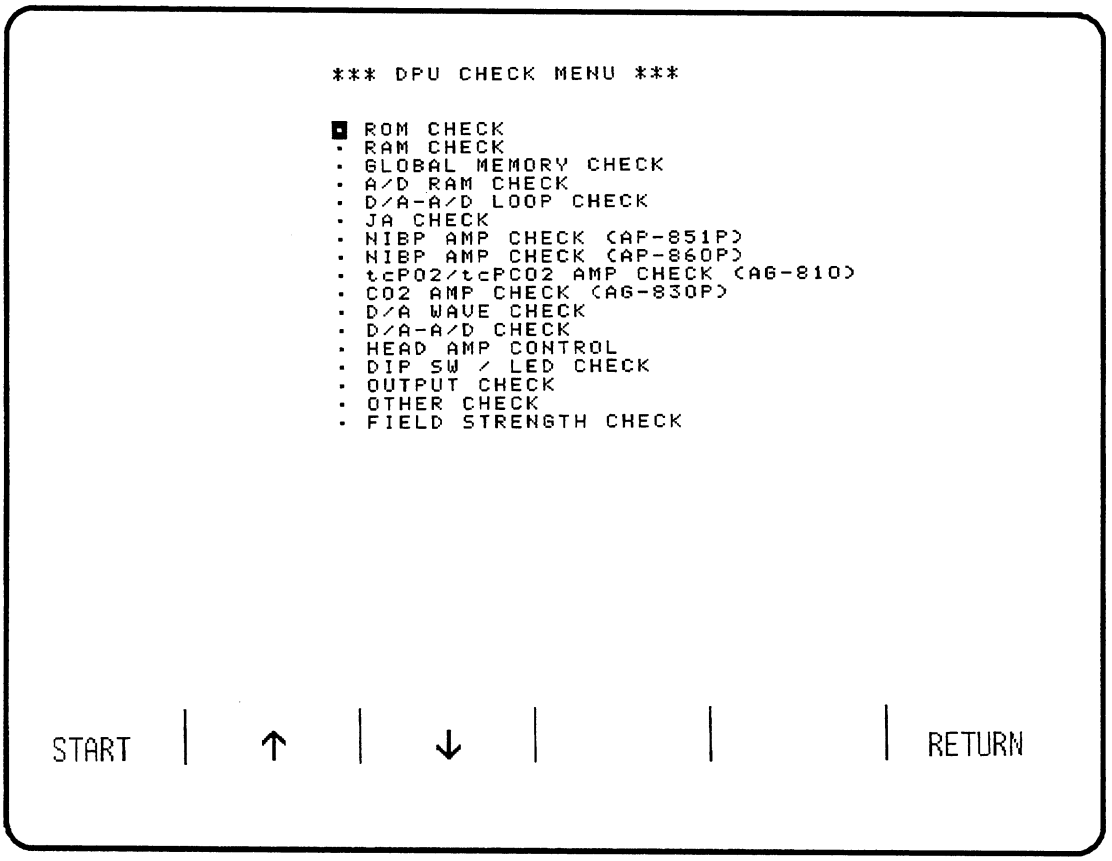
Key	Function
F1	Changes the graphic display screen.
F2	Move the screen downward.
F3	Move the screen upward.
F4	Move the screen to the left.
F5	Move the screen to the right.
F6	To return to the CRTC CHECK MENU

By pressing F1 key, the display changes as follows:



◆DPU (Data Processing Unit board) check

The following display appears on the CRT by first pressing the REVIEW key and then pressing the "DPU CHECK" multifunction key in the CHECK MENU display.



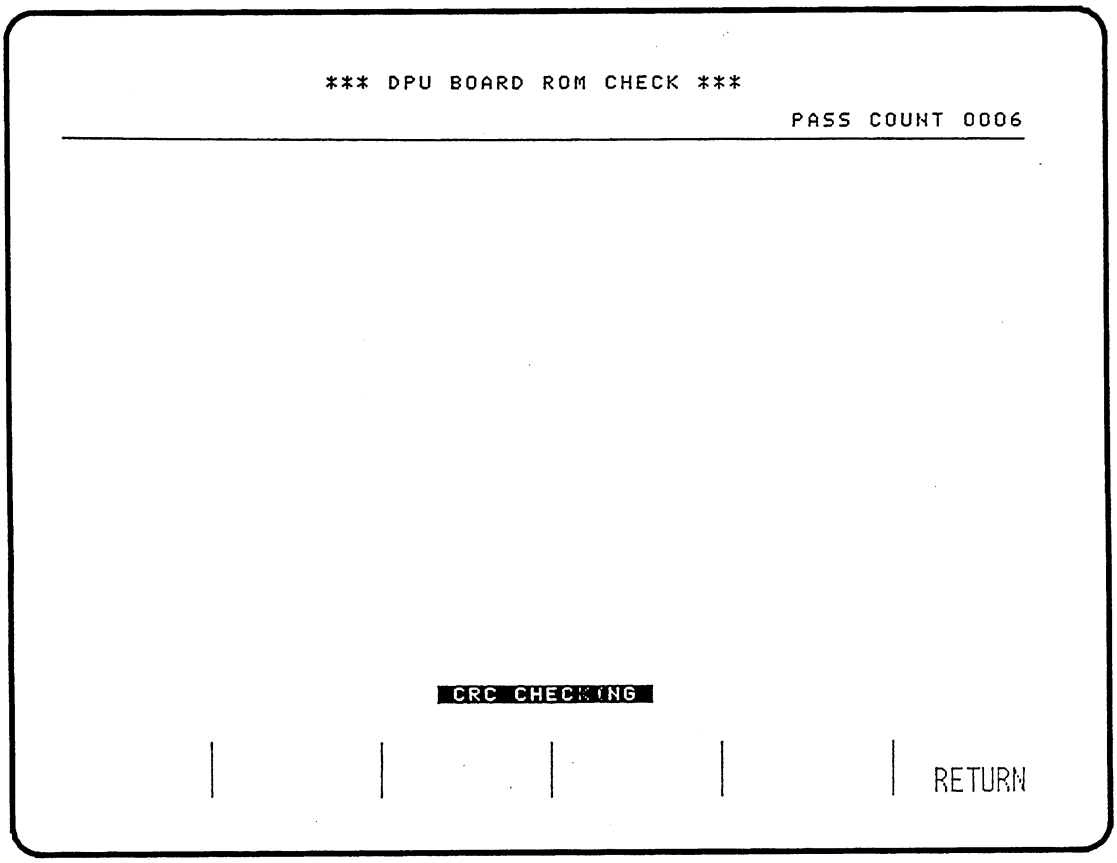
On the above display,

↑ ↓: to select a check item from the check items on the CRT

START: to execute the program for a selected check item while changing to the display for the check item

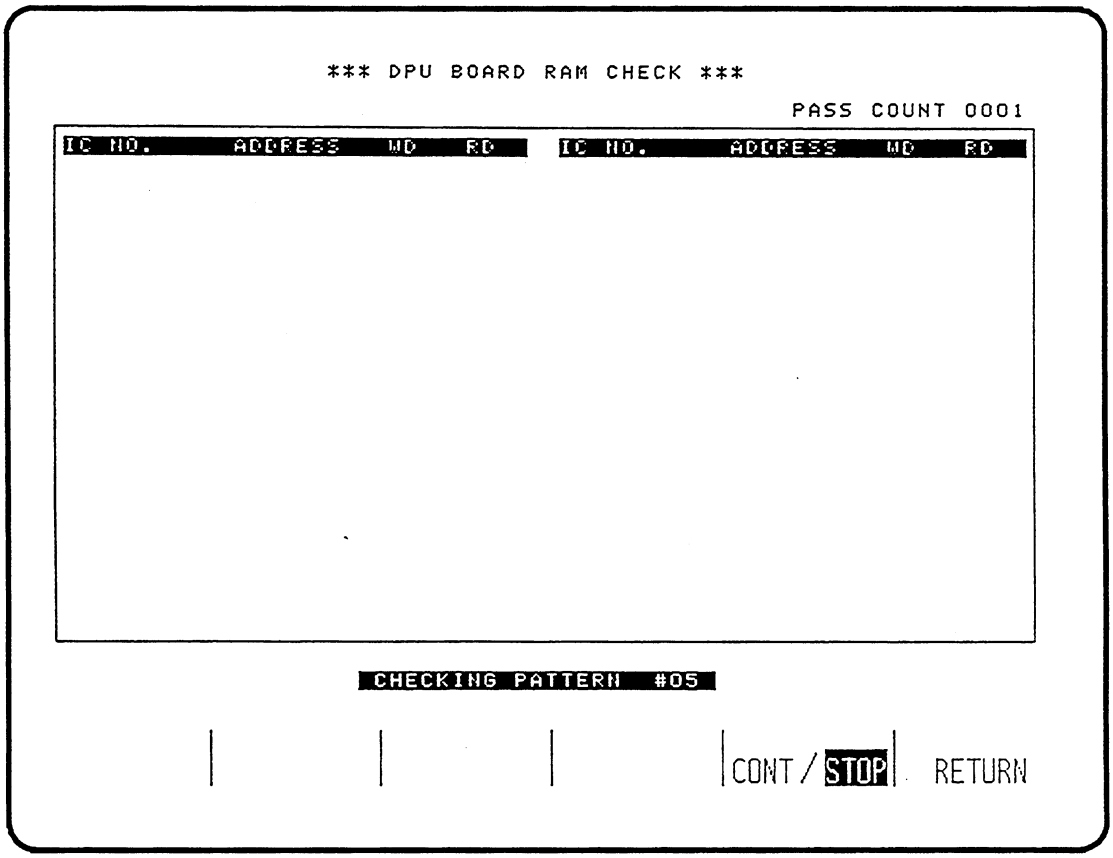
RETURN: to return to the CHECK MENU display

- **ROM check**



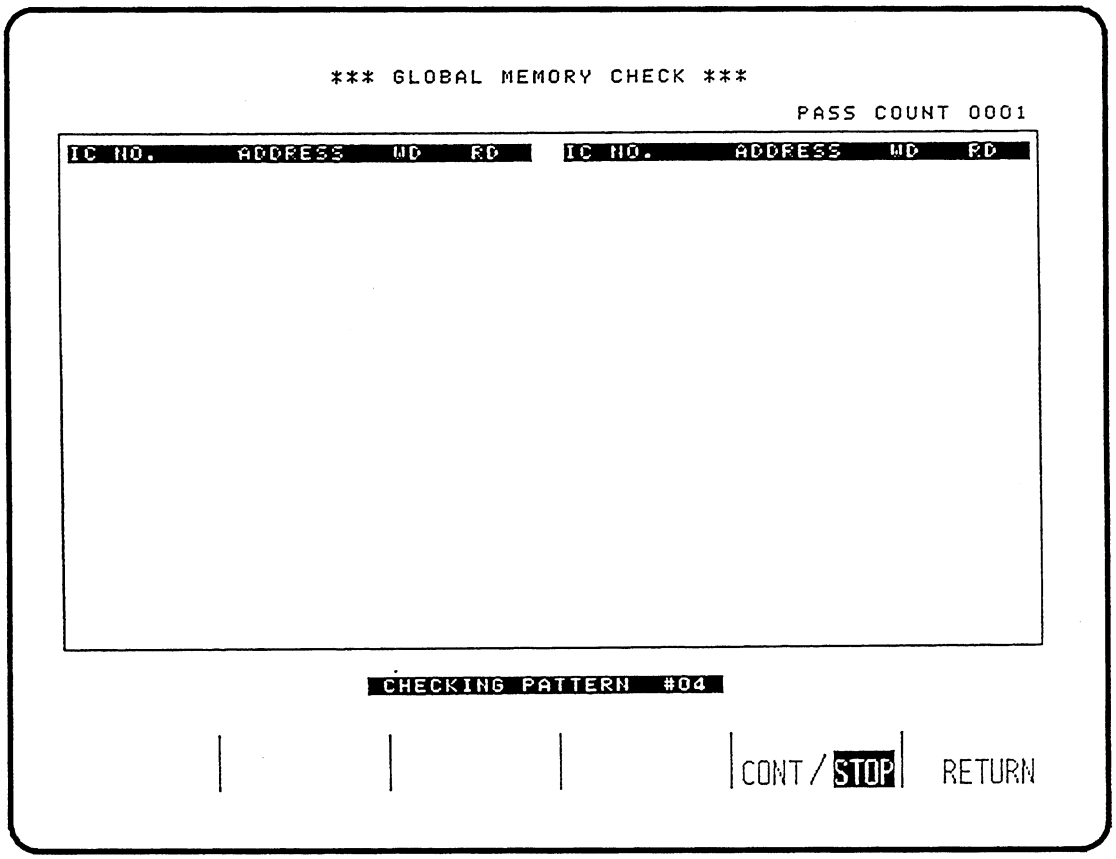
"CRC CHECKING" message blinks during the checking.
The check is executed with C.R.C. similar to the ROM CHECK on the CPU board.

- **RAM check**



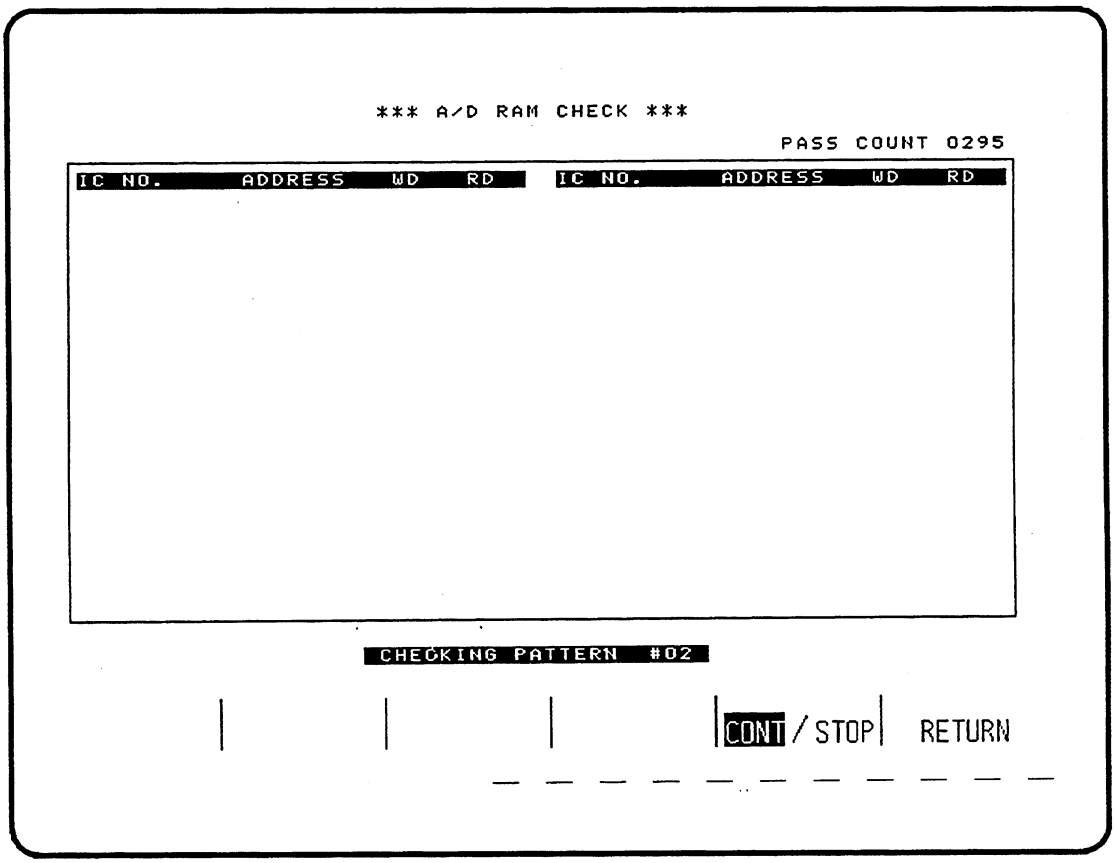
"CHECKING PATTERN #XX" message blinks during the checking. Patterns No. 1 to 15 of Table-1 are used as the check pattern. The check is the same as the RAM CHECK on the CPU board.

- **GLOBAL MEMORY check**



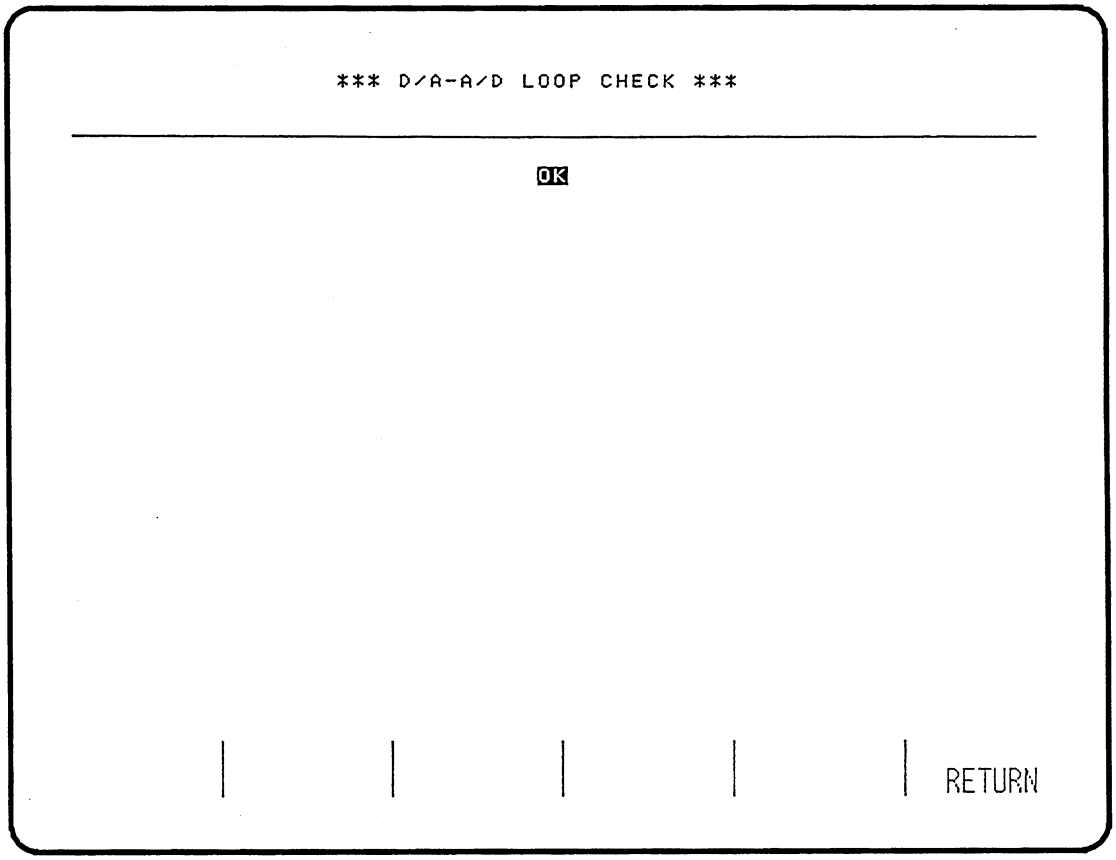
"CHECKING PATTERN #XX" blinks during the checking.
Patterns No. 1 to 15 of Table 1 are used as the check pattern. The check is the same as the GLOBAL MEMORY CHECK on the CPU board.

- **A/D RAM check**



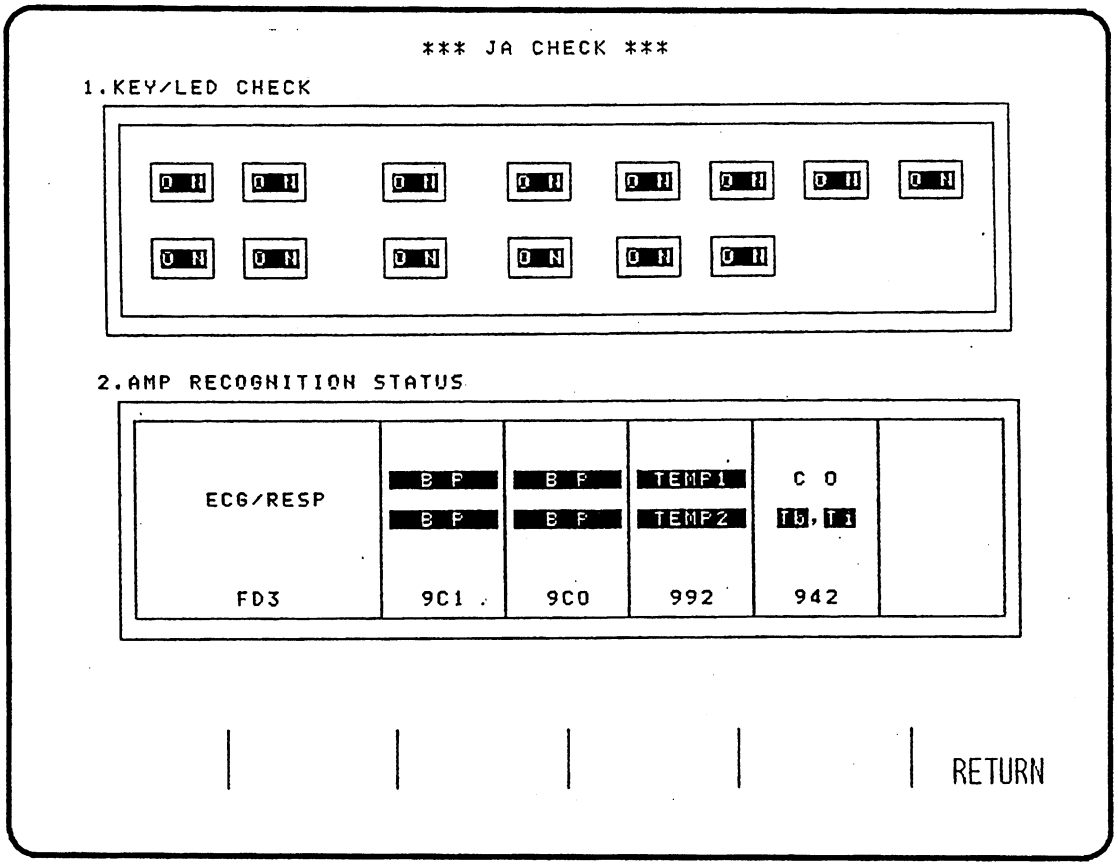
"CHECKING PATTERN #XX" blinks during the checking.
Patterns No. 1 to 15 of Table 1 are used as the check pattern. The check is the same as the RAM CHECK on the CPU board.

- **D/A - A/D Loop check**



The result after checking the D/A - A/D LOOP, "OK" or "ERROR" is indicated. The check is the same as the D/A - A/D LOOP CHECK on the A/D - D/A CHECK display.

●JA check (Input Box check)



1) KEY / LED CHECK

The "OFF" marks located according to the key switches on the operation panel of the Input box (JA-860PA/880PA) appear on the CRT. When a key switch is normal, the "OFF" mark changes to a reverse-lit "ON" mark accompanied by a high tone by pressing the key.

2) AMP RECOGNITION STATUS

When certain head-amplifiers are mounted, the amplifier name is indicated in the appropriate location. If an amplifier is not prepared for measurement, the indication is reverse-lit.

When a head-amplifier is not mounted, the corresponding position is blank. (See the right side of "CO Tb Ti 942" of above.)

NOTE

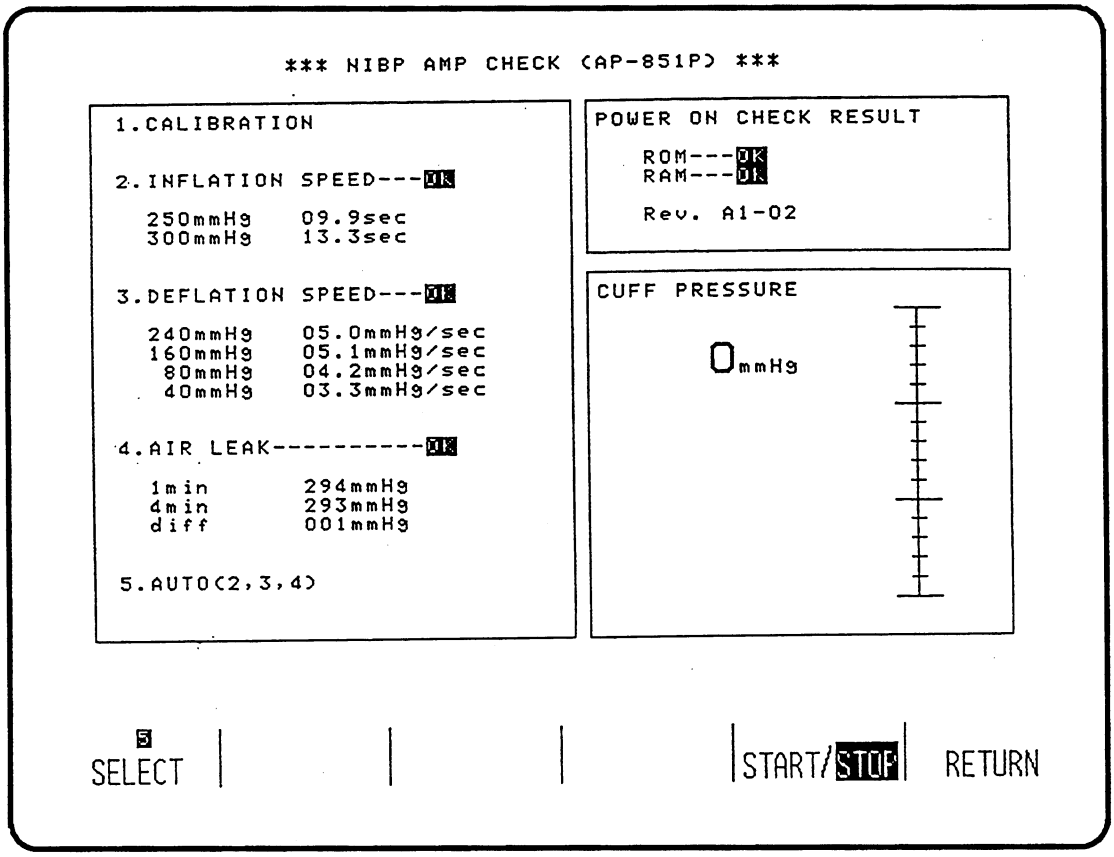
a) The ECG/RESP. head amplifier must be located next to the male receptacle for the connection cable between the input box and the main unit.

b) When one BP (Blood Pressure) head amplifier is mounted, the BP amp must be located next to the ECG/RESP. amp.

c) When the other BP amp is mounted, it must be located next to the BP amp already installed.

d) When no BP amp is mounted, the other head amplifier can be installed in any of the 5 slots of the JA-860PA Input Box, or, any of the 7 slots of the JA-880PA Input Box.

- **NIBP AMP check (AP-851P)**



Approx. 10 sec after this mode is called up, the ROM and RAM check results, and software revision are displayed. Check items 1 to 5 require the dummy cuff chamber — a hermetically sealed box of 800 cc internal volume which is not deformed by a 300 mmHg pressure. Press the "SELECT" multifunction key to select the check item.

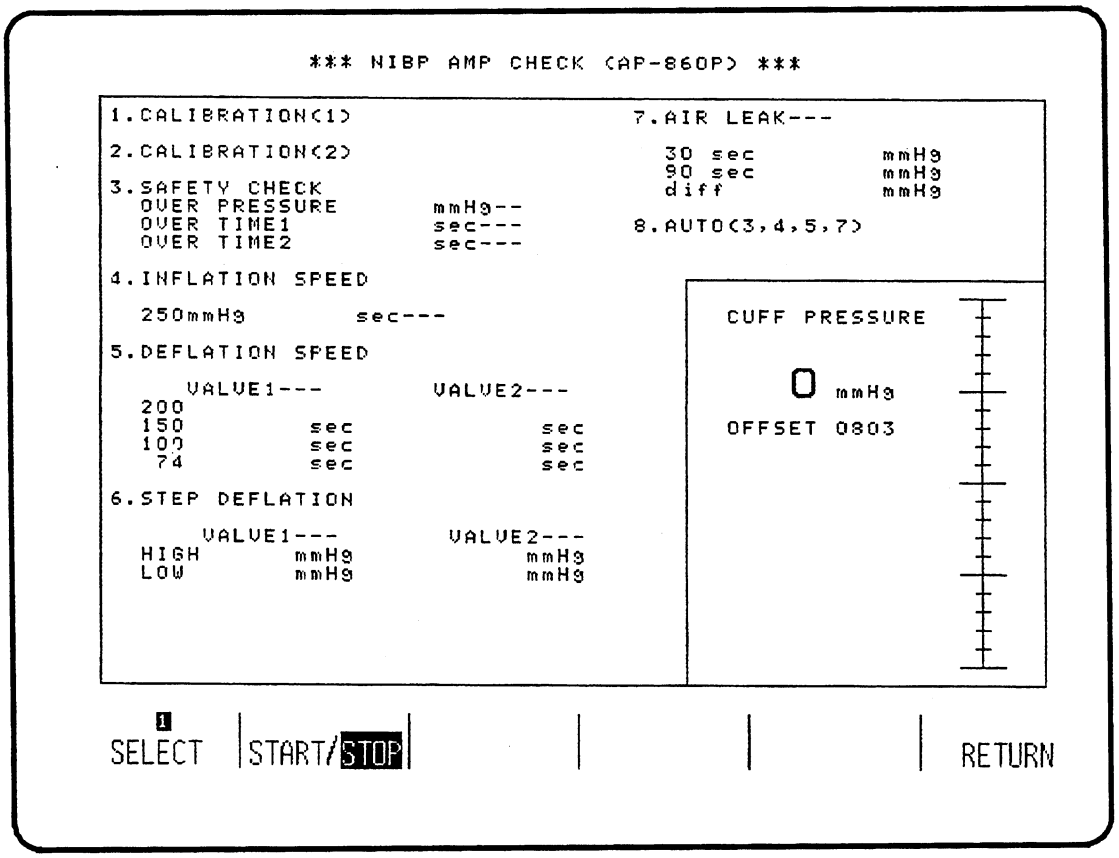
Calibration

1. Connect the dummy cuff to the air hose connector.
2. Press the "START/STOP" multifunction key to start pressure inflation. Wait until the pressure becomes 180 mmHg.
3. Disconnect the dummy cuff from the air hose connector.
4. Connect the mercury manometer and external pump using the Y-tube joint.
5. Increase the pressure of the dummy cuff. Compare the reading on the manometer and the screen. Tolerance is ±3 mmHg (10 ~ 200 mmHg) and ±4 mmHg (201 ~ 300 mmHg).

Auto check for inflation speed, deflation speed, and air leak (Manual is also available)

1. Connect the dummy cuff to the air hose connector.
2. Press the "START/STOP" multifunction key. Check items 2 to 4 are automatically performed. If within the following tolerances, "OK" is displayed.
   Inflation speed: 7 to 14 sec at 250 mmHg
   Deflation speed: 4.7 to 6.0 mmHg/s at 240 and 160 mmHg, 3.5 to 5.0 mmHg/s at 80 mmHg, 2.3 to 4.2 mmHg/s at 40 mmHg
   Air leak: ±3 mmHg difference between 1 min. and 4 min.

- **NIBP AMP check (AP-860P)**



WARNING

Do not connect the cuff to the patient when performing this check because some of the check programs in the NIBP AMP CHECK (AP-860P) menu exerts high pressure on the connected cuff.

Press the "SELECT" multifunction key to select the check item. If necessary, press the "START/STOP" multifunction key to start or stop the check of the selected check item.

1) CALIBRATION (1)

This check item requires an external hand bulb pump and a manometer to be connected to the two NIBP connectors on the NIBP head amplifier. Compare the pressure applied by the external pump on the manometer and that displayed on the NIBP AMP check display. Check whether the tolerance is within the values given in the table below, if not, performed the Pressure Gain Adjustment (refer to Sections 6-2-8).

Applied Pressure Range	Tolerance
0 ~ 150 mmHg	±3 mmHg
150 ~ 290 mmHg	±2% reading

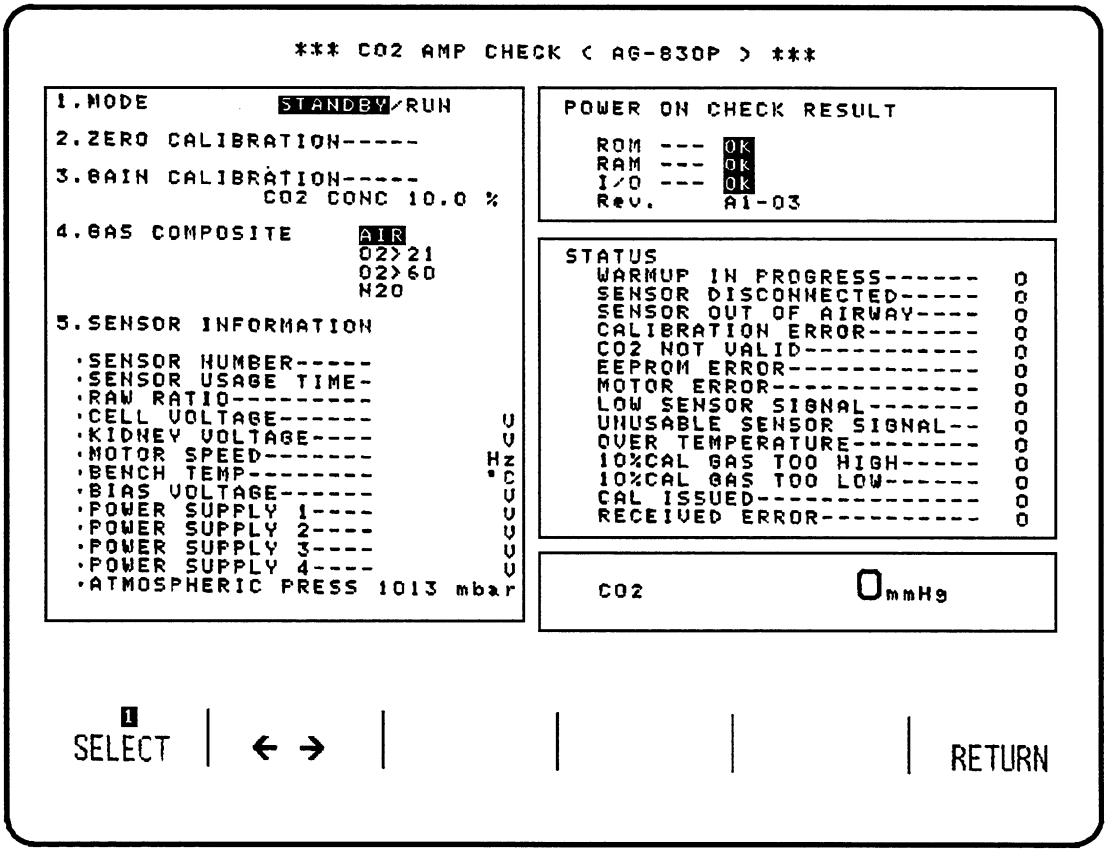
2) CALIBRATION (2)

The function of this check item is the same as that of CALIBRATION (1).

NOTE

Check items No. 3~8 are used in the factory during the production of the bedside monitor. Do not use these check items in the field.

- **CO2 AMP check (AG-830P)***



*** Not available in the U.S.**

The CO2 AMP check item consists of the following:

1) Power On check

The power on check checks the ROM, RAM, and input/output devices in the CO_2 head amplifier every time the CO2 AMP check is performed. The ROM, RAM, and input/output device checks are the same as those in the main unit of the bedside monitor. The result of the check is shown on the CO2 AMP check display.

2) CO_2 head amplifier status display

Set the mode of the SELECT item No. 1 to RUN to display the status of the CO2 head amplifier. A status value of "1" means "YES" and "0" means "NO".

3) CO_2 sensor information

In the RUN mode, select item No. 5 to display the CO_2 sensor information.

4) Calibration and setup items

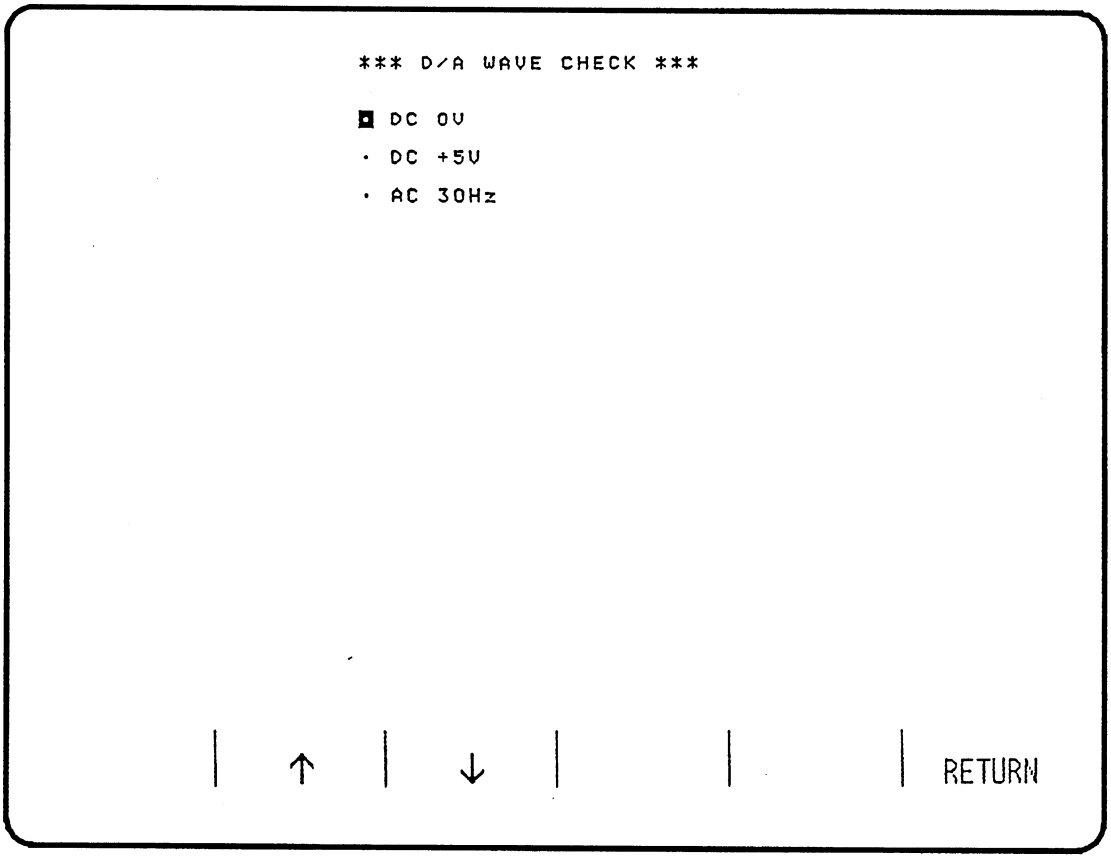
In the RUN mode, SELECT items No. 2 ~ 4 are used to calibrate and set the setting of the CO_2 head amplifier.

5) CO_2 measurement display

Set the mode of the SELECT item No. 1 to RUN to display the measured CO_2 gas pressure reading.

The following sections are displayed by pressing the "REVIEW" and MANUAL CHECK keys simultaneously on the DIAGNOSTIC CHECK AND SYSTEM SETUP display. These sections are for your reference, since these check program are for product inspection at the factory.

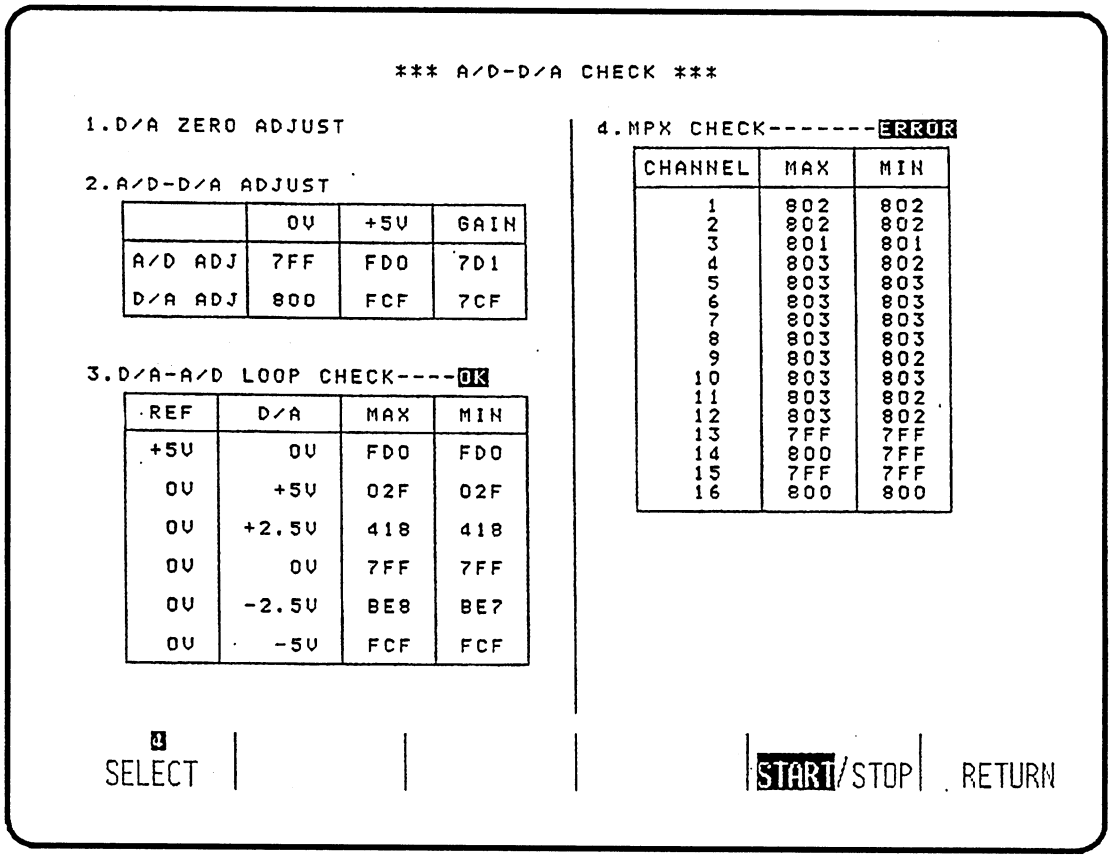
- **D/A WAVE check**



Check the waveform at the "DA" test pin (D/A converter output) on the DPU board. UP-0670 after selecting one of the following waveforms.

DC 0V: 0V is output at the test pin.
DC+5V: + 5V d.c. is output at the test pin.
AC 60/30Hz: $6V_{P-P}$ sine wave with 30.125 Hz is output for CH3 to CH8 at the test pin.
$6V_{P-P}$ sine wave with 60.25 Hz is output for ECG1W (CH1), ECG2 (CH2) at the test pin.
PSEUDO PACING WAVE: Pseudo pacing wave is output on ECG1 (CH1).

- **A/D - D/A check**



	0V	+5V	GAIN
A/D ADJ	7FF	FD0	7D1
D/A ADJ	800	FCF	7CF

REF	D/A	MAX	MIN
+5V	0V	FD0	FD0
0V	+5V	02F	02F
0V	+2.5V	418	418
0V	0V	7FF	7FF
0V	-2.5V	BE8	BE7
0V	-5V	FCF	FCF

CHANNEL	MAX	MIN
1	802	802
2	802	802
3	801	801
4	803	802
5	803	803
6	803	803
7	803	803
8	803	803
9	803	802
10	803	803
11	803	802
12	803	802
13	7FF	7FF
14	800	7FF
15	7FF	7FF
16	800	800

SELECT: to select a check item from check items No.1 to 4.
START/STOP: to start or stop the check program for a selected item.

1) D/A ZERO ADJUST
The D/A converter output is set to 0V for the zero adjustment.

2) A/D - D/A ADJUST
[A/D ADJ]
When the D/A converter output voltage is set to 0V and the reference voltage (REF.) of the D/A converter is 0V or 5V, the respective A/D converter output value is indicated by the hexadecimal code in the table.

GAIN = (A/D value in 5V REF.) - (A/D value in 0V REF.)

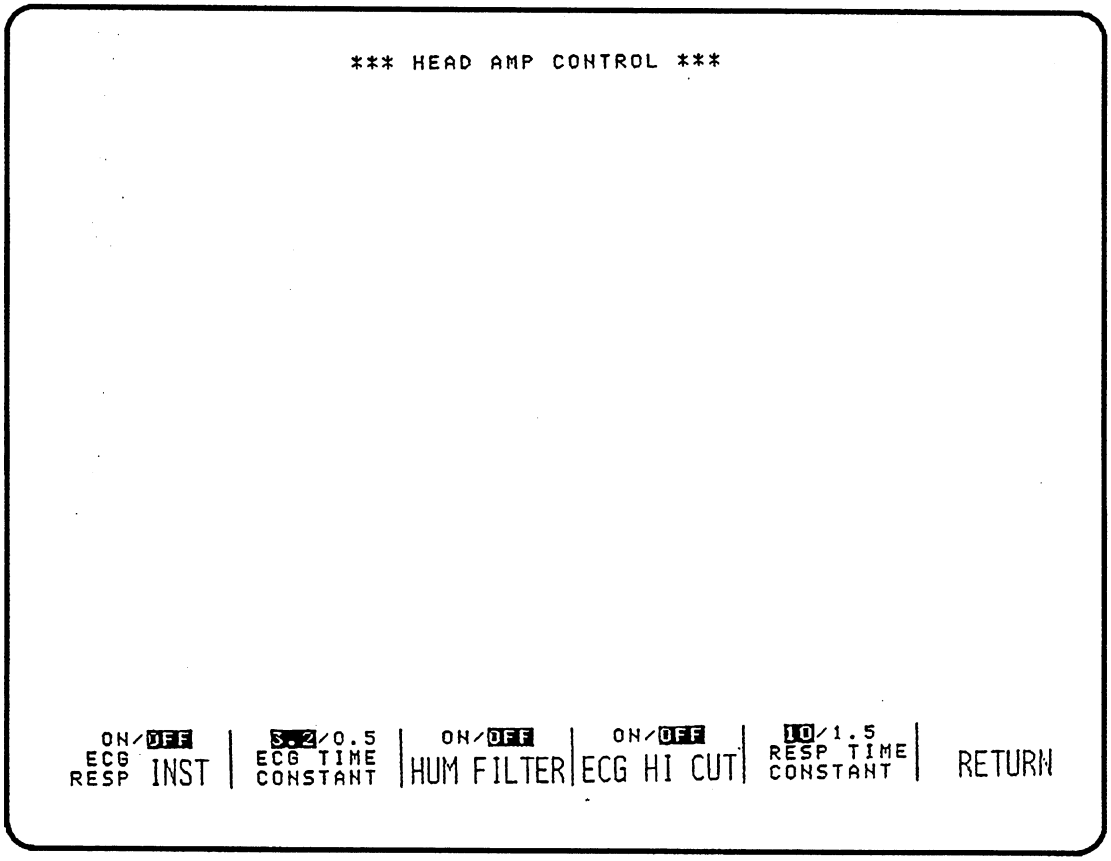
[D/A ADJ]
When the reference voltage of the D/A is set to 0V and the D/A output voltage is 0V or 5V, the A/D output value is indicated by the hexadecimal code on the table.

GAIN = (A/D value in 5V D/A out) - (A/D value in 0V D/A out)

3) D/A - A/D LOOP CHECK
When each REF. and D/A voltage is set as shown in the table, the maximum and Minimum values of the A/D output are indicated on the table after sampling the data. If the max. or min. value exceeds the regulated range, "ERROR" is indicated as shown in the table.

4) MPX CHECK (Multiplexer check) → Special jig is needed.
The input signals from the input box or the auxiliary input signals from external equipment (up to 16 channels) are switched for the one A/D with the two multiplexer in front of the A/D. The multiplexed signal is converted to a digital signal with the A/D converter. If the max. or min. value exceeds the regulated range, "ERROR" is indicated as shown next to "4.MPX CHECK".

- **HEAD AMP control**
  The ECG/RESP Head-amplifier condition can be selected on this display for factory inspection only.



ECG/RESP INST: ON/OFF selection of instantaneous short function against excessive voltage at the ECG/RESP input

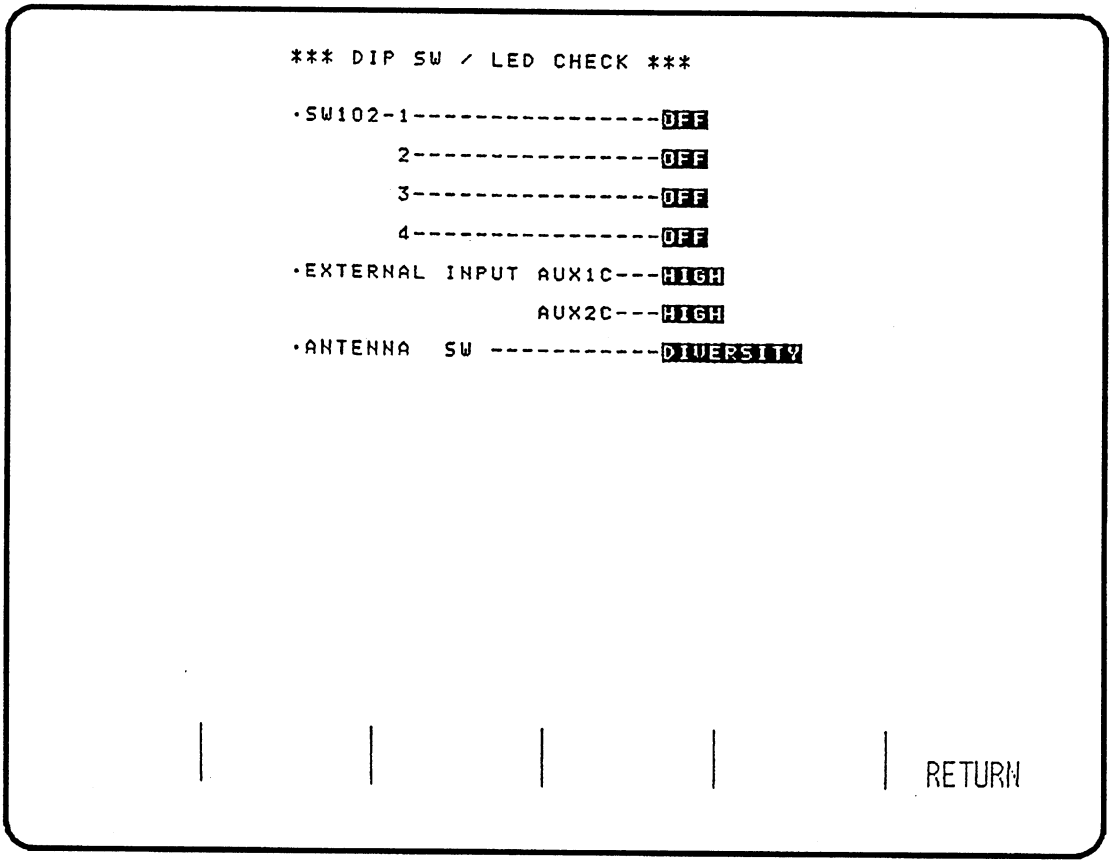
ECG TIME CONSTANT: 3.2 sec. / 0.5 sec. selection of time constant (low cut filter) for ECG

HUM FILTER: ON/OFF selection for ECG

ECG HI CUT: ON/OFF selection of high cut filter (40Hz) for ECG

RESP TIME CONSTANT: 10 sec./ 1.5 sec. selection of time constant for Respiration waveform

- **DIP SW/LED check**



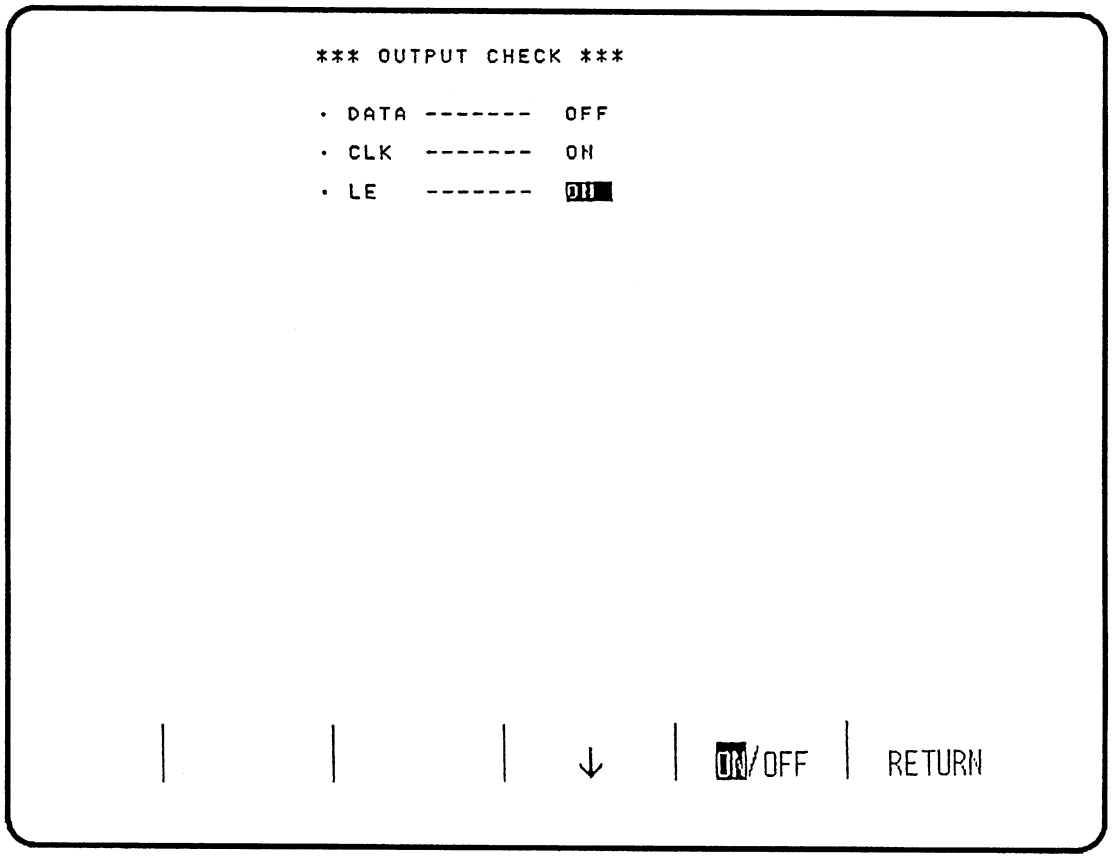
1) DIP SWITCH CHECK
The set condition of the dip switch on the DPU board, SW102, appears on the CRT.

2) EXTERNAL INPUT CONTROL SIGNAL CHECK
The control signals, AUX1C and AUX2C, must be indicated as "HIGH" when not connected with external equipment.

3) ANTENNA SWITCH CHECK
The switch condition of the antenna (ANT1, DIVERSITY) is displayed.

4) LED CHECK
Each LED on the DPU board sequentially lights and goes out one after another.

- **OUTPUT check**

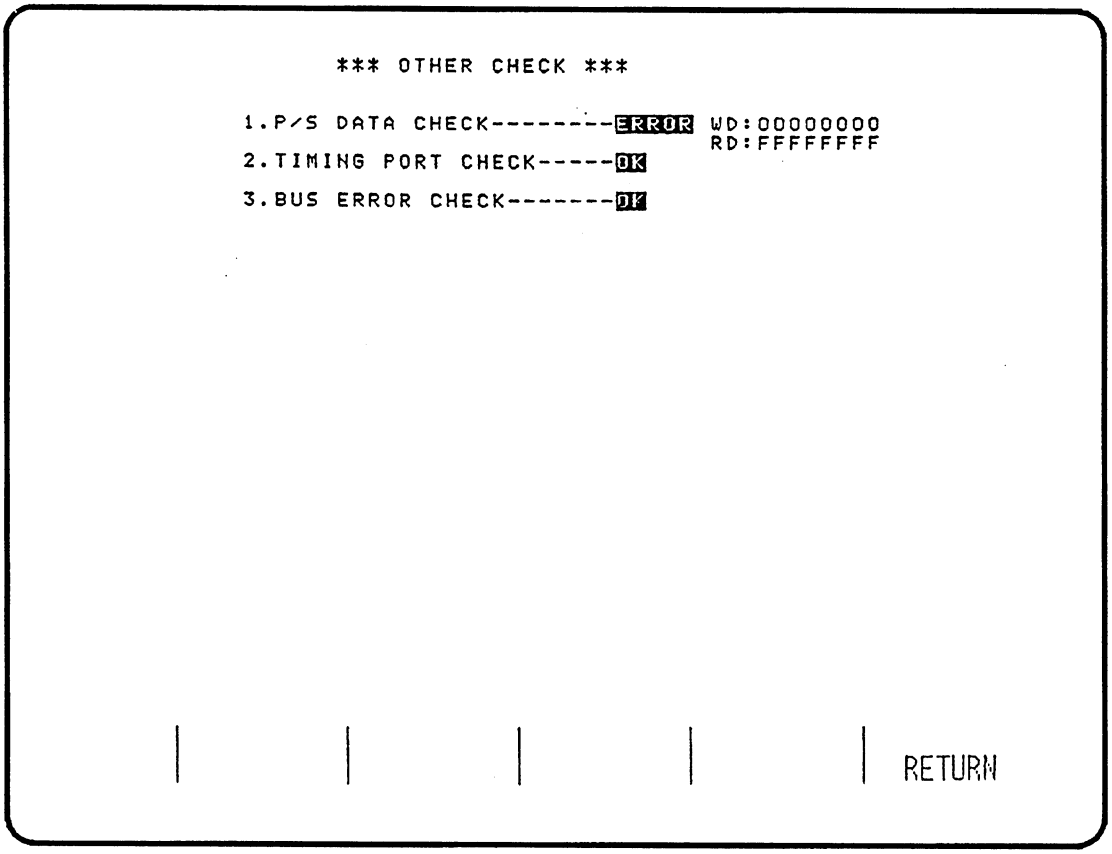


1) DATA CHECK
   High (ON) or Low (OFF) level signal is output.

2) CLK CHECK
   High (ON) or Low (OFF) level signal is output on CLK line.

3) LE CHECK
   High (ON) or Low (OFF) level signal is output on LE line.

- **OTHER check**

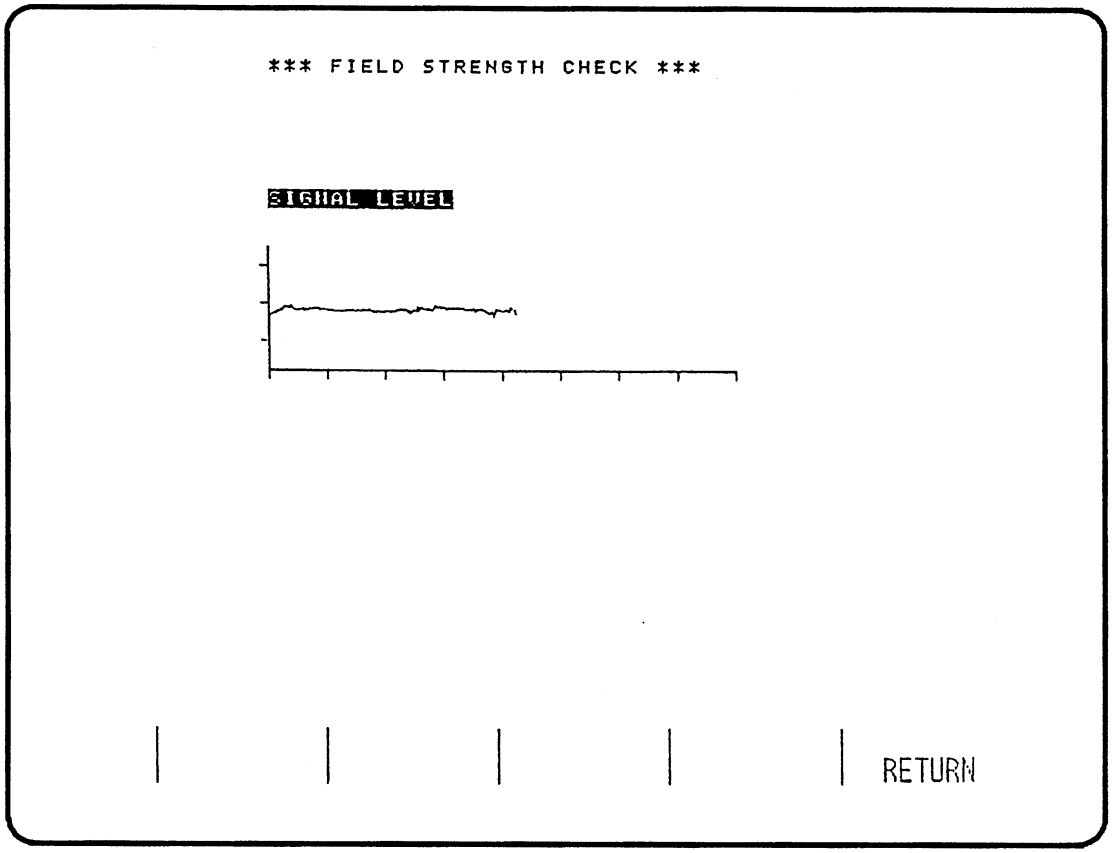


1) P/S DATA CHECK → jig for signal return is needed.
The check is executed by reading the S/P converter output via the jig instead of the input box after a 32bits data is inputted into the P/S converter.

2) TIMING PORT CHECK
The check is executed by confirming a increment of the data after reading a 4bits data of the Timing Port every 1 millisec.

3) BUS ERROR CHECK
The check is executed by confirming a Bus Error after accessing to the address where there is no memory area.

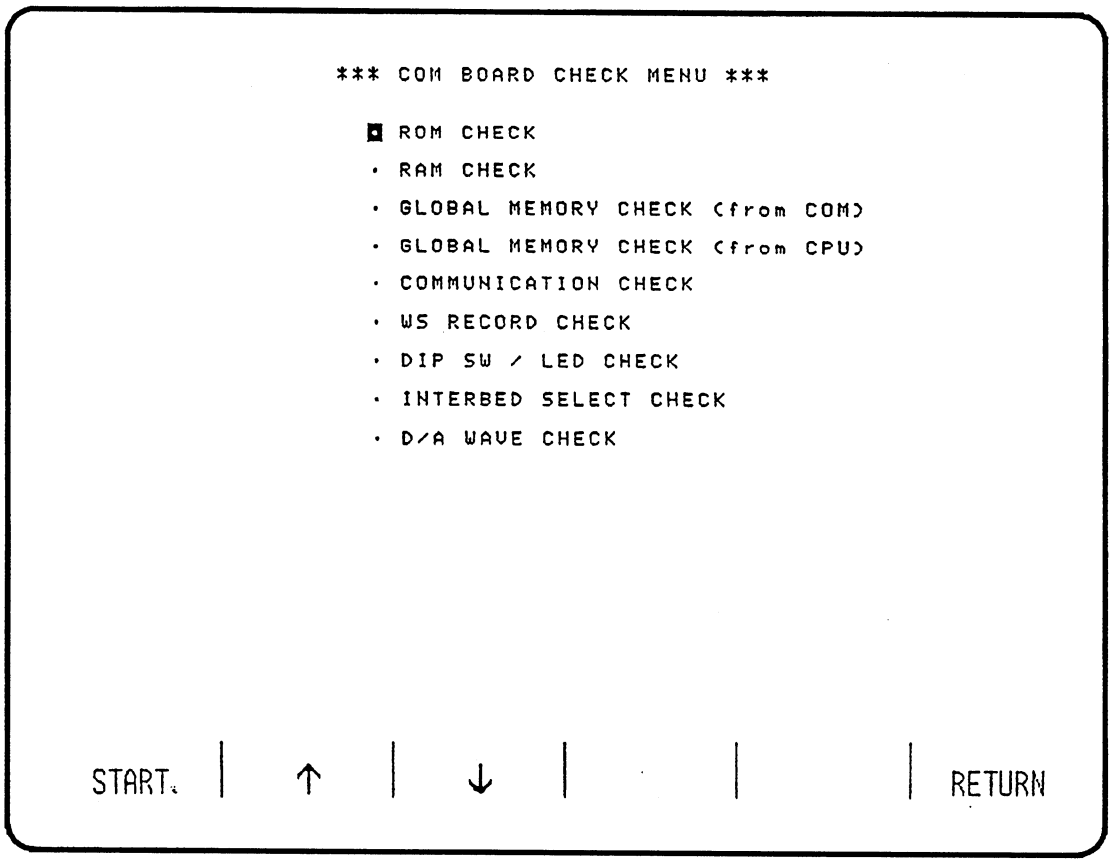
- **FIELD STRENGTH check**



Field strength of the receiving signal is displayed with a scale of 30 seconds.

◆COM check (Communication board check)

The following display appears on the CRT by first pressing the REVIEW key and then pressing the "COM CHECK" multifunction key in the CHECK MENU display.



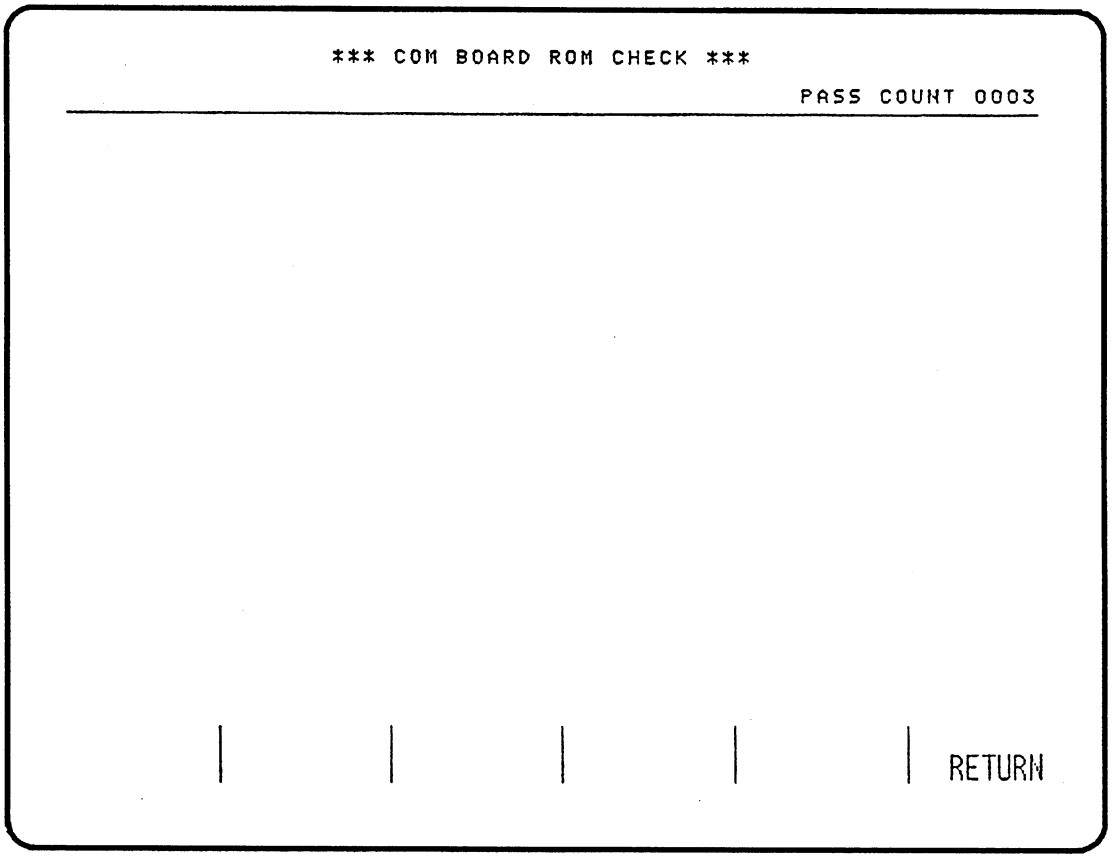
On the above display,

↑ ↓: to select a check item from the check items on the CRT

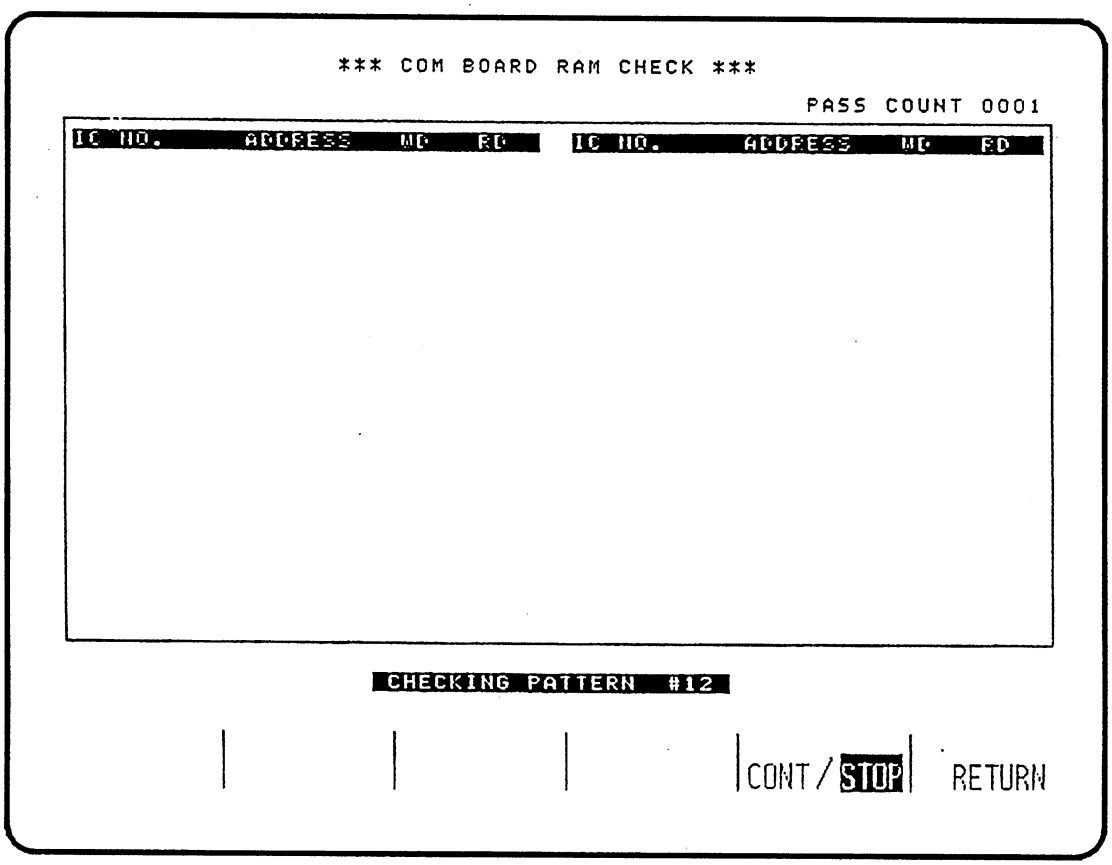
START: to execute the program for a selected check item while changing to the display for the check item

RETURN: to return to the CHECK MENU display

- **ROM check**
  The check is the same as the ROM check in "POWER-ON INITIAL SELF CHECK".



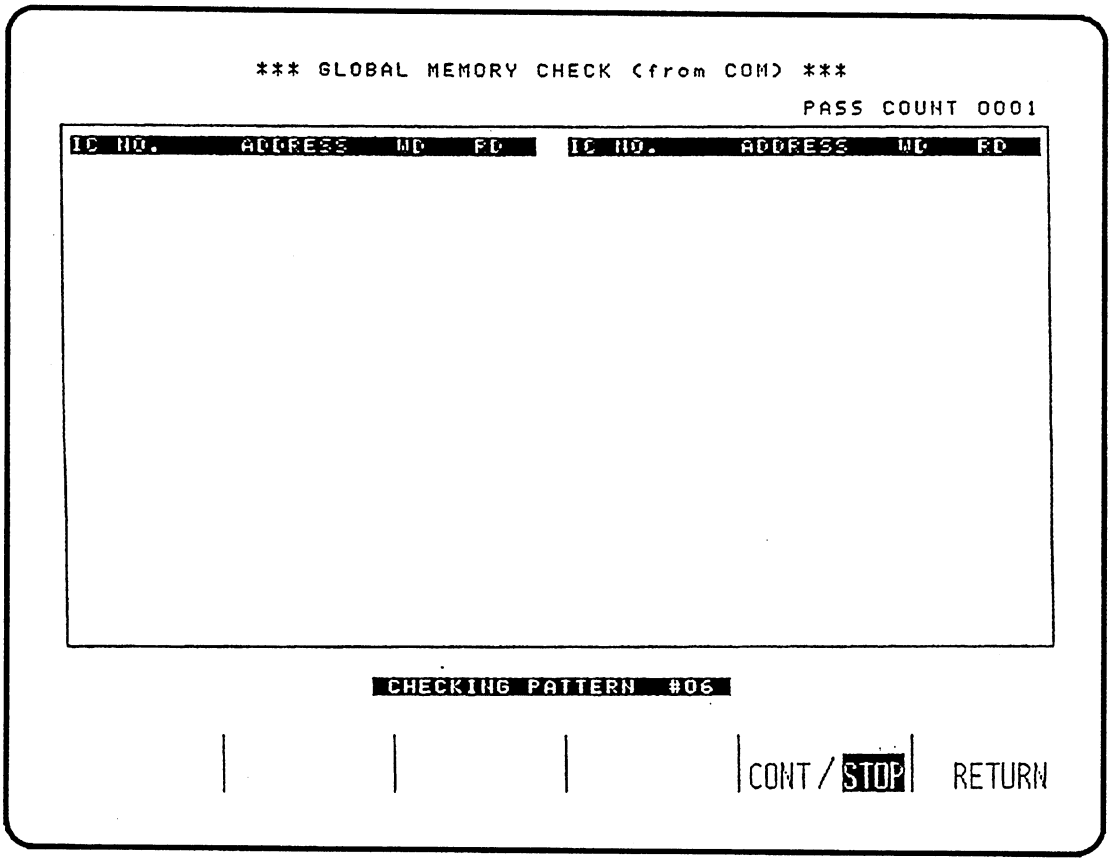
- **RAM check**



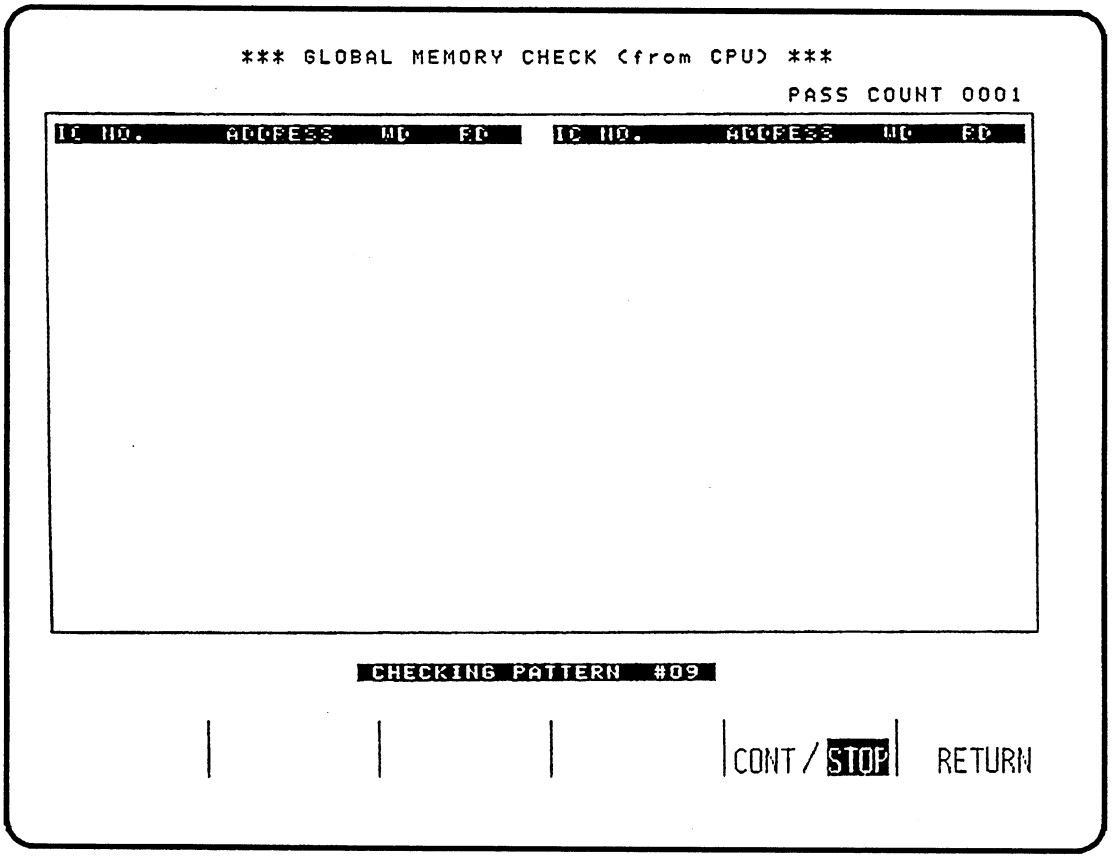
The following check patterns (No.1 to 20) are applied to this RAM check or the next GLOBAL MEMORY CHECK. The check is the same as the RAM CHECK on the CPU board.

No.	PATTERN	No.	PATTERN
1	55H	11	10H
2	AAH	12	EFH
3	01H	13	20H
4	FEH	14	DFH
5	02H	15	40H
6	FDH	16	BFH
7	04H	17	80H
8	FBH	18	7FH
9	08H	19	The same pattern as the COM RAM check pattern in "POWER-ON INITIAL SELF CHECK".
10	F7H	20	FFH

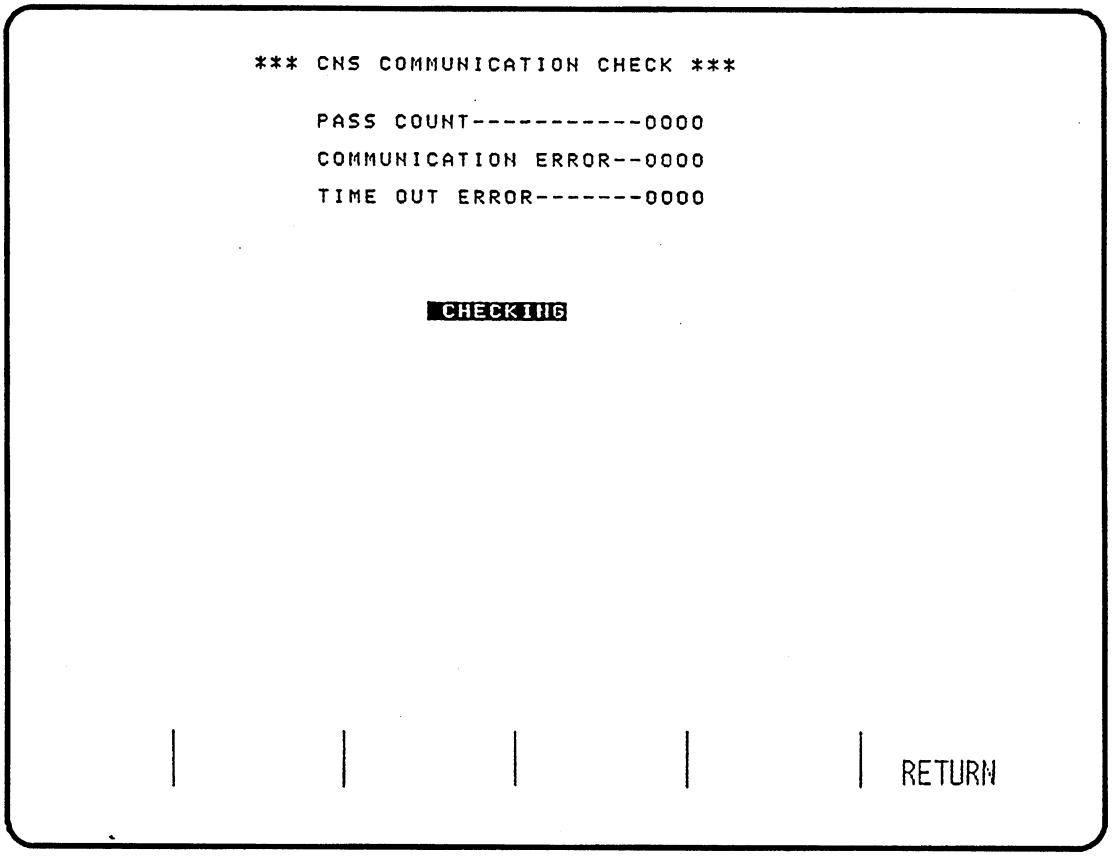
- **GLOBAL MEMORY check (from COM)**
  The Global memory is accessed from the MPU on the COM board. The check is the same as the RAM CHECK on the CPU board.



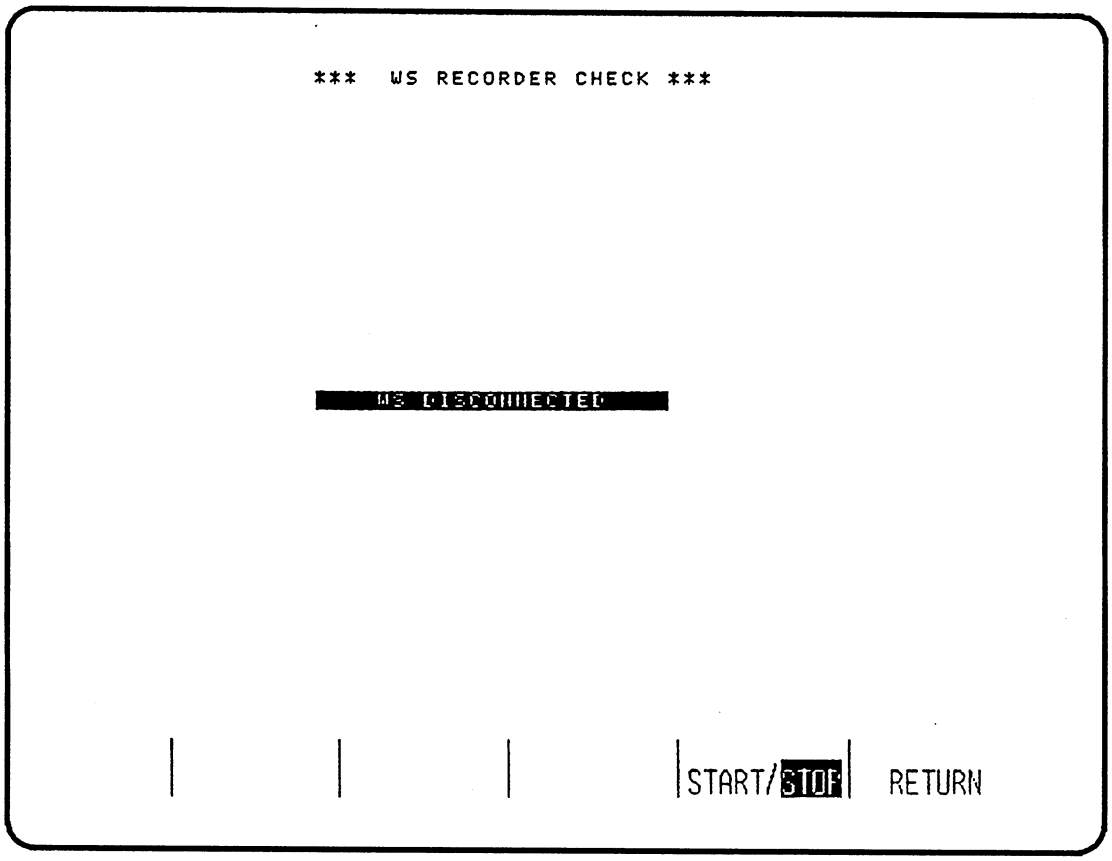
- **GLOBAL MEMORY check (from CPU)**
  The Global memory is accessed from the MPU on the CPU board. The check is the same as the RAM CHECK on the CPU board.



- **CNS COMMUNICATION check**
  The check is executed by transferring a regulated communication test data to a Central Monitor (CNS-8200).
  "CHECKING" message blinks during the checking.



- **WS RECORD check (recorder check)**

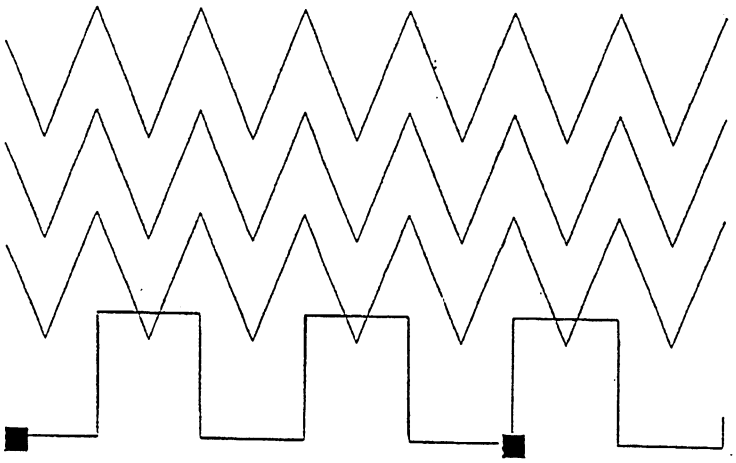


On the above display,

START/STOP: to start to record sawtooth and square waveform on the recording paper or stop recording and printing

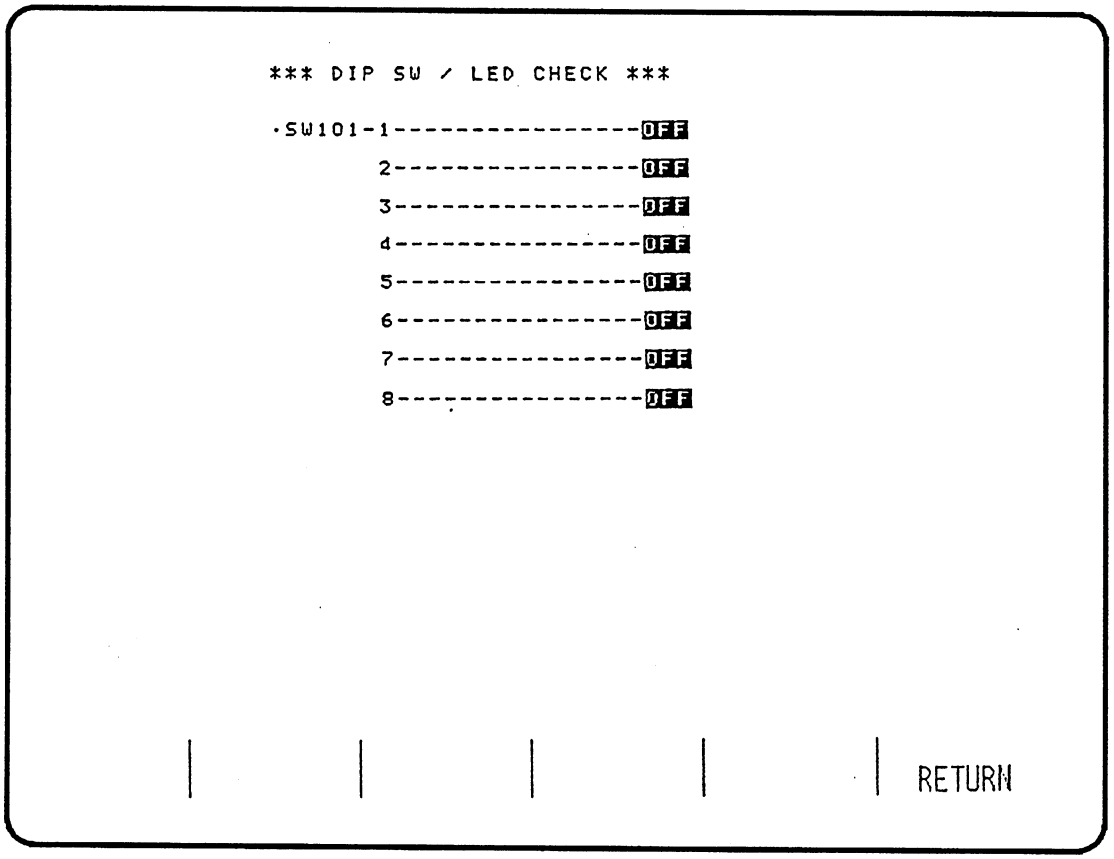
RETURN: to return to the COM BOARD CHECK MENU

Recording example



The following sections are displayed by pressing the "REVIEW" and MANUAL CHECK keys simultaneously on the DIAGNOSTIC CHECK AND SYSTEM SETUP display. These sections are for your reference since these check programs are for product inspection at the factory.

- **DIP SW / LED Check**

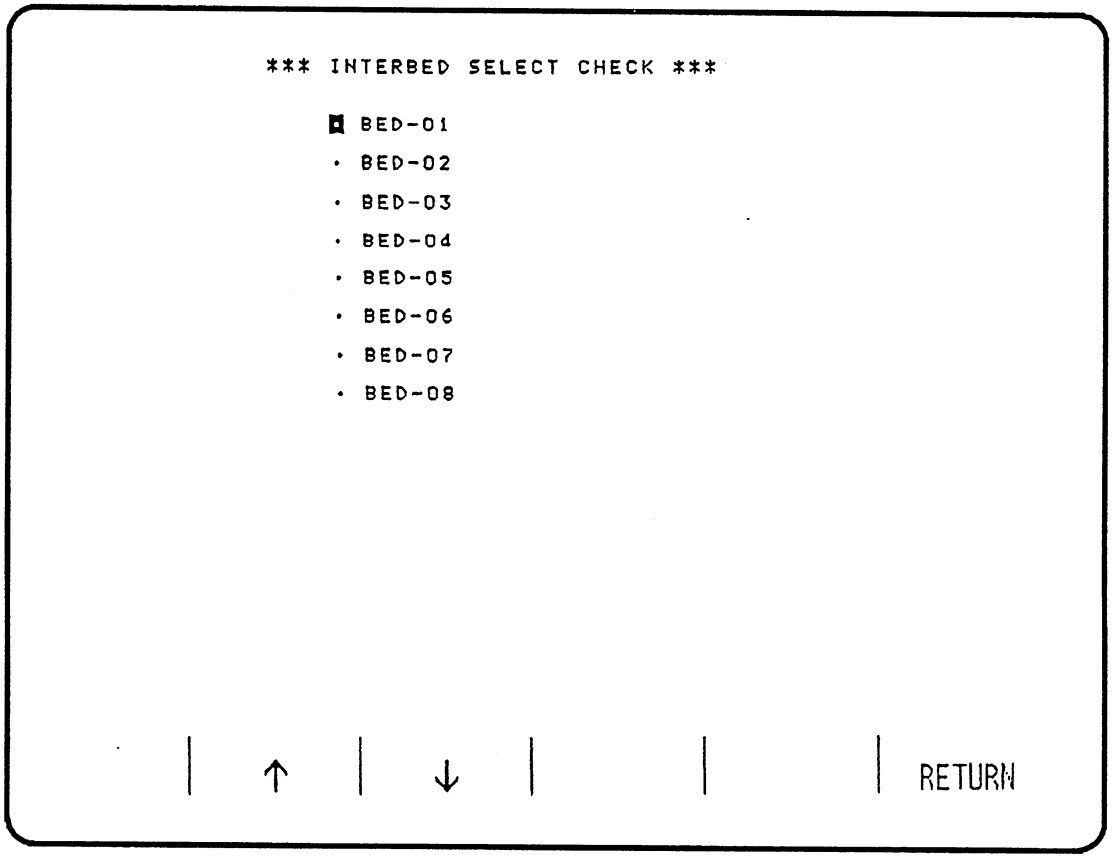


1) DIP SWITCH CHECK
The set condition of the dip switch (SW101) on the COM board appears on the CRT.

2) LED CHECK
Each LED (8bits) on the COM board sequentially lights and goes out one after another.

- **INTERBED SELECT check**

  The signal to select the other Bedside Monitor, "IBSEL", is output by this check.

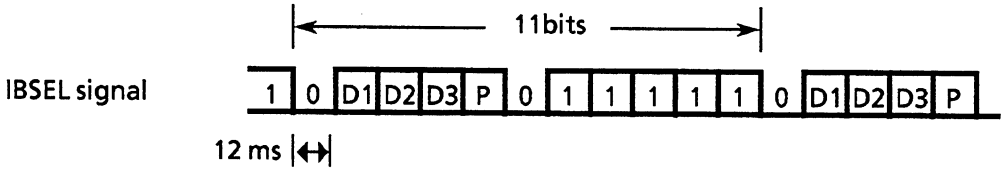


On the above display,

↑ ↓: to select any other bed number

RETURN: to return to the COM BOARD CHECK MENU

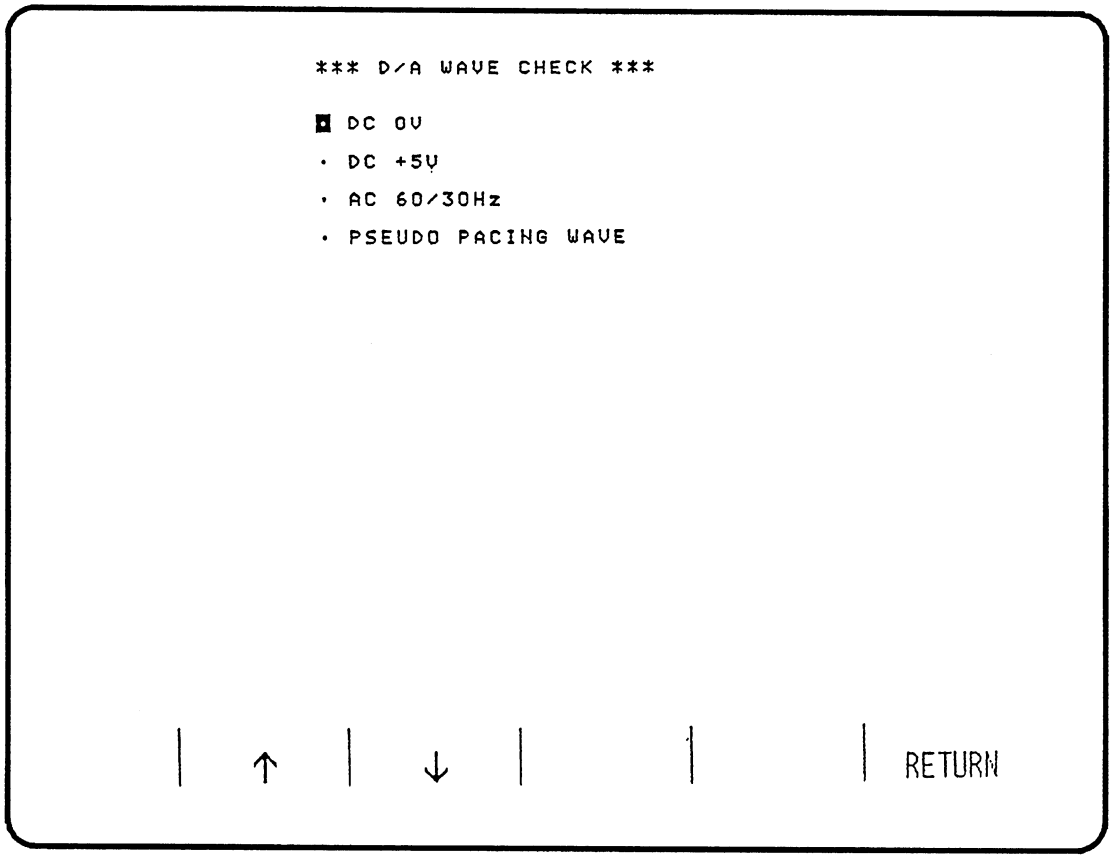
The signal "IBSEL" (serial signal) consists of 11bits of serial format data.



Note: Selection of BED1 to BED8 depends on D1 to D3.

Check pin No.3 of the connector (CN105) to connect with a central monitor on the IO board (UP-0797).

- **D/A WAVE Check**



On the above display,

↑ ↓: to select one waveform from three kinds of waveforms.

RETURN: to return to the COM BOARD CHECK MENU

Check the waveform at the test pin, "DA OUT".

1) DC 0V: 0 V is output at "DA OUT" for the D/A offset check. The offset must be ±10 mV or less.
2) DC+5V: 5 V d.c. is output for noise check. The noise must be ±10 mV or less.
3) AC 30Hz: 10 V p-p. a.c. (30Hz sine wave) is output for frequency characteristic check of delayed ECG ("MDW"). The amplitude of the 30Hz sine wave should be 7.0±0.4 V p-p. at the test pin "DHW".

4-4 Transmitter

When a new battery (more than 1.1 V should be output) is inserted into the transmitter, internal buzzer sounds approx. 1 sec. and operation starts.
When the transmitter is normally functioning, internal buzzer also sounds when "CALL" button is pressed.
If the internal buzzer continuously sounds or does not sound when the battery is inserted, the battery voltage is low or the transmitter is defective.

4-5 Receiver

Refer the self check of main unit.

Section 5 TROUBLESHOOTING

5-1 System Initialization

5-1-1 When Initialization Is Required

Initialize the instrument in the following cases.

- The system is locked-up due to CPU run away or any other reasons.
- The default setting is required.
- ROM is exchanged.
- The board is exchanged.

When the unit is initialized, the data and setting are as follows.

- All patient data is erased.
- The setting contents return to default condition.
- All error history is erased.
- Only data saved is date, time and language settings.

5-1-2 Initialization Procedure

1. Confirm that the power of the main unit is on.

SELF CHECK ◯

2. Continue pressing the SELF CHECK key on the bedside monitor for about 3 sec until the screen disappears. DIAGNOSTIC CHECK AND SYSTEM SETUP screen is displayed.

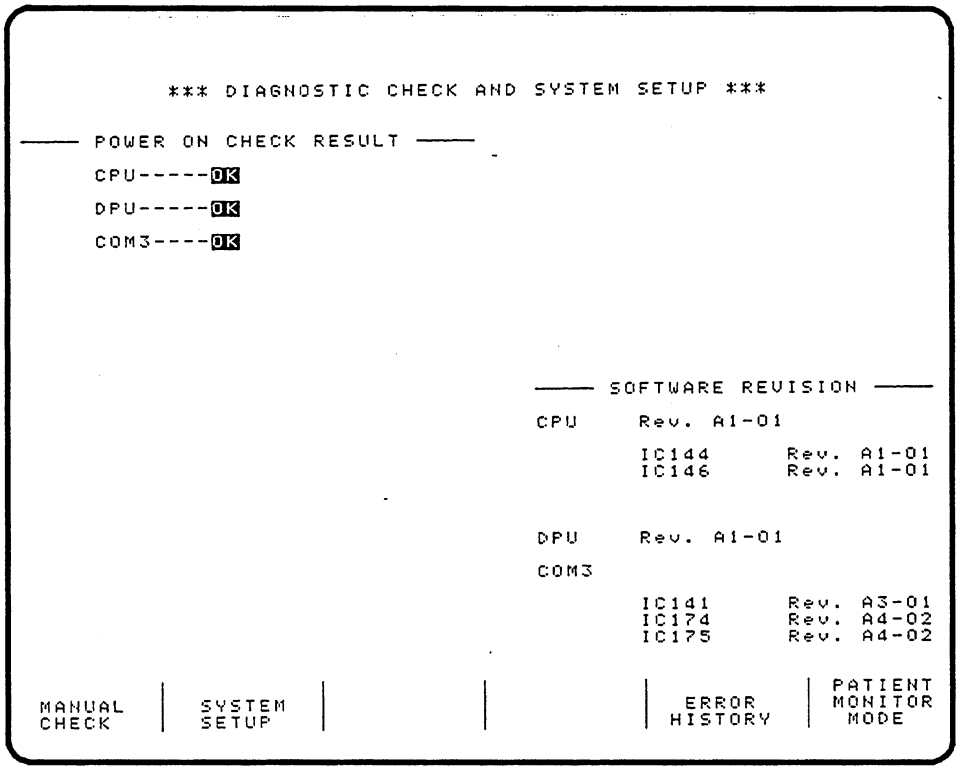
OR

REVIEW

When the main power is off, switching on the main power switch while pressing the SUSPEND key can also call up the DIAGNOSTIC CHECK AND SYSTEM SETUP screen.

3. Press the REVIEW key on the keypad. (The screen does not change.)

4. Press the "PATIENT MONITOR MODE" multi-function key. The following reverse shaded message "SYSTEM INITIALIZE" is displayed for 1sec and disappears. This operation finishes system initialization.



5. Press the "PATIENT MONITOR MODE" multi-function key again to return the screen to the monitoring screen.

5-2 Observed Malfunction Matrix

Before replacing a doubtful Printed Circuit Board (PCB) to a malfunction according to the list, Check the following points as shown in the list.

A: Check patient cable and lead wires. Check electrodes at patient.
B: Check cable connection from patient to Main Unit (MU-881RA/RJ/RK).
C: Check patient cable, lead wires and electrodes.
D: Check to see if LOW mV or NOISE is being displayed on CRT.
E: Check if RESP OFF is selected on RESP SETUP display. Check cable connection from patient to Main Unit.
F: Check external interference and patient cable.
G: Check noise on respiration waveform after adjusting the respiration wave amplitude to be more than 4mm.
H: Check operation of blood pressure transducer.
I: Verify that zero is correct. Check the transducer.
K: Check temperature probe. Check cable connection from patient to Main Unit.
L: Check cable connection from patient to Main Unit. See operator's Manual for correct operation procedures.
M: Verify operation of recorder. Check cable connection from recorder to Main Unit.
N: Check connections between JJ and CNS. Verify that the communication indicator on JJ is lit for the connected CNS.
O: Check connections between JJ and BSM. Verify that the communication indicator on JJ is lit for the connected BSM.
P: Check the connection cable among units, such as the main unit, display unit and keypad
Q: Check whether the correct cables are connected to the input box.
R: Check the battery of the remote control.
S: Check the integrity speaker and its connection cables.
T: Check volume control for synchronizing tone.
U: Check the connections between the main unit and the display unit.
V: Check the main fuse.
W: Verify that the fan is connected.

BSM8800 MALFUNCTION CHECK LIST

MALFUNCTION		ERRONEOUS OPERATION	CPU BD UR-3027 Yellow	DPU BD UP-0670 Green	CRTC BD UP-0795 Red	COM3 BD QI-816P Black	I/O BD UP-0797 White	Power S.U. SC-018R	KEYPAD BD UR-3025	DISPLAY UNIT VD-881R	Input Box JA-880P	HEAD AMP XX-XXX	REMOTE CTRL RY-001P	NOTE
System Error	Constant LEADS OFF	1		3							4CC, 5AA	2DD		A
ECG	No ECG display	1		3							4BB	2DD		B
	Noisy ECG with HUM	1		5							3CC, 4AA	2DD		C
	HR=0 (ECG display OK)	1									3AA	2DD		D
RESP	No Resp. display	1		4							2AA, 5BB	3DD		E
	Artifact on Resp. wave	1		4							2AA	3DD		F
	No Resp. count	1									2AA			G
B.P.	No B.P. wave display	1		3							4BB	2EE		H
	B.P. value not correct	1		3								2EE		I
	Unable to auto-zero	1		3								2EE		H
TEMP	No Temp display			2							3BB	1FF		
	Temp value not correct	1		3								2FF		K
C.O.	C.O. not working	1		3							4BB	2GG		L
WS	No recorder operation	1				2								M
CNS/BSM	No communication with CNS/BSM	1				2	3							N
	No interbed ECG display	1		3		2								O
SWITCH	No key operation on Main Unit		3				2		1					P
	No key operation on Input Box			2							1CC, 3AA			Q
	No key operation on Remote Control		5				4			2LL, 3HH			1	R
SOUND	No sound generated		4		5		1			2HH, 3II				S
	No QRS sync tone	1	4	5			2			3HH, 6II				T
	No alarm sound		3				1			2HH, 4II				
	No LED or sound on Input Box			2							1CC, 3AA			
Display	No CRT display		5		2					1JJ, 3HH, 4KK				U
	Distorted display				2					1JJ, 3HH				
	Wave, character, or graph not normal				1									
POWER	Power lamp does not light	1						2						V
	Fan does not rotate							1						W
	60V fuse blows out							1						
OTHERS	Display changes to Self Check display from normal program display		1					3	2					

Note: AA = JA I/F BD, UP-0270/0271 BB = JA MOTHER BD, UP-0762/0692 CC = JA OPERATION BD, UP-0693/0761 DD = ECG Head Amp, AC-800PA
EE = BP Head Amp, AP-800PA FF = TEMP Head Amp, AM-800PA GG = CO Head Amp, AH-800PA HH = OPERATION CONTROL BD, UP-0801
II = OPERATION (VR) BD, UP-0802 JJ = CRT Unit KK = Display Unit's Power Supply Unit, SC-019R LL = LED BD, UP-0806

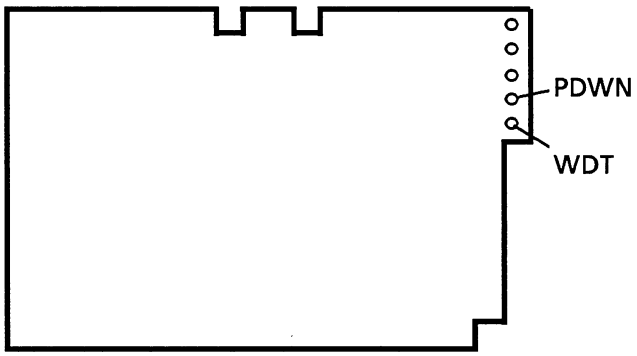
5-3 Error Code Malfunction Matrix

5-3-1 Error Status Indication

1) **Error indication on the CRT:** In an on-line Error, the Error code is indicated on the CRT while the error is registered on the ERROR HISTORY list.

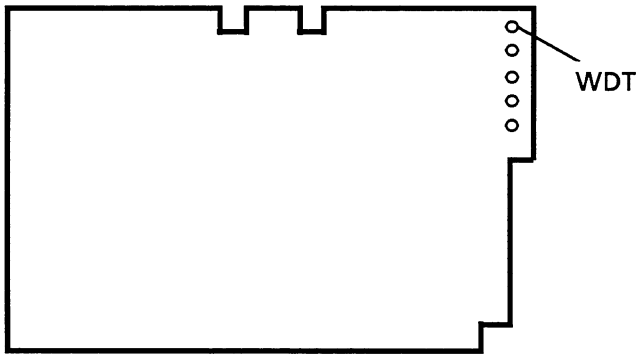
2) **Error indication on each board:** LEDs for WDT or PDWN (Power Down) are located and operate as follows.

◆ **CPU board, UR-3027**



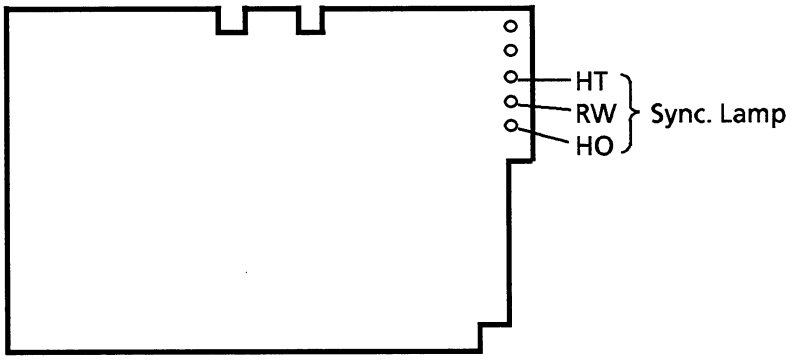
Status	WDT LED	PDWN LED
Normal	ON	ON
MPU Runaway/Stop	OFF	ON
Power down	OFF	OFF

◆**COM3 board, UP-0563 (QI-816P)**



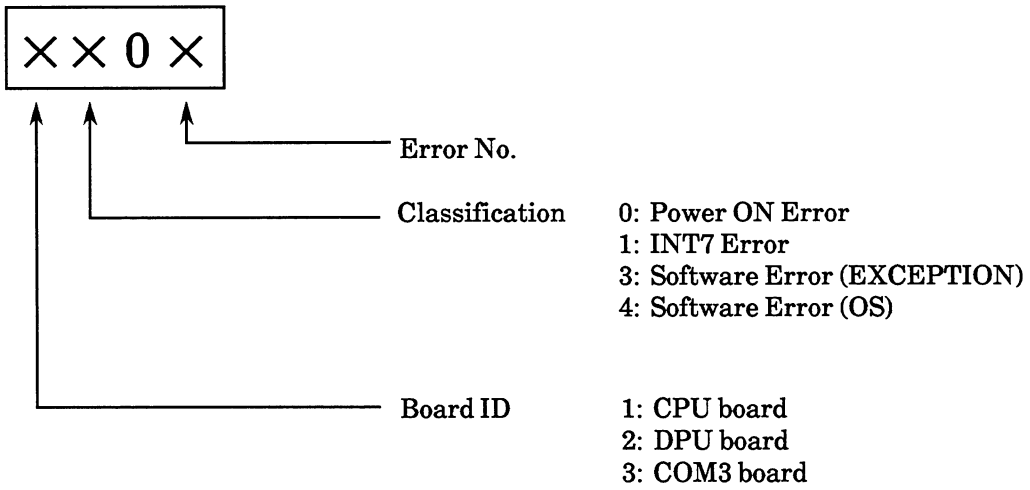
Status	WDT LED
Normal	ON
MPU Runaway/Stop	OFF

◆**DPU board, UP-0670**



5-3-2 Error Code

The error code is registered with a 4-digit hexadecimal number in ERROR HISTORY according to the following list if an error is found.



NOTE

In case of software error, check CPU board for poor contact between ROM and ROM socket, connectors, or replace CPU board.

BSM8800 ERROR CODE LIST

ERROR CODE	CPU Board UR-3027 Yellow	DPU Board UP-0670 Green	CRTC Board UP-0795 Red	COM3 Board QI-816P Black	I/O Board UP-0797 White	Power Trans-former Unit SC-018R	KEYPAD RY-881P	DISPLAY UNIT VD-881R	Input Box JA-880P	HEAD AMP XX-XXX
POWER ON ERROR										
1001	1									
1002	1									
1004	1									
1005	1									
1006	2				1					
1009	1									
100A	3	1		2						
100B	2	1								
100D	2			1						
2001		1								
2002		1								
2006		1								
200A		1								
200E		1								
3001				1						
3002				1						
3004				1						
3006				1						
300A				1						

◆Error Code List by Board

● CPU Board

	Error code	Suspect area
Power on error	1 0 0 1	ROM
	1 0 0 2	RAM
	1 0 0 4	71051
	1 0 0 5	8279
	1 0 0 6	72001
	1 0 0 9	E^2PROM
	1 0 0 A	Global Memory (DPU, COM3)
	1 0 0 B	Communication (CPU-DPU)
	1 0 0 D	Communication (CPU-COM3)

● DPU Board

	Error code	Suspect area
Power on error	2 0 0 1	ROM
	2 0 0 2	RAM
	2 0 0 6	Timing Port
	2 0 0 A	Global Memory
	2 0 0 E	A/D-D/A

● COM3 Board

	Error code	Suspect area
Power on error	3 0 0 1	ROM (on COM3)
	3 0 0 2	RAM (on COM3)
	3 0 0 4	8251
	3 0 0 6	RTC
	3 0 0 A	Global Memory

5-4 Troubleshooting For Telemetry System

In telemetry system, the most frequent trouble is no communication between transmitters and receivers, i. e., telemetry signals cannot be received. Referring signal flow, do troubleshooting.

NOTE

Transmitter and receiver can not be adjusted locally. See Section 6 for details.

5-4-1 The Most Typical Trouble Sources

Transmitter side

1. Defect of analog circuit
2. Defect of coding/modulation system

Between transmitter and receiver

3. Defect from antenna of transmitter to antenna of receiver

Receiver side

4. Wiring trouble from antenna to splitter
5. Defect of splitter (ZA-003P)
6. Wiring trouble from splitter to receiver
7. Defect of receiver
8. Defect of DPU which controls the receiver
9. Wiring trouble for DPU board

5-4-2 The Most Typical Symptom Actually Happened

1. All waves cannot be received.
2. Telemetry signal can be received. However, waveform and/or status information is abnormal.
   Examples: a) Noise is superimposed on the wave.
   b) The shape of the wave is abnormal.
   c) NURSE CALL is displayed in spite of that CALL button is not pressed on the transmitter.

5-4-3 Troubleshooting for 2 Cases in Section 5-4-2

Since the troubleshooting procedures differ for 2 cases, they are explained separately as follows:

1. All waves cannot be received.
   There are several points to be checked as follows;
   (A) Defect of antenna system
      a) Poor installation of antenna system(Ex., Cut down of antenna cables)
      b) Wiring trouble between the main unit and the distributor of antenna system.
      c) Defect of distributor of antenna system
         In this case, when the transmitter is closely placed to the main unit, telemetry signal can be received.
      d) Power supply trouble to distributor of antenna system
   (B) Defect of main unit
      a) Defect of DPU board
      b) Power supply trouble to receiver

2. Telemetry signal can be received. However, waveform and/or status information is abnormal.
   Examples: a) Noise is superimposed on the wave.
   b) The shape of the wave is abnormal.
   c) NURSE CALL is displayed in spite of that CALL button is not pressed on the transmitter.

   Exchanging frequencies of receivers between the troubled one and normal one, check operation for both channels.
   If the symptom is transferred to the other channel, the probable trouble source is the transmitter.
   If the symptom still remains, the probable trouble source is DPU board.

Section 6 ADJUSTMENT

6-1 Main Unit

UP-0278 extension board is required in the adjustment of the Main Unit.

6-1-1 Regulator Board, UP-0813

◆ **+5 V Adjustment (VR101)**

Adjust the VR101 to set 5.10 ±0.01 V between test pin +5 V and E2 without a load.

◆ **Ampere Adjustment (VR102) : for operation of over current protection**

Connect a load and a voltmeter in parallel between +5 V and E2 and connect an ammeter in series with the load.

Adjust the VR102 for protecting the 5 V Switching Regulator Circuit against excessive current so that the 5 V starts to drop down at test pin +5 V when the load current becomes 9 A.

6-1-2 DPU Board, UP-0670

◆ **REF2.5 Adjustment (VR101)**

Adjust the VR101 to set 2.500 V between test pin REF2.5 and AGND (E1).

◆ **D/A and A/D Converter Adjustment (VR102 - VR105)**

Call up A/D-D/A CHECK display on the CRT in the Manual Self Check program (refer to page 4.52 of this service manual).

(1) D/A OFFSET-1 (VR105)
   a) Select the check item No.1 (SELECT①) on the CRT.
   b) Press the START/STOP key to load the program.
   c) Adjust the VR105 to set 0.000 V at test pin DA.

(2) A/D GAIN-1 (VR103)
   a) Select SELECT② on the CRT.
   b) Press the START/STOP key to load the program.
   c) Adjust the VR103 to set 7D0H at A/D ADJ. GAIN on A/D-D/A ADJUST table.

(3) A/D OFFSET (VR102), A/D GAIN-2 (VR103)
   a) Adjust the VR102 to set 800H at A/D ADJ. 0V on the table.
   b) Repeat the adjustment procedure of (2)-c) or adjust the VR103 to set 7DOH on the table.
   c) Adjust VR102 again with the same procedure of a). After these adjustments, do no rotate VR102 and VR103.

(4) D/A GAIN (VR104), D/A OFF SET (VR105)
   a) Adjust the VR104 to set 7D0H at D/A ADJ. GAIN on the table.
   b) Adjust the VR105 to set 800H at D/A ADJ. 0V on the table.
   c) Adjust VR104 again with the same procedure of a).

(5) D/A-A/D LOOP
   a) Select SELECT③.
   b) Press the START/STOP key to load the program.
   c) Confirm that the OK mark is indicated next to the D/A-A/D LOOP CHECK title.

6-1-3 CRTC Board, UP-0795

◆ DCLK Adjustment (VC601)

Adjust the VC601 until there is no display distortion on the GRAPHIC DISPLAY CHECK SCREEN, and also WAVE DISPLAY CHECK screen.

6-1-4 CPU Board, UR-3027

◆ Real Time Clock Adjustment (VC101)

Adjust the VC101 so that a 1 Hz clock ±0.000011 is acquired between test pin TP10 and E2.

6-1-5 COM3 Board, UP-0563 (QI-816P)

◆ REV2.5 Adjustment (VR104)

Adjust the VR104 to set 2.5000 V between TP REF2.5 and AGND.

◆ D/A, A/D Converter Adjustment (VR-101 to VR-103)

Call up D/A WAVE CHECK display on the CRT in the Manual Self Check program (refer to page 4.51 of this service manual).

(1) D/A OFFSET-1 (VR-102)
Adjust the VR102 so that DC 0 V display on the screen indicates 0 V and the voltage at the test point DA OUT is 0 V ±10 mV.

(2) D/A GAIN-1 (VR-103)
Adjust the VR103 so that DC +5 V display on the screen indicates +5 V and the voltage at the test point DA OUT is 5 V ±10 mV.

(3) D/A OFFSET-2 (VR101)
Adjust the VR101 so that DC 0 V display on the screen indicates 0 V and the voltage at the test point MDW is 0 V ±100 mV.

6-1-6 I/O Board, UP-0797

◆ AUX 1 Offset (VR101)

Short pin No. 1 and 3 of the connector CN103. Adjust VR101 so that the voltage at test pin TPAUX1 is less than ±2 mV.

◆ AUX 2 Offset (VR103)

Short pin No. 2 and 3 of the connector CN103. Adjust VR103 so that the voltage at test pin TPAUX2 is less than ±2 mV.

◆ AUX 1 Gain (VR102)

Short test pin ±5 V and the individual input pins of connector CN103. Adjust VR102 so that the voltage at test pin TPGAIN1 is ±5.000 ±0.002 V.

◆ AUX 2 Gain (VR104)

Short test pin ±5 V and the individual input pins of connector CN103. Adjust VR104 so that the voltage at test pin TPGAIN2 is ±5.000 ±0.002 V.

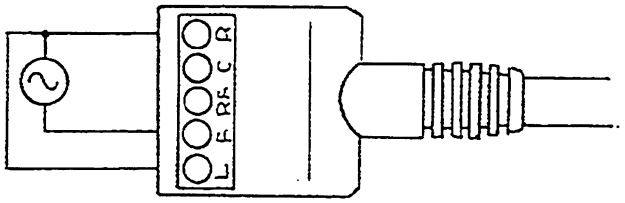
6-2 Head Amplifier

YS-008P3 extension board is required in the adjustment of the head amplifier.

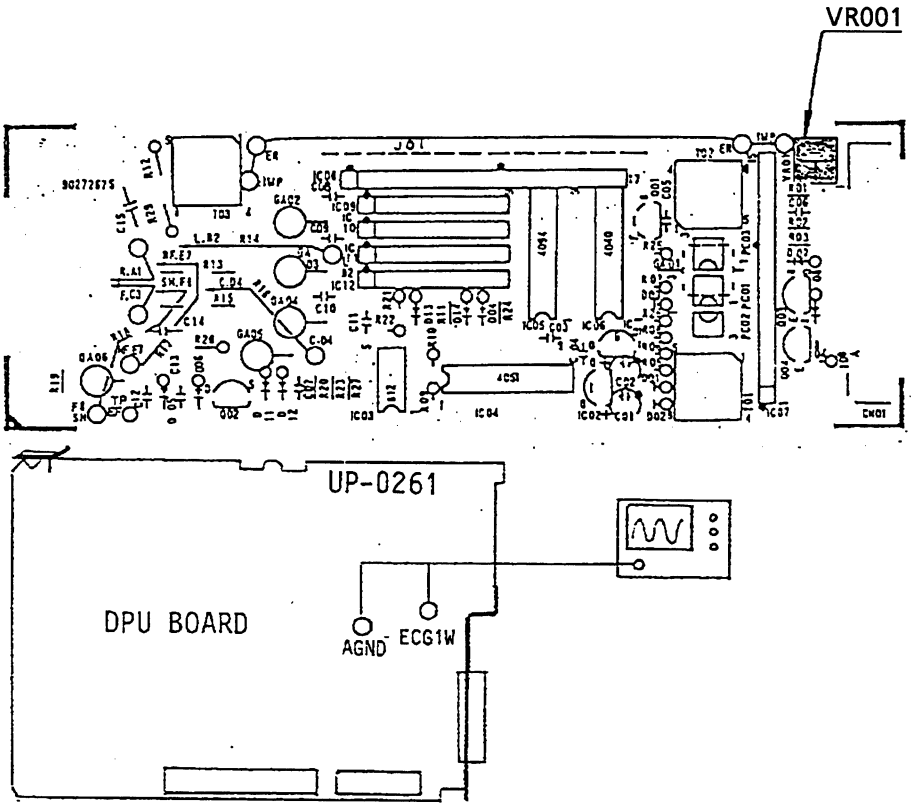
6-2-1 ECG Head Amp Board, UP-0272

◆ **ECG Gain Adjustment (VR001)**

1) Select Lead–Ⅱ of 3–electrode leads on the SETUP display.
2) Apply a 10 Hz sine wave (6 mVp-p) between R(RA) and F(LL) with an oscillator.



3) Adjust the VR001 on the board for 6±0.3 Vp-p between test pin ECG1 W and AGND on the DPU board (UP-0670) with an oscilloscope.



◆ECG Gain Simplified Adjustment (VR001)

1) Apply normal QRS (Mode: WAVE-1) to the ECG input connector with the vital signs simulator, AX-800P.
2) Press the ECG LEAD key to select Lead-Ⅱ
3) Adjust the VR001 for a 1.5 V amplitude of the R-wave at the ECG OUT connector on the front panel with an oscilloscope.

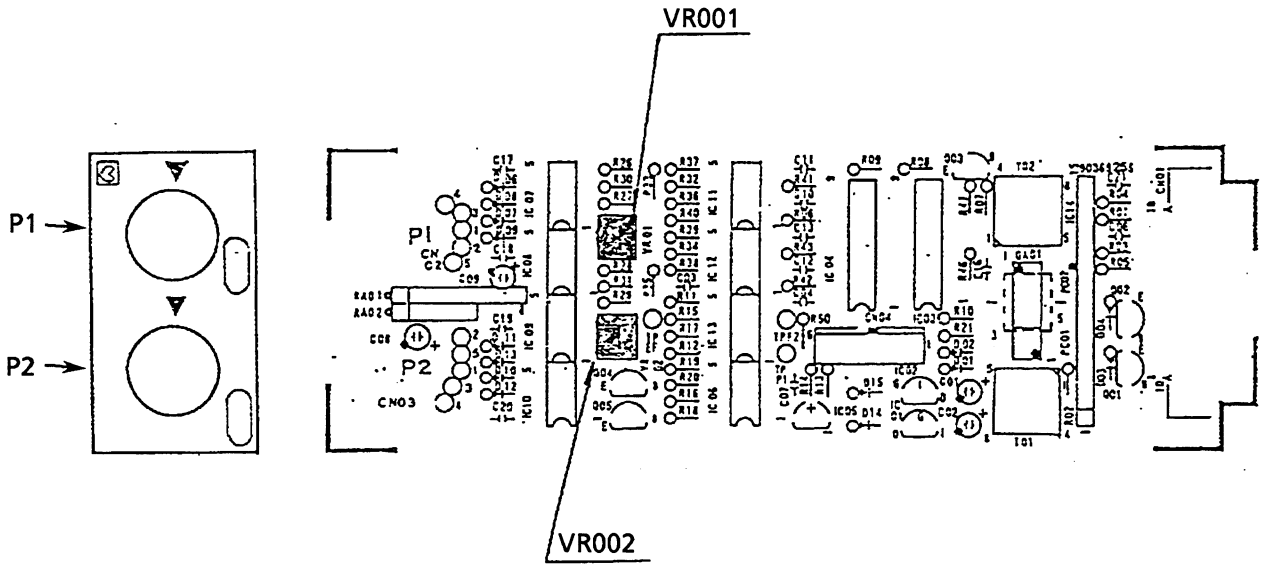
6-2-2 Blood Pressure Head Amp Board (AP-851PA), UP-0369

◆ Blood Pressure Channel-1 (P1) Adjustment (VR001)

1) Connect the P1 output of the AX-800P to the P1 input connector on the head amplifier (AP-800PA).
2) Apply 0 mmHg (Mode: 2) to the P1 input connector with the AX-800P.
3) Zero a P1 value on a blood pressure waveform display by pressing the BP1 ZERO key on the operation panel of the input box.
4) Applying 200 mmHg (Mode: 4) to the P1 input connector with the AX-800P.
5) Adjust the VR001 to indicate 200 mmHg (P1 value) on the B.P. Display.

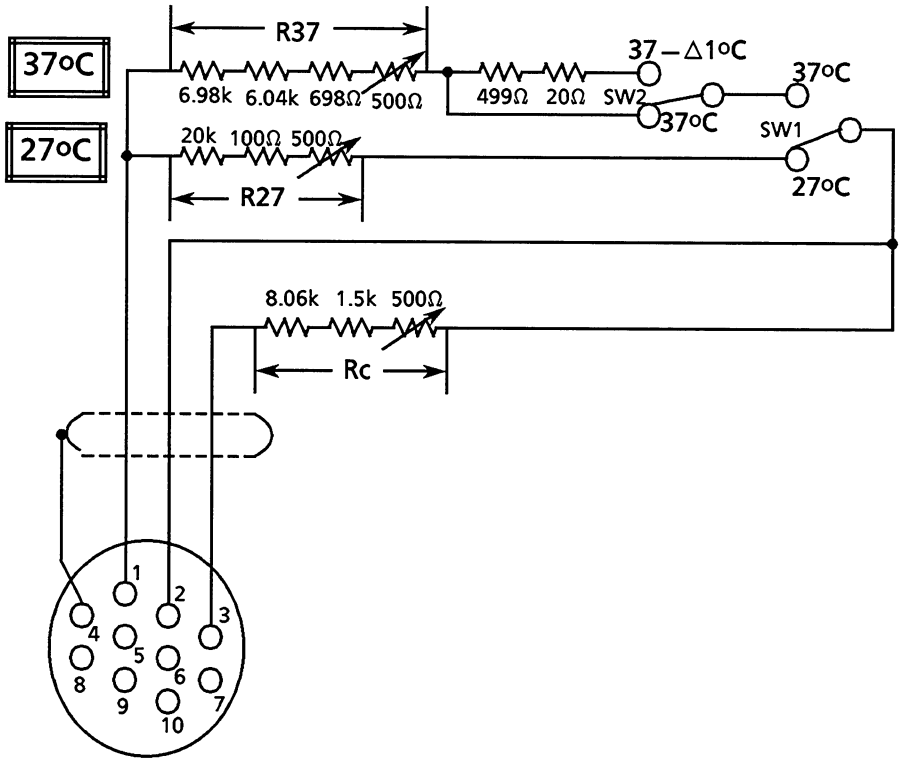
◆ Blood Pressure Channel-2 (P2) Adjustment (VR002)

1) Connect the P1 output of the AX-800P to the P2 input connector.
2) Apply 0 mmHg (Mode: 2) to the P2 input connector with the AX-800P.
3) Zero the P2 value on the B.P. Display by pressing the BP2 ZERO key.
4) Apply 200 mmHg (Mode: 4) to the P2 input connector.
5) Adjust the VR002 to indicate 200 mmHg (P2 value) on the B.P. Display.



6-2-3 CO Head Amp Board, UP-0318

The CO Head Amp board should be adjusted with not only the Vital Signs Simulator (AX-800P) but also the following special CO Input Jig.



NOTE

All the above resistors are F-type resistors.

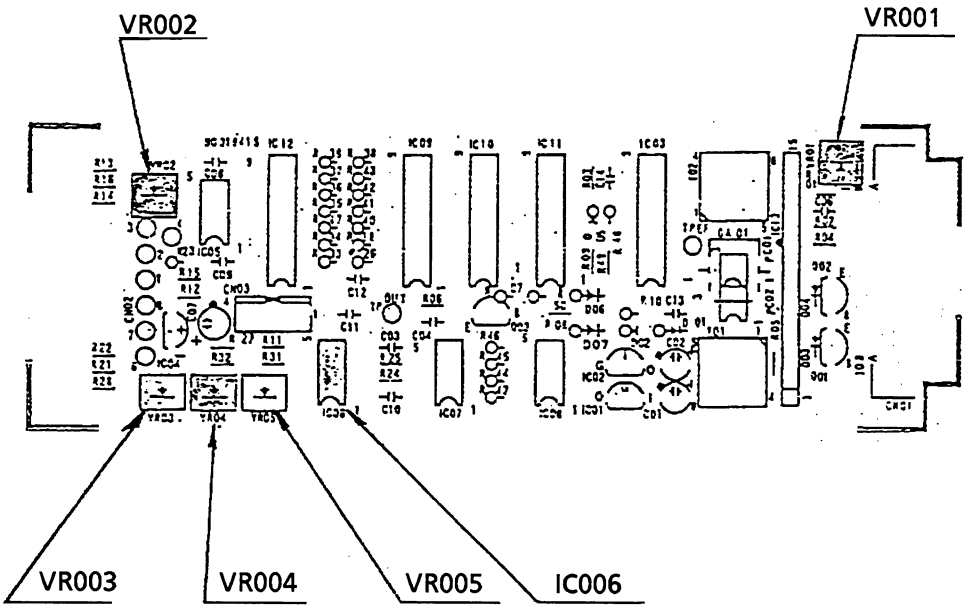
◆ **CO input Jig Adjustment**

Adjust each variable resistor (500 Ω) of R27, R37 and Rc to be the following values with a digital voltmeter (Valid digits: 4 and 1/2 or more).

R27: 20.359 kΩ ± 5 Ω

R37: 13.999 kΩ ± 5 Ω

Rc: 9.755 kΩ ± 5 Ω



◆ **Tb Adjustment (VR003/001)**

1) Put a CO Head Amplifier (AH-800PA) into the slot farthest from the JAInterface unit (QI-802P) of the input box.
2) Call up the DEBUG PROGRAMdisplay by pressing the DISPLAY key and ALARM LIMIT key on the Main Unit simultaneously.
3) Select Item-7, A/D TEST PROGRAM, on the display.
4) Apply 27° C to the CO input connector on AH-800PA with the CO Input Jig.
5) Adjust the VR003 to indicate 800±1(H) at the crossing point of CH#8 and TS6 on the A/D TEST PROGRAM display.

[A/D TEST PROGRAM DISPLAY]

AD TEST	TS1	TS2	TS3	TS4	TS5	TS6	TS7	TS8
CH#1								
CH#8						800 801		
CH#12								

6) Apply 37° C to the CO input connector on AH-800PA with the CO Input Jig.
7) Adjust the VR001 to indicate B20±1(H) at the crossing point of CH#8 and TS6 on the display.

◆ **Ti Adjustment (VR002/004)**

NOTE

Execute Ti Adjustment only after finishing Tb Adjustment.

1) Apply 0° C(Mode: 1) to the CO input connector with the AX-800P.
2) Call up the A/D TEST PROGRAM display.
3) Adjust the VR002 to indicate 800±1(H) at the crossing point of CH#8 and TS4 on the display.

[A/D TEST PROGRAM DISPLAY]

AD TEST	TS1	TS2	TS3	TS4	TS5	TS6	TS7	TS8
CH#1								
CH#8				800 800				
CH#12								

4) Apply 20° C(Mode: 3) to the CO input connector with the AX-800P.
5) Adjust the VR004 to indicate B20±1(H) at the crossing point of CH#8 and TS4 on the display.

[A/D TEST PROGRAM DISPLAY]

AD TEST	TS1	TS2	TS3	TS4	TS5	TS6	TS7	TS8
CH#1								
CH#8				B20 B20				
CH#12								

◆ ΔT Adjustment

NOTE

Execute ΔT Adjustment only after finishing Tb and Ti Adjustment.

1) Execute CO START on the CO MEASURE screen after applying 37° C to the CO input connector with the CO Input Jig.
2) Measure the voltage at Pin-6 and Pin-7 on IC006B.
   The voltage at Pin-6: $E_{37⑥}$
   The voltage at Pin-7: $E_{37⑦}$
3) Measure the voltage at Pin-6 and Pin-7 on IC006B after setting the switch (SW2) on the CO Input Jig to 37 – Δ1°C.
   The voltage at Pin-6: $E_{Δ1⑥}$
   The voltage at Pin-7: $E_{Δ1⑦}$
4) Adjust the VR005 for the following equation.
   $E_{37⑦} - E_{Δ1⑦} = -10\ X\ (E_{37⑥} - E_{Δ1⑥})$

Reference

Output voltages to Tb and Ti of the calibrated AH-800PA are shown as follows:

Tb Temperature(°C)	Tb Output Voltage
22	−0.955 V
37	+2.000 V
45	+3.612 V

Ti Temperature(°C)	Ti Output Voltage
0	0 V
10	+0.995V
20	+2.012 V

Relation between Tb and Thermistor Resistance in catheter (Rb) is shown as follows:

Tb	Rb(Ω)	Tb	Rb(Ω)	Tb	Rb(Ω)	Tb	Rb(Ω)	Tb	Rb(Ω)	Tb	Rb(Ω)
15	32871	21	25760	26	21161	31	17481	36	14519	41	12123
16	31544	22	24755	27	20359	32	16837	37	13999	42	11700
17	30277	23	23795	28	19591	33	16220	38	13500	43	11294
18	29068	24	22877	29	18857	34	15629	39	13022	44	10905
19	27914	25	22000	30	18154	35	15062	40	12563	45	10531
20	26813										

Relation between Ti and Thermistor Resistance in Injection Temperature Probe (Ri) is shown as follows:

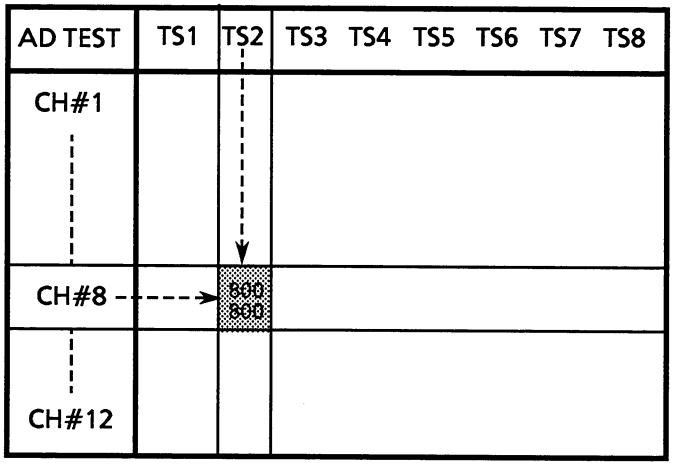
Ti	Ri(kΩ)	Ti	Ri(kΩ)	Ti	Ri(kΩ)	Ti	Ri(kΩ)
0	257.58	7	187.04	14	137.59	21	102.48
1	245.87	8	178.87	15	131.83	22	98.349
2	234.75	9	171.11	16	126.33	23	94.408
3	224.20	10	163.73	17	121.09	24	90.648
4	214.18	11	156.70	18	116.10	25	87.057
5	204.67	12	150.02	19	111.34	26	83.628
6	195.63	13	143.65	20	106.10	27	80.352

6-2-4 Temp Head Amp Board, UP-0319

◆ REF0 Adjustment (VR002)

1) Put a Temperature Head Amplifier (AW-800PA) into the slot farthest from the QI-802P/815P.
2) Call up A/D TEST PROGRAM display. Refer to the section 6-2-3 Tb Adjustment.
3) Adjust the VR002 to indicate 800±1(H) at the crossing point of CH#8 and TS2.

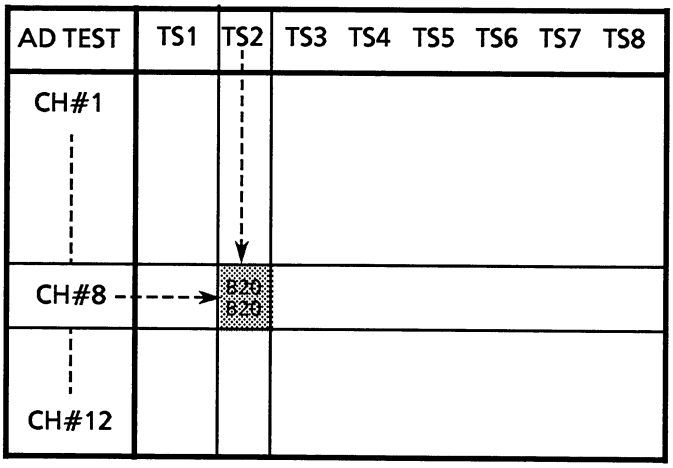
[A/D TEST PROGRAM DISPLAY]



◆ CAL37 Adjustment (VR001)

Adjust the VR001 to indicate B20±1(H) at the crossing point of CH#8 and TS2.

[A/D TEST PROGRAM DISPLAY]



◆ T1, T2 Verification

Verify that Errors of T1 value or T2 value are within ±0.1° C on a normal operating display when 22, 37, or 45° C signal is applied to the input connectors (T1 or T2) on the AW-800PA.

Reference

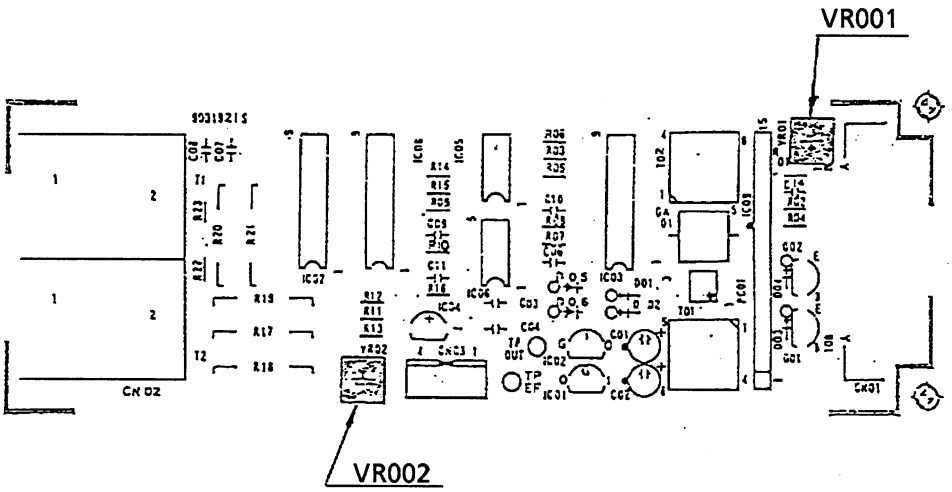
Output voltages to T1 or T2 of the calibrated AW-800PA are shown as follows:

Temperature (T1 or T2)	Output Voltage (T1 or T2)
22 °C	−0.950 V
37 °C	+2.000 V
45 °C	+3.590 V

The relation between temperature (T) and thermistor resistance (Rt) in Temperature Probe (YSI-400) is shown as follows:

T	Rt	T	Rt	T	Rt	T	Rt	T	Rt
0	7355	10	4483	20	2814	30	1815	40	1200
1	6990	11	4273	21	2690	31	1740	41	1153
2	6645	12	4075	22	2572	32	1668	42	1108
3	6319	13	3887	23	2460	33	1599	43	1065
4	6011	14	3708	24	2354	34	1534	44	1024
5	5720	15	3539	25	2253	35	1471	45	984.2
6	5444	16	3379	26	2156	36	1412		
7	5184	17	3226	27	2065	37	1355		
8	4937	18	3082	28	1977	38	1301		
9	4704	19	2944	29	1894	39	1249		

NOTE
T (°C)
Rt (Ω)



6-2-5 Thermister Resp Head Amp Board, UP-0548

NOTE

When IC005 or VR001 is replaced, offset adjustment (VR001) is required.

◆ Offset Adjustment(VR001)

1) Connect the respiration pickup to the respiration head amplifier.
2) Measure voltage with a digital voltmeter across the pin-29 (CH7W/RW) and pin-33 (GND) of the CNS connector(or WS connector) on the rear of the MU-802R bedside monitor main unit.
3) Adjust the VR001 so that the voltmeter reads DC ±10 mV.

6-2-6 CO_2 Head Amp Board, UP-0588

NOTE

When the D/A convertor IC002 is replaced, the D/A Converter Reference Adjustment (VR001) is required.

◆D/A Converter Reference Adjustment(VR001)

1) Read DC voltage across the TP E1(analog ground) and IC008 pin-8 with a digital voltmeter.
2) Disconnect the CO2 sensor and adjust the VR001 so that the voltmeter reads −4.8 V ± 0.01 V.

6-2-7 O_2 Head Amp Board, UP-0592

NOTE

When the IC009 or IC010 is replaced, this offset adjustment (VR001 and VR002) is required.

◆ **Offset Adjustment(VR001, VR002)**

1) Insert the O_2 head amplifier into the last slot of the input box.
2) Call up the A/D Test Screen of the bedside monitor main unit.
3) Shorten the input connector pins 2, 3, and 5 to the pins 1 and 4 (EF: floating ground) and adjust each volume so that Test pins TS6 and TS8 becomes within ±10mV of REFO.

Reference

TS2 value and TS4 value of #5 (O_2) lines in the table indicate REF0V voltage. TS6 value indicates the offset voltage of IC009. TS8 indicates the offset voltage of IC010.

Unit of the value is mV and upper numerals show maximum value and lower numerals show minimum value in one second.

AD TEST	TS1	TS2	TS3	TS4	TS5	TS6	TS7	TS8
CH#1 (ECG1) CH#2 (ECG2) CH#3 (RESP)	..... 	5117 5117 -10 2 0 7	..... 	5117 5117 -10 2 -2 7	..... 	5117 5117 -10 5 0 10	..... 	5117 5117 -10 5 -2 7
CH#4 ( )	.....	5 12	.....	5 12	.....	7 12	.....	-15 -10
CH#5 (02)	.....	-4870 -4865	.....	-4870 -4865	.....	-4875 -4870	.....	-4872 -4865
CH#6 ( )	.....	2 10	.....	2 7	.....	2 10	.....	2 10
CH#7 ( ) CH#8 ( ) CH#9 ( )	5 12 5 10 -17 -10	5 10 5 10 17 22	2 10 7 10 -12 -5	5 10 5 10 17 22	5 12 5 12 10 15	2 7 5 10 5 10	7 12 5 12 8 12	5 12 2 10 5 10
CH#10 ( ) CH#11(PARA)	2 7 97 102	2 7 5020 5025	2 10 457 462	2 7 5020 2025	5 10 5017 5022	2 7 5020 5025	5 10 5017 5022	2 10 5020 5025
CH#11( )	0 2	-5030 -5027	-2515 -2512	2 2	2512 2515	5027 5030	5020 5022	2 2
HEAD AMP INSTALLED	ECG	.....	O_2	.....	.....	.....	.....	.....

6-2-8 NIBP Head Amp Sub Board (AP-860PA), UP-0630

NOTE

This adjustment is for the NIBP Head Amplifier AP-860PA only.

◆ **Pressure Zero Adjustment(VR201)**

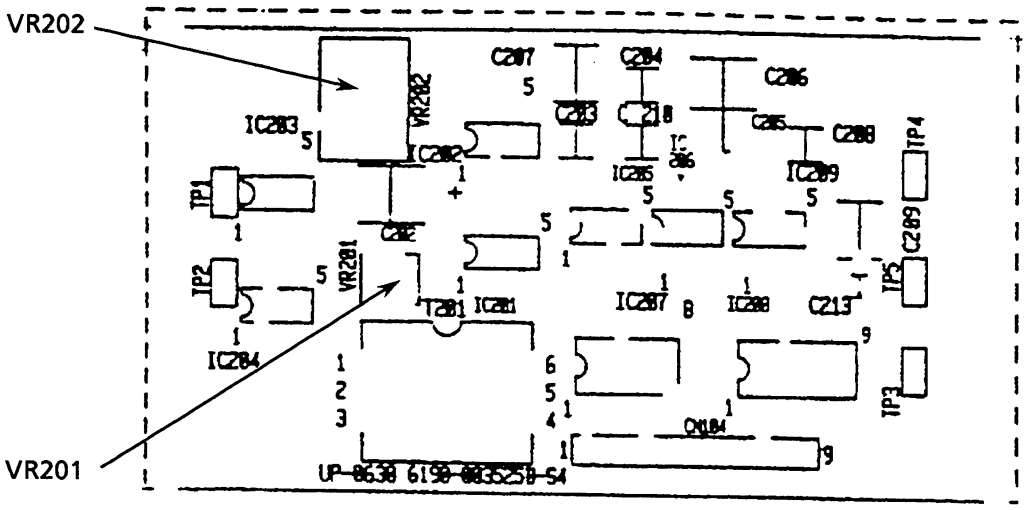
1) Disconnect the double air hose from the NIBP connectors on the NIBP head amplifier.
2) Adjust the VR201 to set 0 V ±10 mV between test pin TP5 and AGND.

◆ **Pressure Gain Adjustment(VR202)**

1) Call up NIBP AMP CHECK (AP-860P) display on the CRT in the Manual Self Check program (refer to page 4.47 of this service manual).
2) Select the check item No. 1, CALIBRATION (1), or No. 2, CALIBRATION (2).
3) Connect the external pump and manometer to the two NIBP connectors on the NIBP head amplifier.
4) Increase the pressure until the reading on the manometer reads 300 mmHg.
5) Adjust the VR202 to set the pressure reading on the NIBP AMP CHECK (AP-860P) display to read 300 mmHg ±1 mmHg.

NOTE

The bedside monitor automatically carries out the zero calibration every time the NIBP AMP CHECK (AP-860P) display is called up. Therefore, exit the NIBP AMP CHECK (AP-860P) display and call up the NIBP AMP CHECK (AP-860P) again every time the NIBP head amplifier is replaced during this check mode.



6-3 Display Unit (Internal), VD-881R

6-3-1 Power Supply Unit Board, SC-019R

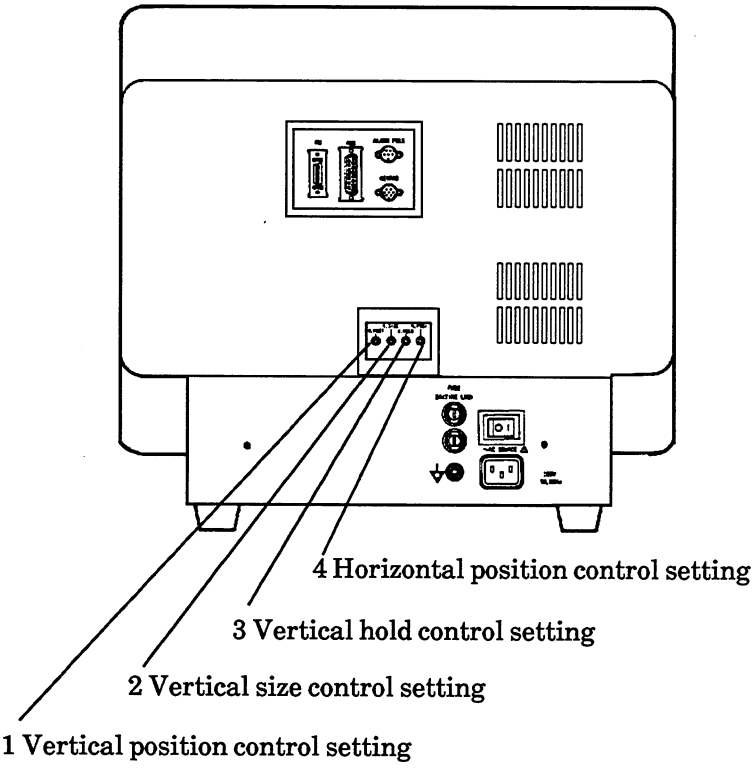
◆ **+ 5V Adjustment (VR101)**

Adjust the VR101 to set 5.10 V ±0.01 V between the test pin +5 V and E2 without a load.

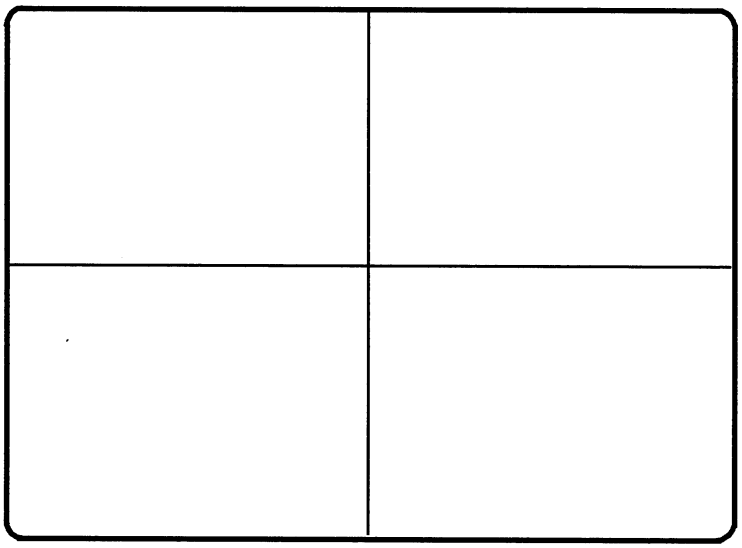
6-4 Display Unit (External), VD-881R

6-4-1 Display Unit's Rear Panel Adjustment Knob

Rear Panel



Call up the following screen of the GRAPHIC DISPLAY CHECK screen in the CRTC CHECK mode.



1 VERTICAL. POSITION

Adjust the V.POSI KNOB so that the left and right margins on the CRTC CHECK screen shown on the previous page are equal.

2 Vertical Size

This is to adjust the gain along the Y–axis. Adjust the V.SIZE knob so that the image on the screen is the same as the CRTC CHECK screen shown on the previous page.

3 Vertical Hold

If the image on the screen continuosly sweeps along the Y–axis, adjust the V. HOLD knob until the CRTC CHECK screen shown on the previous page appears stationary.

4 Horizontal Position

Adjust the H. POSI knob so that the upper and bottom margins on the CRTC CHECK screen shown on the previous page are equal.

6-5 Receiver Unit, ZR-800P

Do not perform the adjustment locally. The reason is as follows;

For the adjustment of this block, a personal computer, the related special software, shield room, high-frequency spectrum analyzer etc. are essential and it is out of level of the field service.
NIHON KOHDEN does not provide above device and information.
If the adjustment should perform locally without above facility, the specification can not be guaranteed.

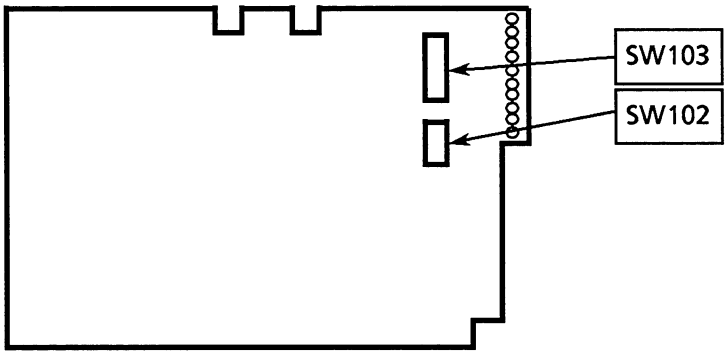
6-6 Transmitter

The same situation as above.

Section 7 INTERNAL SWITCH AND JUMPER SETTING

7-1 Main Unit, MU-881R

7-1-1 CPU Board, UR-3027



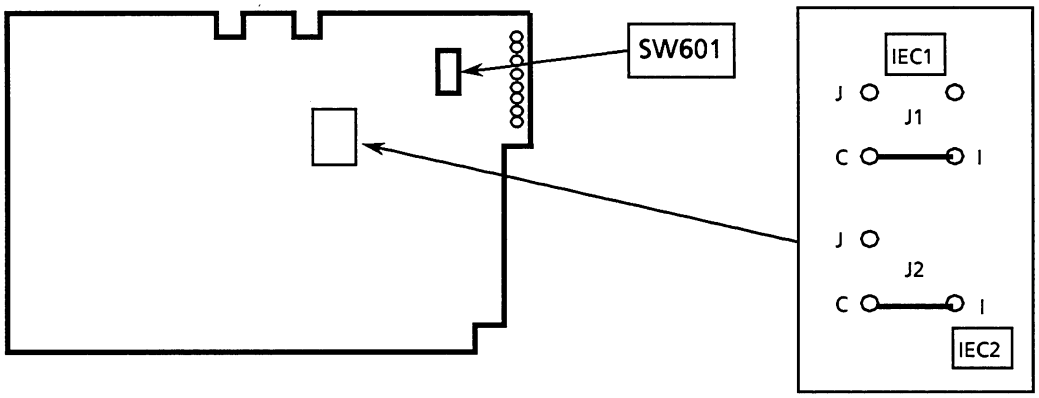
DIP Switch SW102

Bit	Function	Initial setting
1	Not used	OFF
2	Not used	OFF
3	Not used	OFF
4	ON : Watch dog timer does not function	OFF

DIP Switch SW103

Bit	Function	Initial setting
1	Not used	OFF
2	Not used	OFF
3	Not used	OFF
4	Not used	OFF
5	Not used	OFF
6	Not used	OFF
7	ON: Use for additional RAM	OFF
8	ON: Use in debug mode	OFF

7-1-2 DPU Board, UP-0670



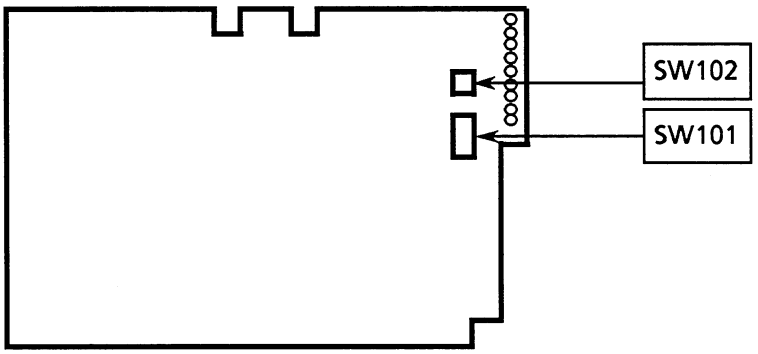
DIP Switches,SW601

Bit	Function	Initial setting
1	Telemetry channel selection (ON : USA ; OFF : Others)	ON
2	Not used	OFF
3	Not used	OFF
4	Not used	OFF

Jumpers J1 & J2: Shorted by wire

Jumper	Function	Initial setting
J1	Filter characteristics (I–C:IEC ; J–C:Japan standard)	I–C
J2	See the circuit diagram of UP-0670 18/19	I–C

7-1-3 COM3 (QI-816P) Board, UP-0563



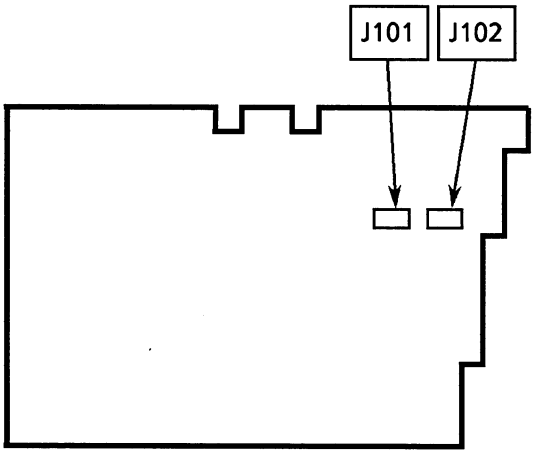
DIP Switch, SW101

Bit	Function	Initial setting
1	Not used	OFF
2	Not used	OFF
3	Not used	OFF
4	Not used	OFF
5	Not used	OFF
6	Not used	OFF
7	Not used	OFF
8	Not used	OFF

DIP Switch, SW102

Bit	Function	Initial setting
1	SYSTEM (Normal operating mode : ON , Debug mode : OFF	ON
2	WDTRST (Reset with WDT Error : ON/OFF)	OFF
3	WDTINT (Interrupt Request from WDT : ON/OFF)	ON
4	SWWDT (Software WDT Function : ON/OFF)	ON

7-1-4 I/O Board, UP-0797

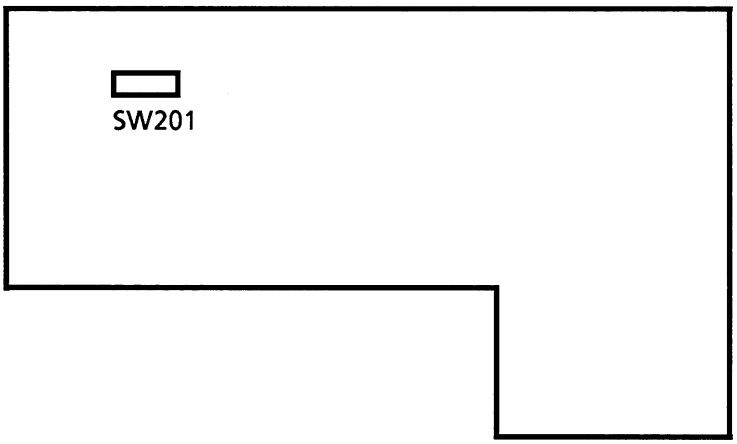


Jumpers J101 & J102: Shorted by wire

Jumper	Function	Initial setting
J101	AUX1W Gain select Short : ×1 Open : ×5	Short
J102	AUX2W Gain select Short : ×1 Open : ×5	Short

7-2 Display Unit, VD-881R

7-2-1 OPERATION CONTROL Board, UP-0801

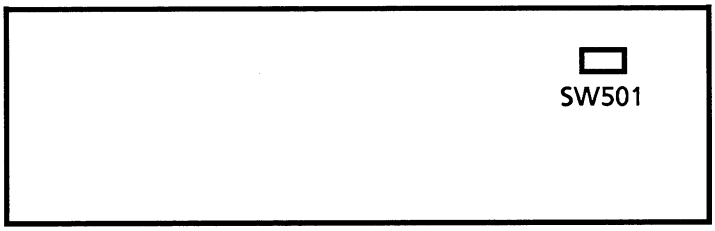


Dip switch SW201

Bit	Function	Initial setting
1	ON : Baud rate is 9600bps	OFF
2	ON : Alarm pole goes on and off (HT Sync)	OFF
3	Not used	OFF
4	Not used	OFF

7-3 Keypad, RY-881PA

7-3-1 OPERATION Board, UR-3025



Dip switch SW501

Bit	Function	Initial setting
1	ON : Baud rate is 9600bps	OFF
2	Not used	OFF
3	Not used	OFF
4	Not used	OFF

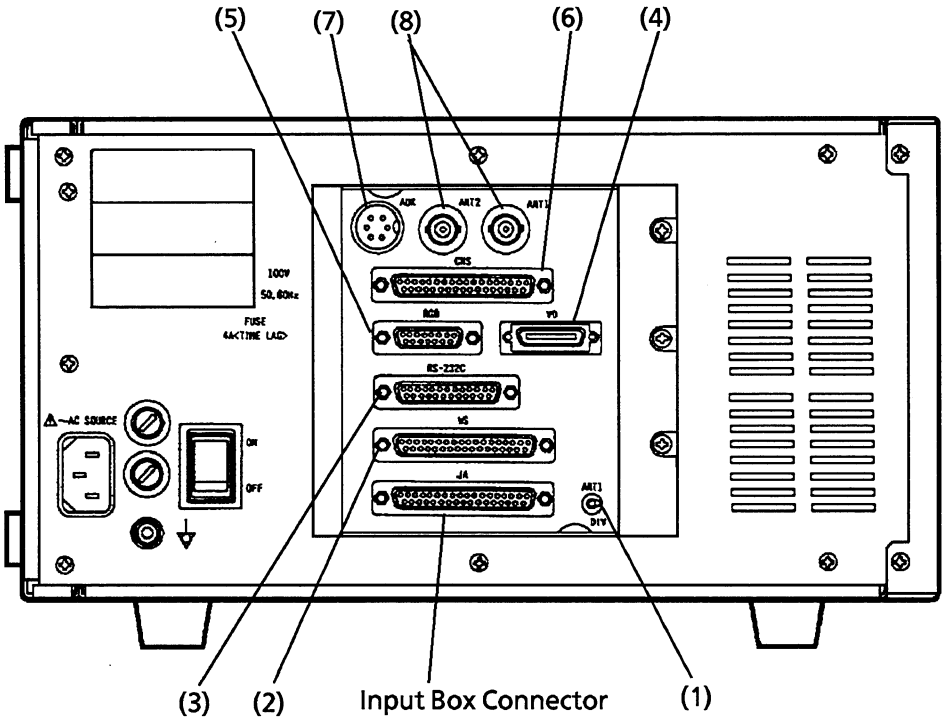
Section 8 CONNECTOR PIN ASSIGNMENT

8-1 Main Unit, MU-881R

8-1-1 External Connectors and Switches on the Main Unit

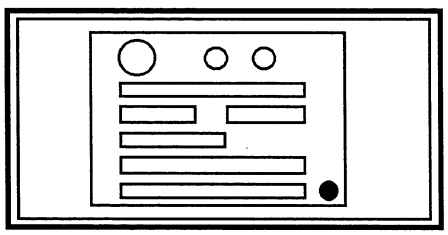
(See Section 1-8 CONNECTION DIAGRAM, and Section 2. SIGNAL LIST.)

Rear Panel



1) Antenna Selector Switch

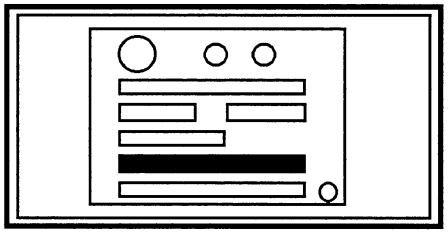
Model: ATE1D-6M3-10
Part No: 317319
Function: Selects the antenna operation; ANT 1 or Diversity

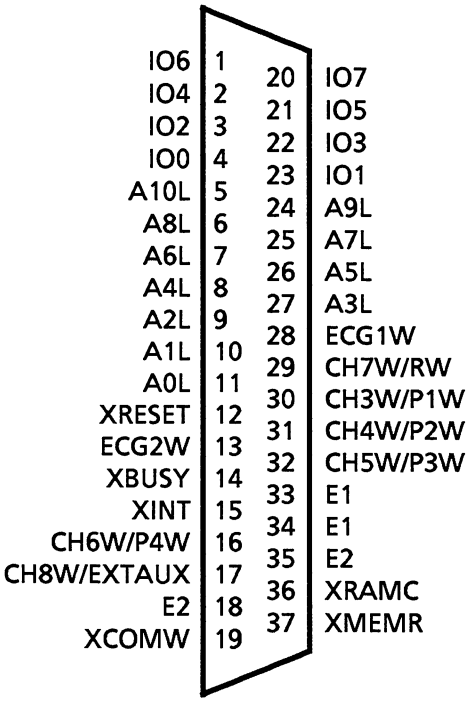


2) WS Connector

Circuit No.: CN103
Model: RDCD-37SE-LNA, Female
Part No.: 081092
Mating Type: D Sub 37P Male Connector

Mating Connector: BSM-WS Connector Cable
Part No.: YS-015P3 (for WS-840R/841R)
367844 (for WS-880R)

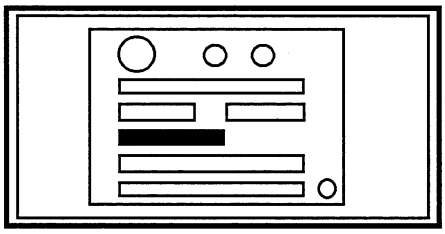


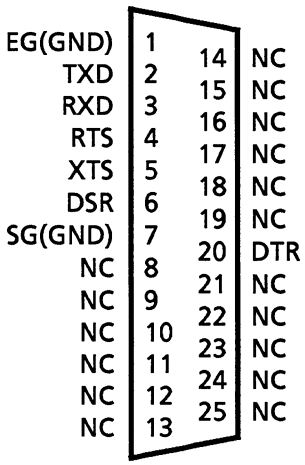


Construction of D Sub 37P Male Connector			Model	Part No.
Connector	Caulked Type	Housing	CDC-37P	080404
		Contact Pin	CD-PC-121	080431
	Souldered Type		HDCD-37P	080725
Case			HDC-CTH1	080672

3) RS-232C Connector

Circuit No.: CN103
Model: RDBD-25SE-LNA, Female
Parts No.: 081109
Mating Type: D Sub 25P Male Connector



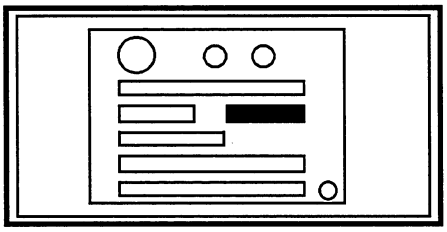


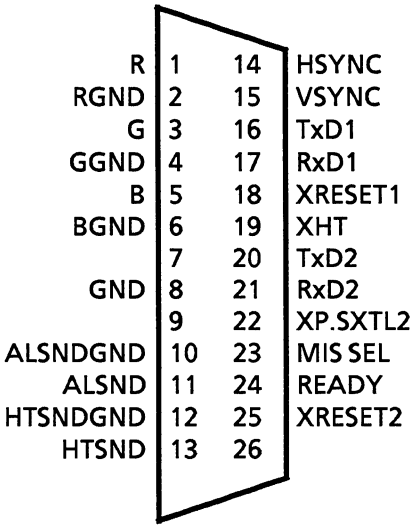
Construction of D Sub 25P Male Connector			Model	Part No.
Connector	Caulked Type	Housing	CDB-25P	080413
		Contact Pin	CD-PC-121	080431
	Souldered Type		HDBB-25P	080779
Case			HDB-CTH1	080663

4) VD Connector

Circuit No.: CN102
Model: DX10M-26SE
Parts No.: 354359

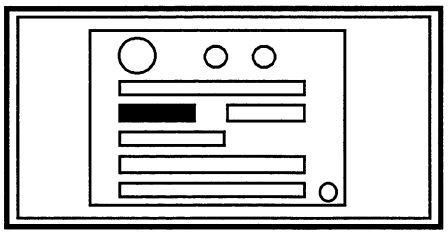
Mating Connector : VD Connector Cord
Part No.: YS-023P8 (1.5 m)
YS-024P5 (3 m)
YS-025P2 (10 m)

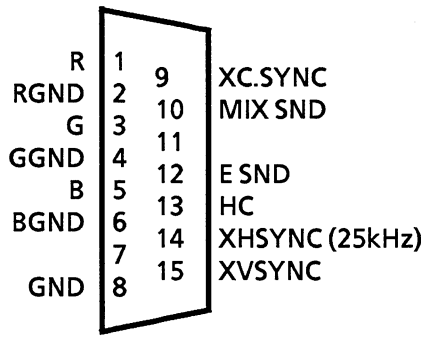




5) RGB Output Connector

Circuit No.: CN103
Model: RDAD-15SE-LNA, female
Parts No.: 367862
Mating Type: D Sub 15P Male Connector



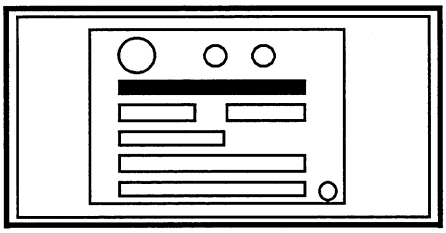


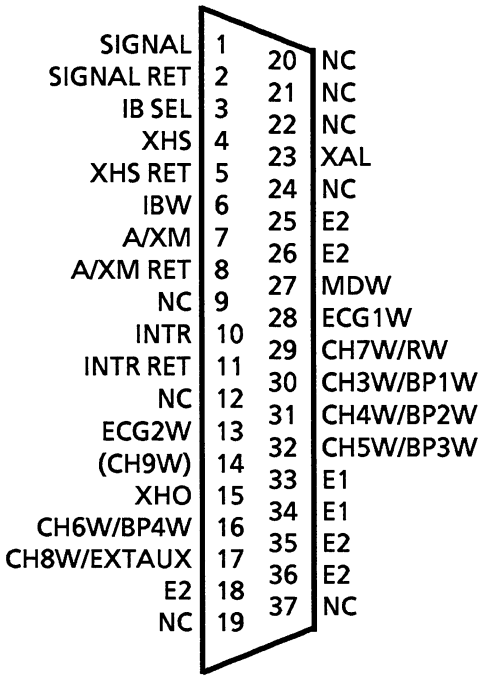
Construction of D Sub 25P Male Connector			Model	Part No.
Connector	Caulked Type	Housing	CDA-15P	080333
		Contact Pin	CD-PC-121	080431
	Souldered Type		HDAB-15P	080699
Case			HDA-CTH1	080564

6) CNS Connector

Circuit No.: CN105
Model: RDCD-37SE-LNA, Female
Part No.: 081092
Mating Type: D Sub 37P Male Connector

Mating Connector : BSM-JJConnector Cable, YS-006P2

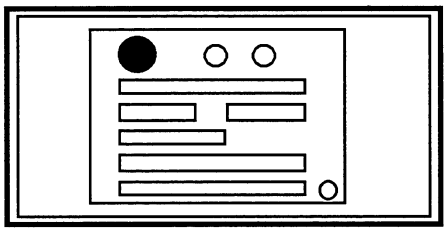




7) AUX IN Connector

Circuit No.: CN104
Model: RM12BRD-6S
Part No: 079772
(See Section 1-10, RELATED INSTRUMENTS CONNECTION for more information.)

Mating Connector : RM12BPG-6P
Part No.: 078541



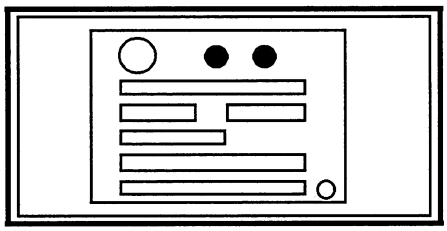
The table below lists the type of connectable auxiliary units and the signal name of each pin in this AUX IN connector.

Pin No..	Signal Name	Auxiliary Instrument For			
		CO_2	SpO_2	$tcPO_2/tcPCO_2$	Auxiliary Waveform Input
1	AUX1IN (±8 V)	$ETCO_2$ (20 mmHg/V)	SpO_2 (100%/V)	$tcPCO_2$ (200 mmHg/V*)	Not used
2	AUX2IN (±8 V)	CO_2W (20 mmHg/V)	Not used	$tcPO_2$ (200 mmHg/V*)	Auxiliary Waveform
3	AGND	Ground for Analog signal	Ground for Analog signal	Ground for Analog signal	Ground for Analog signal
4	AUX1C (Open collector type)	$ETCO_2$ alarm	SpO_2 alarm	$tcPCO_2$ alarm	Not used
5	AUX2C (Open collector type)	CO_2 measure	SpO_2 measure	$tcPO_2$ alarm	Not used
6	DGND	Ground for Digital signal	Ground for Digital signal	Ground for Digital signal	Not used

* To increase the gain to 1000 mmHg/V, cut the jumpers, J101 and J102 of the I/O board, UP-0797 (refer to 7-1-4).

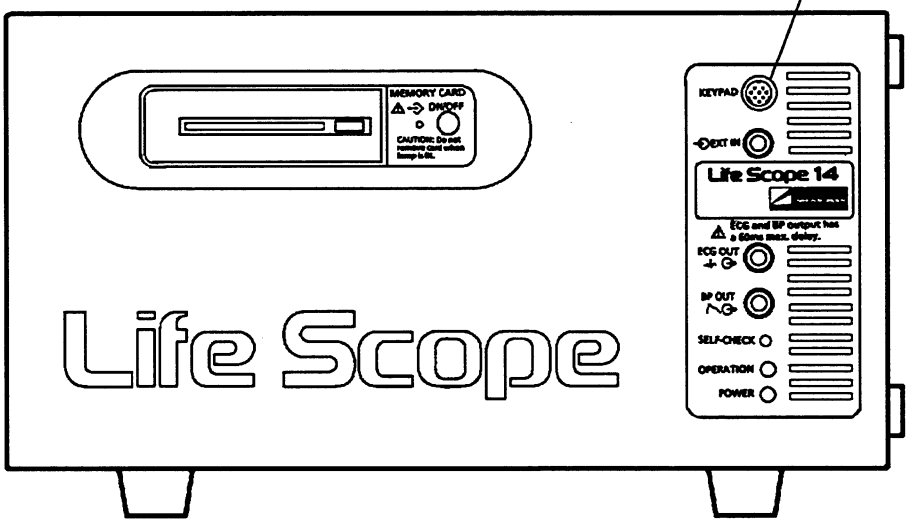
8) ANT1, ANT2 Connector

BNC Connector



(9)

Front Panel



9) Keypad Connector

Circuit No.:	CN104 in the FRONT CONNECTOR board or CN108 in the OPERATION CONTROL board (Display Unit)
Model:	HR212-10R-8SDL
Parts No.:	356802
Mating Connector :	Keypad Connector Cord
Part No.:	359996

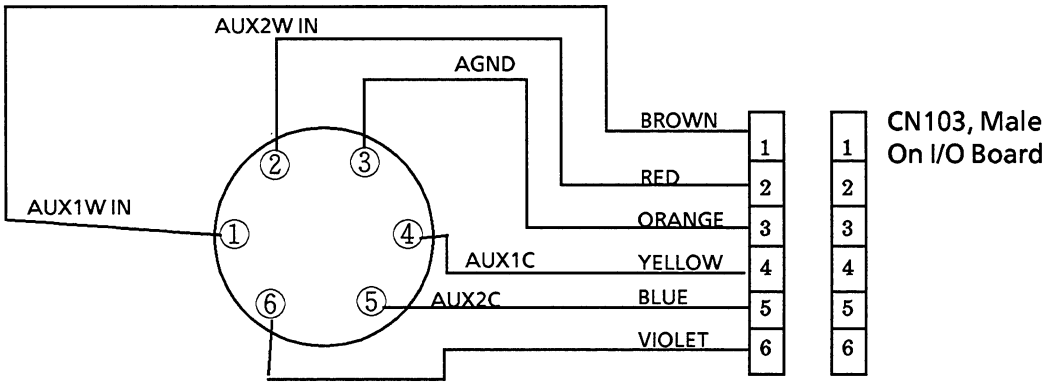
+ 5V	1	5	XKREADY
KREADY	2	6	E2
TxD2	3	7	E2
RxD2	4	8	XP.SCTL2

8-1-2 Internal Connectors and Wires in Main Unit

1) I/O Board Connector

Circuit No.: CN103
Model: M60-06-30-134P (to AUX Input)
Part No.: 089725

Connecting cable: CN-ASSY M62-06-0004SA L=300
Part No.: 089645



2) DPU Board Connector

Circuit No.: CN104 (to J3 on ZR-800P/PA)
Model: DF11-16DP-2DS
Part No.: 084356

Connecting Cable: DF11-16DS-2C(20)
Part No.: 319282

DATA	1	9	NC
CLK	2	10	RT
LE	3	11	RD
NC	4	12	NC
+8V	5	13	NC
NC	6	14	NC
E1	7	15	NC
E1	8	16	E1

3) COM 3 Board Connector

Circuit No.: CN104 (to I/O Board)
Model: HIF3BA-40PA-2.54DS
Part No.: 085934

Connecting cable: HIF3BA-40D-AC-10
Part No.: 319157

SIGNAL	1	2	NC
SIGNAL RET	3	4	NC
IB SEL	5	6	NC
XHS	7	8	XAL
XHS RET	9	10	NC
IBW	11	12	E2
A/XM	13	14	E2
A/XM RET	15	16	MDW
NC	17	18	ECG1W
INTR	19	20	CH7W/RW
INTR RET	21	22	CH3W/P1W
NC	23	24	CH4W/P2W
ECG2W	25	26	CH5W/P3W
(CH9W)	27	28	E1
XHO	29	30	E1
CH6W/P4W	31	32	E2
CH8W/EXTAUX	33	34	E2
E2	35	36	E2
E2	37	38	E2
E2	39	40	E2

4) MOTHER Board Connectors

- **To Fan Motor**

Circuit No.: CN112 (to fan's motor)
Model: M60-02-30-114P
Part No.: 090206

Socket Contact: M62C84-4
Part No.: 090233

Socket Mould: M62M84-02
Part No.: 090224

E5	1
+ 12V	2

- **To FRONT CONNECTOR Board**

Circuit No.: CN113 (to CN101 of FRONT CONNECTOR Board)
Model: FFC-20BSM1#02
Part No.: 091232A

Connecting Cable: HKP-20FS02-10BT(30)
Part No.: 088904

+ 5VL	1	11	+ 5VB
+ 5VBL	2	12	EXTRDY
E2	3	13	IOTXD3
E2	4	14	IORXD3
P1W	5	15	XKEYRST2
ECG1W	6	16	STNBY
E1	7	17	E2
E1	8	18	E2
EXTIN	9	19	XEXTRST
AUX2IN	10	20	NC

5) REGULATOR Board Connector

- **To MOTHER Board**

Circuit No.: CN105 (to CN111 on MOTHER board)
Model: 171457-1
Part No.: 268069

Connecting Cable: SC-018R Connecor Cord
Part No.: 372437

+ 5.1V (8.7A)	1	12	+ 5.1V (8.7A)
+ 5VS	2	13	ER2
E2	3	14	E2
+ 5VB	4	15	E2
PWRCTL	5	16	NC
	6	17	E4
+ 21V (1.3A)	7	18	E4
–21V (0.15A)	8	19	E1
+ 8V (0.75A)	9	20	ER1
–8V (0.7A)	10	21	E5
+ 12V (0.15A)	11		

- **To TRANSFORMER UNIT Board**

Circuit No.: CN102 (to CN101 on TRANSFORMER UNIT board)
Model: 172034-1
Part No.: 83407

0	7	1	12V (0.9A)
NC	8	2	12V (0.7A)
NC	9	3	21V (3.3A)
		4	21V (0.15A)
0	10	5	0
7.5V (1A)	11	6	7.5V (1A)

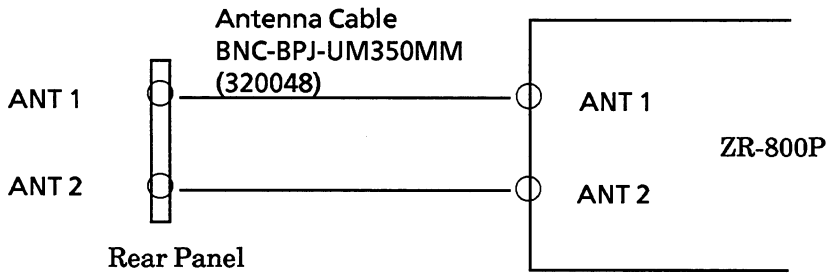
6) MEMORY CARD Board Connector

Circuit No.: CN101 (to CN201 on I/O Board)
Model: HIF-6-68PA-1.27DS
Part No.: 356767

Connecting cable: HIF6-68D-1.27R-AA(30)
Part No.: 369147

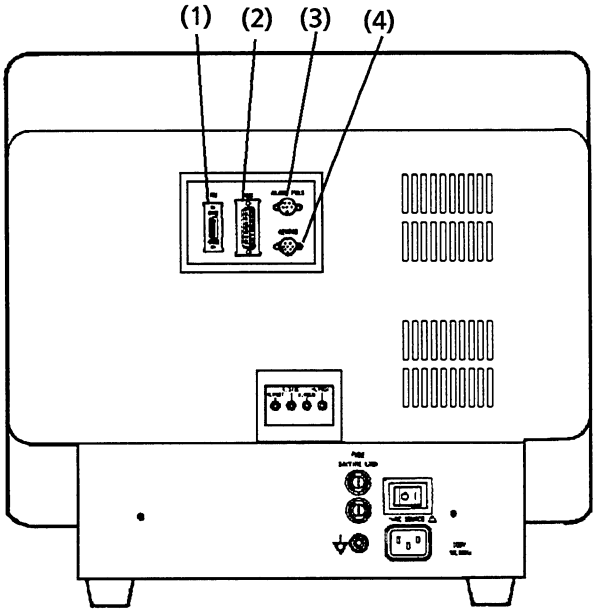
MD3	1A	1B	MCSW
MD5	2A	2B	MD4
MD7	3A	3B	NC
MA10	4A	4B	XCE1
MA11	5A	5B	XOE
MA8	6A	6B	MA9
MA14	7A	7B	MA13
RDY/XBSY	8A	8B	XWE
MCLED	9A	9B	+ 5V
MA15	10A	10B	MA16
MA7	11A	11B	MA12
MA5	12A	12B	MA6
MA3	13A	13B	MA4
MA1	14A	14B	MA2
MD0	15A	15B	MA0
MD2	16A	16B	MD1
E2	17A	17B	WP
XCD1	18A	18B	E2
MD12	19A	19B	MD11
MD14	20A	20B	MD13
XCE2	21A	21B	MD15
RFU1	22A	22B	XRFSH
MA17	23A	23B	RFU2
MA19	24A	24B	MA18
MA21	25A	25B	MA20
VPP	26A	26B	+ 5V
MA23	27A	27B	MA22
MA25	28A	28B	MA24
RFU4	29A	29B	RFU3
RFU6	30A	30B	RFU5
BVD2	31A	31B	XREG
MD8	32A	32B	BVD1
MD10	33A	33B	MD9
E2	34A	34B	XCD2

8-1-3 Wiring


Antenna Cable
BNC-BPJ-UM350MM
(320048)
ANT 1
ANT 2
Rear Panel
ANT 1
ANT 2
ZR-800P

8-2 Display Unit, VD-881R

8-2-1 External Connectors on the Display Unit



1) MU Connector

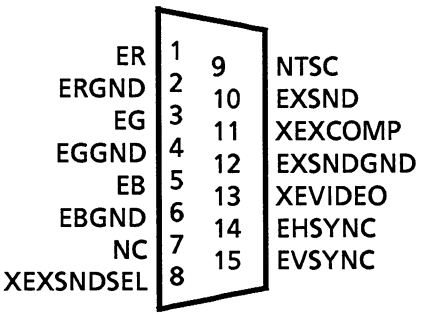
Circuit No. : CN101
Model : DX20M-26S
Part No. : 356829

Mating Connector: VD Connector Cord
Part No.: YS-0238

MR	1	14	MHSYNC
MRGND	2	15	MVSYNC
MG	3	16	RXD1
MGGND	4	17	TXD1
MB	5	18	XRESET1
MBGND	6	19	XHT
NC	7	20	TXD2
NC	8	21	RXD2
NC	9	22	XP.SCTL2
ALSNDGND	10	23	M/S SEL
ALSND	11	24	READY
HTSNDGND	12	25	XRESET2
HTSND	13	26	NC

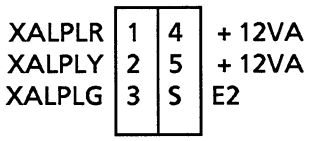
2) MU Auxiliary Unit Connector

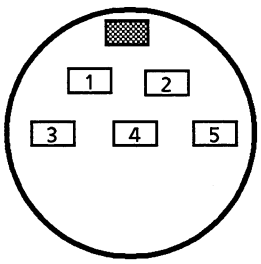
Circuit No. : CN102
Model : SDAB-15SSL-LNK
Part No. : 362724
Mating Type: D Sub 15P Male Connector



3) Alarm Pole Connector

Circuit No. : CN108
Model : HR212-10R-5SD
Part No. : 356785

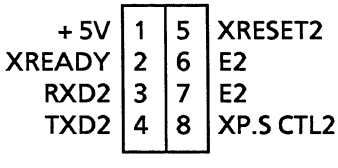


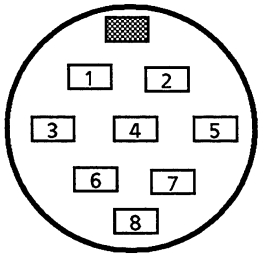


4) Keypad Connector

Circuit No. : CN106
Model : HR212-10RB-8SD
Part No. : 369441

Mating Connector: Keypad Connector Cord
Part No.: 359996



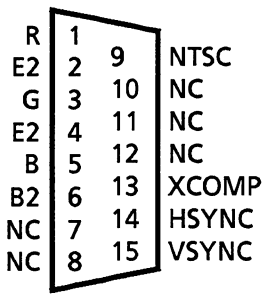


8-2-2 Internal Connectors in the Display Unit

1) CRT Unit Input Connector

Circuit No. : CN103
Model : RDAD-15SE-LNA
Part No. : 081118

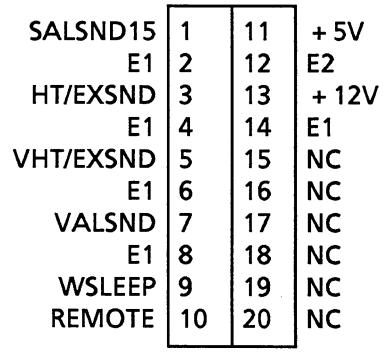
Connecting Cable : CDA-15PP-100
Part No. : 366007



2) OPERATION (VR) Board's CN101 Connector

Circuit No.: CN104
Model : HIF3BA-20PA-2.54DSA
Part No. : 085899

Connecting Cable : HIF3BA-20D-AC-60
Part No. : 357828



3) Speaker Connector

Circuit No. : CN105
Model : M60-03-30-114P
Part No. : 089663

Connecting Cable: CN-ASSY M62-03-0018SA L=300
Part No.: 089654

SPKR-	1
SPKR +	2
NC	3

4) SC-019R Power Supply Unit's CN101 Connector

Circuit No. : CN107
Model : FFC-14BSM1#02ST
Part No. : 091205A

Connecting Cable : HKP-14FS02-7BT
Part No. : 099233

+ 5V	1	8	E1
+ 5V	2	9	-12V
E2	3	10	-12V
E2	4	11	XP.SCTL1
+ 12V	5	12	NC
+ 12V	6	13	NC
E1	7	14	NC

5) LED Board (UP-0806)'s CN101 Connector

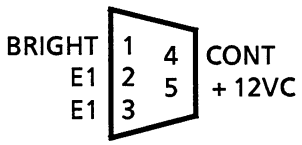
Circuit No.: CN103
Model : HKP-6ML-3BT
Part No. : 085515

Connecting Cable : HKP-6FS02-3BT(20)
Part No. : 089119

+ 5V	1	4	E1
E2	2	5	REMOTE
+ 12V	3	6	NC

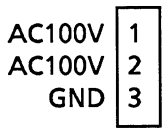
6) CRT Unit Connector

Circuit No.:	CN102
Model :	B5B-EH
Part No.:	313377



7) CRT Unit Power Supply Connector

Circuit No. :	CN105
Model :	350429-1
Part No.:	083384
Connecting Cable:	CRT Connecting Cable
Part No.:	371367



8-3 Keypad, RY-881PA

8-3-1 External Connectors on the Keypad

1) Main Unit or Display Unit Connector

Circuit No.: CN101
Model: HR212-10RA-8SDL
Part No.: 356811

Mating Connector: Keypad Connector Cord
Part No.: 359996

+5V	1	5	XRESET2
XREADY	2	6	E2
RXD2	3	7	E2
TXD2	4	8	XP.S CTL2

Section 9 ELECTRICAL PARTS LIST

ASSY	CKT NO.	PART NO.	QTY	DESCRIPTION
UP-1234	IC101	146584	1	CMOS TC74HC74AP

- TC74HC74AP — Part name
- CMOS — Part abbreviation
- 1 — Quantity used (0 is shown for compatible part)
- 146584 — Nihon Kohden part number
- IC101 — Circuit No. indicated on the circuit diagram and PCB (* means compatible part)
- UP-1234 — Assembly name

ABBREVIATIONS

TRANSISTOR

TR	Transistors other than below
FET	FET
PTR	Phototransistor, photoreflector, and photocoupler

DIODE

D	Diodes other than below
LED	LED
ZD	Zener diode

IC

IC	ICs other than below
ADIC	A/D converter and D/A converter
CRTC	CRT controller
CMOS	CMOS
HIC	Hybrid
OPIC	Operational amplifier
REG	Regulator
RAM	RAM
TTL	TTL

SWITCH

SW	Switches other than below
ATT	Attenuator
RS	Rotary switch

CAPACITOR

C	Titanate, paper block, oil and mica
CEC	Ceramic
CM	Module
EC	Electrolyte
FLC	Film
TAC	Tantalum
VC	Variable capacitor

RESISTOR (Carbon and metal film type are omitted)

R	Mold, solid and cement
RM	Module
WR	Wirewound

VARIABLE RESISTOR

VR	Single rotation
POT	Multi rotation potentiometer
WVR	Wirewound

TRANSFORMER

TF	Transformers other than below
COIL	Choke, rotator, flyback and deflection yoke
PT	Power

CONNECTOR

CN	Connectors other than below
CNA	Harness cord
PCN	Mounted on PC board

MIISCELLANEOUS

ANT	Antenna
BATT	Battery
CLUT	Electromagnetic clutch
CORD	Cord
DISP	CRT, LCD, plasma display, and fluorescent screen
FAN	Fan
FUSE	Fuse, fuse holder and thermal fuse
GAGE	Gauge
HEAD	Thermal head and discharge head
LAMP	Bracket type lamp
MOTOR	Motor
PUMP	Pump
RY	Relay
SP	Speaker, headphone and buzzer
TUBE	Vacuum tube, discharge tube, neon tube and gas arrestor
UNIT	Assembled unit
VALV	Electromagnetic valve
XTAL	Crystal oscillator

ASSY	CKT NO.	PART NO.	QTY	DESCRIPTION	
CD-130P CHASSIS 1					
CD-130P		079772	1	CN	RM12BRD-6S
CD-130P		090224	1	CN	socket M62 M83-02
CD-130P		090233	2	CN	socket contact M62C84-4
CD-130P		320048	2	CNA	antenna cord BNC-BPJ-UM 350MM
CD-130P		320271	2	CN	BNC-J cap
CD-130P		367737	1	FAN	fan motor ASF-84371 12V type
CD-130P		378556	1	CNA	M62-06-0004SA L = 30
CD-131P CHASSIS 1					
CD-131P		089654	1	PCN	M62-03-0018SA (30)
CD-131P	SP001	073662	1	SP	EAS-65P34S 16OHM
CD-137P CHASSIS 2					
CD-137P		088904A	1	PCN	HKP-20FS02-10BT(30) terminal
CD-137P		319157	1	PCN	HIF3BA-40D-AC-10
CD-137P		369147	1	CNA	HIF6-68D-1.27R-AA(30)
CD-157P CHASSIS 2					
CD-157P		089119A	1	PCN	HKP-6FS02-3BT(20)
CD-157P		357828	1	CNA	HIF3BA-20D-AC-60
CD-157P		366007A	1	CNA	CDA-15PP-100A
CD-157P		410325B	1	DISP	QA1465A 14b inch color-CRT unit
SC-018RA POWER TRANSFOMER UNIT					
SC-018RA	F101	103996	1	FUSE	SAU-3A (GDL-3)
SC-018RA	F101	104825	1	FUSE	fuse holder FEU031 1681
SC-018RA	F101	104834	1	FUSE	fuse cap FEK031.1661
SC-018RA	F102	103996	1	FUSE	SAU-3A (GDL-3)
SC-018RA	F102	104825	1	FUSE	fuse holder FEU031 1681
SC-018RA	F102	104834	1	FUSE	fuse cap FEK031.1661
SC-018RA	LF101	024252	1	NFLT	SUP-E3G-E-2 line filter
SC-018RA	SW101	370368	1	SW	JW-M22RKK
SC-018RJ POWER TRANSFOMER UNIT					
SC-018RJ	F101	103996	1	FUSE	SAU-3A (GOL-3)
SC-018RJ	F101	104825	1	FUSE	fuse holder FEU031 1681
SC-018RJ	F101	104834	1	FUSE	fuse cap FEK031.1661
SC-018RJ	F102	103995	1	FUSE	SAU-3A (GDL-3)
SC-018RJ	F102	104825	1	FUSE	fuse holder FEU031.1681
SC-018RJ	F102	104834	1	FUSE	fuse cap FEK031.1661
SC-018RJ	LF101	024252	1	NFLT	SUP-E3G-E-2 line filter
SC-018RJ	SW101	370368	1	SW	JW-M22RkK
SC-018RJ	T101	365823	1	PT	power transformer for SC-018RJ
SC-018RJ	TB101	103131	1	TERM	ULC-505-3P-C
SC-018RK POWER TRANSFOMER UNIT					
SC-018RK	F101	104576	1	FUSE	179 120-2A ELU
SC-018RK	F101	104825	1	FUSE	fuse holder FEU031 1681
SC-018RK	F101	104843	1	FUSE	fuse cap FEK031.1663
SC-018RK	F102	104576	1	FUSE	179 120-2A ELU
SC-018RK	F102	104825	1	FUSE	fuse holder FEU031 1681
SC-018RK	F102	104843	1	FUSE	fuse cap FEK031.1663
SC-018RK	LF101	024252	1	NFLT	SUP-E3G-E-2 line filter
SC-018RK	SW101	370368	1	SW	JW-M22RKK

9. ELECTRICAL PARTS LIST

ASSY	CKT NO.	PART NO.	QTY	DESCRIPTION	
SC-019RA	**POWER SUPPLY UNIT**				
SC-019RA		095095	2	CNA	V1.25-4 with cord (250) black
SC-019RA		098252	1	PCN	HKP-14FS02-7BT(40)
SC-019RA	CN102	156876	1	PCN	B3P-VH
SC-019RA	CN105	331981	1	PCN	350429-1 (3P)
SC-019RA	CN106	091205A	1	PCN	FFC-14BSM1#02ST
SC-019RA	C102	040172	1	EC	KME35VB1000 35/1000
SC-019RA	C103-C104	158214	2	EC	KME25VB-220 25V 220UF
SC-019RA	C106-C107	040332	2	EC	KME50VB 1 50V 1MF
SC-019RA	C109	040323	1	EC	KME35VB 220 35V220MF
SC-019RA	D101	004354	1	D	S5VB20
SC-019RA	D103-D104	003649	2	D	1SS81
SC-019RA	D105	004354	1	D	S5VB20
SC-019RA	D106	003943	1	D	V06C (1.1A200V)
SC-019RA	D107-D112	003649	6	D	1SS81
SC-019RA	D113	003943	1	D	V06C (1.1A200V)
SC-019RA	F101	104005	1	FUSE	SAU-4A
SC-019RA	F101	104825	1	FUSE	fuse holder FEU031 1681
SC-019RA	F101	104834	1	FUSE	fuse cap FEK031.1661
SC-019RA	F102	104005	1	FUSE	SAU-4A
SC-019RA	F102	104825	1	FUSE	fuse holder FEU031 1681
SC-019RA	F102	104834	1	FUSE	fuse cap FEK031.1661
SC-019RA	F105-F107	346207	3	FUSE	23902.5 LITTLE
SC-019RA	LF101	024252	1	NFLT	SUP-E3G-E-2 line filter
SC-019RA	Q101	002356	1	TR	2SD717-Y
SC-019RA	Q102	002026	1	TR	2SC2324K
SC-019RA	Q103	002855	1	FET	2SK30A GR
SC-019RA	SW101	370368	1	SW	JW-M22RKK
SC-019RA	VR101	062781	1	VR	GF06P 1 KOHM
SC-019RJ	**POWER SUPPLY UNIT**				
SC-019RJ		095095	2	CNA	V1.25-4 with cord (250) black
SC-019RJ		098252	1	PCN	HKP-14FS02-7BT(40)
SC-019RJ	CN102	156876	1	PCN	B3P-VH
SC-019RJ	CN105	331981	1	PCN	350429-1 (3P)
SC-019RJ	CN106	091205A	1	PCN	FFC-14BSM1#02ST
SC-019RJ	C102	040172	1	EC	KME35VB1000 35/1000
SC-019RJ	C103-C104	158214	2	EC	KME25VB-220 25V 220UF
SC-019RJ	C106-C107	040332	2	EC	KME50VB 1 50V 1MF
SC-019RJ	C109	040323	1	EC	KME35VB 220 35V220MF
SC-019RJ	D101	004354	1	D	S5VB20
SC-019RJ	D103-D104	003649	2	D	1SS81
SC-019RJ	D105	004354	1	D	S5VB20
SC-019RJ	D106	003943	1	D	V06C (1.1A200V)
SC-019RJ	D107-D112	003649	6	D	1SS81
SC-019RJ	D113	003943	1	D	V06C (1.1A200V)
SC-019RJ	F101	104005	1	FUSE	SAU-4A
SC-019RJ	F101	104825	1	FUSE	fuse holder FEU031 1681
SC-019RJ	F101	104834	1	FUSE	fuse cap FEK031.1661
SC-019RJ	F102	104005	1	FUSE	SAU-4A
SC-019RJ	F102	104825	1	FUSE	fuse holder FEU031 1681
SC-019RJ	F102	104834	1	FUSE	fuse cap FEK031.1661
SC-019RJ	F105-F107	346207	3	FUSE	23902.5 LITTLE
SC-019RJ	LF101	024252	1	NFLT	SUP-E3G-E-2 line filter
SC-019RJ	Q101	002356	1	TR	2SD717-Y
SC-019RJ	Q102	002026	1	TR	2SC2324K
SC-019RJ	Q103	002855	1	FET	2SK30A GR
SC-019RJ	SW101	370368	1	SW	JW-M22RKK
SC-019RJ	VR101	062781	1	VR	GF06P 1 KOHM
SC-019RK	**POWER SUPPLY UNIT**				
SC-019RK		095095	2	CNA	V1.25-4 with cord (250) black
SC-019RK		098252	1	PCN	HKP-14FS02-7BT(40)
SC-019RK	CN102	156876	1	PCN	B3P-VH
SC-019RK	CN105	331981	1	PCN	350429-1 (3P)
SC-019RK	CN106	091205A	1	PCN	FFC-14BSM1#02ST
SC-019RK	C102	040172	1	EC	KME35VB1000 35/1000
SC-019RK	C103-C104	158214	2	EC	KME25VB-220 25V 220UF
SC-019RK	C106-C107	040332	2	EC	KME50VB 1 50V 1MF
SC-019RK	C109	040323	1	EC	KME35VB 220 35V220MF
SC-019RK	D101	004354	1	D	S5VB20
SC-019RK	D103-D104	003649	2	D	1SS81
SC-019RK	D105	004354	1	D	S5VB20

ASSY	CKT NO.	PART NO.	QTY	DESCRIPTION	
SC-019RK	D106	003943	1	D	V06C (1.1A200V)
SC-019RK	D107-D112	003649	6	D	1SS81
SC-019RK	D113	003943	1	D	V06C (1.1A200V)
SC-019RK	F101	104576	1	FUSE	179 120-2A ELU
SC-019RK	F101	104825	1	FUSE	fuse holder FEU031 1681
SC-019RK	F101	104843	1	FUSE	fuse cap FEK031.1663
SC-019RK	F102	104576	1	FUSE	179 120-2A ELU
SC-019RK	F102	104825	1	FUSE	fuse holder FEU031 1681
SC-019RK	F102	104843	1	FUSE	fuse cap FEK031.1663
SC-019RK	F105-F107	346207	3	FUSE	23902.5 LITTLE
SC-019RK	LF101	024252	1	NFLT	SUP-E3G-E-2 line filter
SC-019RK	Q101	002356	1	TR	2SD717-Y
SC-019RK	Q102	002026	1	TR	2SC2324K
SC-019RK	Q103	002855	1	FET	2SK30A GR
SC-019RK	SW101	370368	1	SW	JW-M22RKK
SC-019RK	VR101	062781	1	VR	GF06P 1 KOHM

UP-0272 ECG HEAD AMP BOARD

UP-0272	CN001	089895	1	PCN	PCN10EA-20P-2.54DS(05)
UP-0272	C001-C002	042357	2	TAC	204M1602 106M4 (10MF/16V)
UP-0272	C003	071236	1	CEC	TPD55Y5V1H104Z5-W 50V 0.1UF
UP-0272	C004	070718	1	TAC	204M3502 105MB (1MF/35V)
UP-0272	C005	071468	1	CEC	ECB T1H 470J5
UP-0272	C006	071307	1	CEC	DD05-989B101K500 500V 100PF
UP-0272	C007	071138	1	FLC	ECQ-V 1H 224JZ3 (0.22MF)
UP-0272	C008-C013	070834	6	FLC	ECQ-B 1H 102JZ3 0.001MF
UP-0272	C014-C015	046879	2	CEC	DE7090B 102K VA1-KC
UP-0272	D001-D004	071548	4	D	1S2076A RE
UP-0272	D005-D006	071539	2	D	1SS104,TPB2
UP-0272	D007-D008	071548	2	D	1S2076A RE
UP-0272	D011-D012	071539	2	D	1SS104,TPB2
UP-0272	D013-D014	071548	2	D	1S2076A RE
UP-0272	GA001	026811	1	TUBE	Y08-2100B
UP-0272	GA002-GA006	404475	5	TUBE	ceramic arrestor Y06S-100B
UP-0272	IC001	072975	1	REG	u PC78L05J-T
UP-0272	IC002	072984	1	REG	u PC79L05J-T
UP-0272	IC003	016181	1	OPIC	UPC812C
UP-0272	IC004	163262	1	CMOS	MC14051BCP
UP-0272	IC005	163128	1	ADIC	MC14094BCP
UP-0272	IC006	017091	1	CMOS	HD14040BP (MC14040BCP)
UP-0272	IC007	021718	1	HIC	EHD-HA1270 ISOLATE
UP-0272	IC008	021736	1	HIC	EHD-HA1272 ECGSEL
UP-0272	IC009-IC012	021727	4	HIC	EHD-HA1271 ECGBUF
UP-0272	PC001-PC003	002739	3	PTR	PC810A
UP-0272	Q001	071904	1	TR	2SA836 CeaD TZ
UP-0272	Q002	072093	1	FET	2SK163 L1eaL2-T
UP-0272	Q003-Q004	072066	2	TR	2SC1213AKDTZ
UP-0272	T001	036925	1	TF	T3772365 EP10PS transformer
UP-0272	T002	036916	1	TF	T3772356 EP10IS transformer
UP-0272	T003	036943A	1	TF	T3772383 EP10IS(red) transformer
UP-0272	VR001	062799	1	VR	GF06P 5 KOHM

UP-0318 CD HEAD AMP BOARD

UP-0318	CN001	089895	1	PCN	PCN10EA-20P-2.54DS(05)
UP-0318	CN002	079558A	1	CN	HR16-18R-10S(01) red
UP-0318	CN003	090215	1	PCN	M60-04-30-114P (4P)
UP-0318	C001-C002	070531	2	TAC	204M2002 106MB(10MF/20V)
UP-0318	C003	071236	1	CEC	TPD55Y5V1H104Z5-W 50V 0.1UF
UP-0318	C004	070718	1	TAC	204M3502 105MB (1MF/35V)
UP-0318	C006	070959	1	FLC	ECQ-B 1H 103JZ3 0.01MF
UP-0318	C007	042357	1	TAC	204M1602 106M4 (10MF/16V)
UP-0318	C008	070959	1	FLC	ECQ-B 1H 103JZ3 0.01MF
UP-0318	C009-C010	071094	2	FLC	ECQ-V 1H 104JZ3 (0.1MF)
UP-0318	C011	071174	1	FLC	ECQ-V 1H 474JZ3 (0.47MF)
UP-0318	C012	071094	1	FLC	ECQ-V 1H 104JZ3 (0.1MF)
UP-0318	C013-C014	070959	2	FLC	ECQ-B 1H 103JZ3 0.01MF
UP-0318	D001-D007	071548	7	D	1S2076A RE
UP-0318	GA001	026811	1	TUBE	Y08-2100B
UP-0318	IC001	072975	1	REG	u PC78L05J-T
UP-0318	IC002	072984	1	REG	u PC79L05J-T
UP-0318	IC003	163289	1	CMOS	MC14053BCP
UP-0318	IC004	015993	1	REG	LT1009CZ 2.5VREF
UP-0318	IC005	016083	1	OPIC	UPC4062C
UP-0318	IC006	016181	1	OPIC	UPC812C
UP-0318	IC007	015779	1	OPIC	LT1001CN8 LOW DRIFT
UP-0318	IC008	010739	1	OPIC	HA17903PS

9. ELECTRICAL PARTS LIST

ASSY	CKT NO.	PART NO.	QTY	DESCRIPTION	
UP-0318	IC009	163262	1	CMOS	MC14051BCP
UP-0318	IC010	017091	1	CMOS	HD14040BP (MC14040BCP)
UP-0318	IC011	163128	1	ADIC	MC14094BCP
UP-0318	IC012	017091	1	CMOS	HD14040BP (MC14040BCP)
UP-0318	IC013	021718	1	HIC	EHD-HA1270 ISOLATE
UP-0318	PC001-PC002	002739	2	PTR	PC810A
UP-0318	Q001-Q003	072066	3	TR	2SC1213AKDTZ
UP-0318	T001	036925	1	TF	T3772365 EP10PS transformer
UP-0318	T002	036916	1	TF	T3772356 EP10IS transformer
UP-0318	VR001	062932	1	VR	GF06P 2 KOHM
UP-0318	VR002-VR003	062781	2	VR	GF06P 1 KOHM
UP-0318	VR004	062807	1	VR	GF06P 10 KOHM
UP-0318	VR005	062781	1	VR	GF06P 1 KOHM

UP-0319 TEMP HEAD AMP BOARD

UP-0319	CN001	089895	1	PCN	PCN10EA-20P-2.54DS(05)
UP-0319	CN002	092775	1	CN	jack HLJ0527-01-030 with nut
UP-0319	CN003	090215	1	PCN	M60-04-30-114P (4P)
UP-0319	C001-C002	042357	2	TAC	204M1602 106M4 (10MF/16V)
UP-0319	C003	071236	1	CEC	TPD55Y5V1H104Z5-W 50V 0.1UF
UP-0319	C004	070718	1	TAC	204M3502 105MB (1MF/35V)
UP-0319	C006	070959	1	FLC	ECQ-B 1H 103JZ3 0.01MF
UP-0319	C007-C008	071094	2	FLC	ECQ-V 1H 104JZ3 (0.1MF)
UP-0319	C009	071343	1	CEC	DD05-989B471K500 500V 470PF
UP-0319	C010	070834	1	FLC	ECQ-B 1H 102JZ3 0.001MF
UP-0319	C011	071094	1	FLC	ECQ-V 1H 104JZ3 (0.1MF)
UP-0319	C014	070959	1	FLC	ECQ-B 1H 103JZ3 0.01MF
UP-0319	D001-D006	071548	6	D	1S2076A RE
UP-0319	GA001	026811	1	TUBE	Y08-2100B
UP-0319	IC001	072975	1	REG	u PC78L05J-T
UP-0319	IC002	072984	1	REG	u PC79L05J-T
UP-0319	IC003	163289	1	CMOS	MC14053BCP
UP-0319	IC004	015993	1	REG	LT1009CZ 2.5VREF
UP-0319	IC005	016083	1	OPIC	UPC4062C
UP-0319	IC006	015779	1	OPIC	LT1001CN8 LOW DRIFT
UP-0319	IC007	163262	1	CMOS	MC14051BCP
UP-0319	IC008	017091	1	CMOS	HD14040BP (MC14040BCP)
UP-0319	IC009	021718	1	HIC	EHD-HA1270 ISOLATE
UP-0319	PC001	002739	1	PTR	PC810A
UP-0319	Q001-Q002	072066	2	TR	2SC1213AKDTZ
UP-0319	T001	036925	1	TF	T3772365 EP10PS transformer
UP-0319	T002	036916	1	TF	T3772356 EP10IS transformer
UP-0319	VR001	062932	1	VR	GF06P 2 KOHM
UP-0319	VR002	062781	1	VR	GF06P 1 KOHM

UP-0369 PRESS HEAD AMP BOARD

UP-0369	CN001	089895	1	PCN	PCN10EA-20P-2.54DS(05)
UP-0369	CN002-CN003	079487	2	CN	HR16-13R-5S(02) orange
UP-0369	CN004	089672	1	PCN	M60-06-30-114P (6P)
UP-0369	C001-C002	070531	2	TAC	204M2002 106MB(10MF/20V)
UP-0369	C003	071236	1	CEC	TPD55Y5V1H104Z5-W 50V 0.1UF
UP-0369	C004	070718	1	TAC	204M3502 105MB (1MF/35V)
UP-0369	C006	070959	1	FLC	ECQ-B 1H 103JZ3 0.01MF
UP-0369	C007	071094	1	FLC	ECQ-V 1H 104JZ3 (0.1MF)
UP-0369	C008-C009	070531	2	TAC	204M2002 106MB(10MF/20V)
UP-0369	C010	071058	1	FLC	ECQ-V 1H 473JZ3 (0.047MF)
UP-0369	C011	071031	1	FLC	ECQ-V 1H 333JZ3 (0.033MF)
UP-0369	C012	071058	1	FLC	ECQ-V 1H 473JZ3 (0.047MF)
UP-0369	C013	071031	1	FLC	ECQ-V 1H 333JZ3 (0.033MF)
UP-0369	C016	070959	1	FLC	ECQ-B 1H 103JZ3 0.01MF
UP-0369	C017-C021	071094	5	FLC	ECQ-V 1H 104JZ3 (0.1MF)
UP-0369	D001-D004	071548	4	D	1S2076A RE
UP-0369	D006-D013	071539	8	D	1SS104,TPB2
UP-0369	D014-D015	071548	2	D	1S2076A RE
UP-0369	GA001	026811	1	TUBE	Y08-2100B
UP-0369	IC001	072975	1	REG	u PC78L05J-T
UP-0369	IC002	072984	1	REG	u PC79L05J-T
UP-0369	IC003	163289	1	CMOS	MC14053BCP
UP-0369	IC004	017091	1	CMOS	HD14040BP (MC14040BCP)
UP-0369	IC005	015993	1	REG	LT1009CZ 2.5VREF
UP-0369	IC006	016083	1	OPIC	UPC4062C
UP-0369	IC007-IC010	015779	4	OPIC	LT1001CN8 LOW DRIFT
UP-0369	IC011-IC013	016083	3	OPIC	UPC4062C
UP-0369	IC014	021718	1	HIC	EHD-HA1270 ISOLATE
UP-0369	PC001	002739	1	PTR	PC810A
UP-0369	PC002	002695	1	PTR	PC-827

ASSY	CKT NO.	PART NO.	QTY	DESCRIPTION	
UP-0369	Q001-Q003	072066	3	TR	2SC1213AKDTZ
UP-0369	Q004	071931	1	TR	2SA673AKCTZ
UP-0369	Q005	072066	1	TR	2SC1213AKDTZ
UP-0369	RA001	072636	1	RM	EXB-F8 V 103JYV
UP-0369	RA002	060916	1	RM	EXB-F5E-105J
UP-0369	T001	036925	1	TF	T3772365 EP10PS transformer
UP-0369	T002	036916	1	TF	T3772356 EP10IS transformer
UP-0369	VR001-VR002	062923	2	VR	GF06P 200 OHM

UP-0420 ECG HEAD AMP BOARD

UP-0420	CN003	079585A	1	CN	HR16-18R-10S(04) green

UP-0421 MAIN BOARD

UP-0421	CN001	089895	1	PCN	PCN10EA-20P-2.54DS(05)
UP-0421	CN002	089342	1	PCN	HKP-14FDS2-7,8,9T
UP-0421	C001-C002	070531	2	TAC	204M2002 106MB(10MF/20V)
UP-0421	C003	071236	1	CEC	TPD55Y5V1H104Z5-W 50V 0.1UF
UP-0421	C004	070718	1	TAC	204M3502 105MB (1MF/35V)
UP-0421	C005-C006	070959	2	FLC	ECQ-B 1H 103JZ3 0.01MF
UP-0421	C007	071094	1	FLC	ECQ-V 1H 104JZ3 (0.1MF)
UP-0421	C008-C016	070834	9	FLC	ECQ-B 1H 102JZ3 0.001MF
UP-0421	C017	070995	1	FLC	ECQ-B 1H 223JZ3 0.022MF
UP-0421	C018-C019	070531	2	TAC	204M2002 106MB(10MF/20V)
UP-0421	D001-D010	071548	10	D	1S2076A RE
UP-0421	D030-D039	071486	10	D	1SS104,TP3
UP-0421	GA001	026811	1	TUBE	Y08-2100B
UP-0421	IC001	072975	1	REG	u PC78L05J-T
UP-0421	IC002	072984	1	REG	u F286F286 PC79L05J-T
UP-0421	IC003	163289	1	CMOS	MC14053BCP
UP-0421	IC004	017091	1	CMOS	HD14040BP (MC14040BCP)
UP-0421	IC005	021718	1	HIC	EHD-HA1270 ISOLATE
UP-0421	IC006	016083	1	OPIC	UPC4062C
UP-0421	IC007-IC008	020523	2	OPIC	u PC812C yellow low noise
UP-0421	PC001-PC002	002739	2	PTR	PC810A
UP-0421	Q001-Q003	072066	3	TR	2SC1213AKDTZ
UP-0421	T001	036925	1	TF	T3772365 EP10PS transformer
UP-0421	T002	036916	1	TF	T3772356 EP10IS transformer
UP-0421	VR001	062799	1	VR	GF06P 5 KOHM

UP-0422 SUB BOARD

UP-0422	CN050	089235	1	PCN	HKP-14M5S-7,8,9T receptacle male
UP-0422	C050-C057	070531	8	TAC	204M2002 106MB(10MF/20V)
UP-0422	C058-C059	070932	2	FLC	ECQ-B 1H 682JZ3 0.0068MF
UP-0422	C060-C061	070914	2	FLC	ECQ-B1H472JZ3 50V 0.0047UF
UP-0422	C062-C063	070995	2	FLC	ECQ-B 1H 223JZ3 0.022MF
UP-0422	C064-C065	070923	2	FLC	ECQ-B 1H 562JZ3 0.0056MF
UP-0422	C066-C071	071058	6	FLC	ECQ-V 1H 473JZ3 (0.047MF)
UP-0422	C072-C073	070531	2	TAC	204M2002 106MB(10MF/20V)
UP-0422	C074-C075	071236	2	CEC	TPD55Y5V1H104Z5-W 50V 0.1UF
UP-0422	D050-D053	071548	4	D	1S2076A RE
UP-0422	IC050	020523	1	OPIC	u PC812C yellow low noise
UP-0422	IC051-IC054	015779	4	OPIC	LT1001CN8 LOW DRIFT
UP-0422	IC055-IC056	016083	2	OPIC	UPC4062C
UP-0422	VR050-VR051	164386	2	POT	ET-6S 20KOHM
UP-0422	VR054-VR055	063031	2	VR	GF06S 500OHM
UP-0548	CN001	089895	1	PCN	PCN10EA-20P-2.54DS(05)

UP-0548 TERMISTOR RESP HEAD AMP BOARD

UP-0548	CN002	092035	1	CN	LGY 6501-0101 SMK
UP-0548	CN003	090215	1	PCN	M60-04-30-114P (4P)
UP-0548	C001-C002	070531	2	TAC	204M2002 106MB(10MF/20V)
UP-0548	C003-C004	070718	2	TAC	204M3502 105MB (1MF/35V)
UP-0548	C005	070531	1	TAC	204M2002 106MB(10MF/20V)
UP-0548	C006	071174	1	FLC	ECQ-V 1H 474JZ3 (0.47MF)
UP-0548	C007	071031	1	FLC	ECQ-V 1H 333JZ3 (0.033MF)
UP-0548	C008	043873	1	FLC	DH4M2A-105K 100V 1UF
UP-0548	C009	071094	1	FLC	ECQ-V 1H 104JZ3 (0.1MF)
UP-0548	C010	071031	1	FLC	ECQ-V 1H 333JZ3 (0.033MF)
UP-0548	C011-C012	070959	2	FLC	ECQ-B 1H 103JZ3 0.01MF
UP-0548	D001-D006	071548	6	D	1S2076A RE

9. ELECTRICAL PARTS LIST

ASSY	CKT NO.	PART NO.	QTY	DESCRIPTION	
UP-0548	D007-D008	071539	2	D	1SS104,TPB2
UP-0548	GA001	026811	1	TUBE	Y08-2100B
UP-0548	IC001	072975	1	REG	u PC78L05J-T
UP-0548	IC002	072984	1	REG	u PC79L05J-T
UP-0548	IC003	015993	1	REG	LT1009CZ 2.5VREF
UP-0548	IC004	021718	1	HIC	EHD-HA1270 ISOLATE
UP-0548	IC005	016163	1	OPIC	UPC811C
UP-0548	IC006	016181	1	OPIC	UPC812C
UP-0548	IC007	016083	1	OPIC	UPC4062C
UP-0548	IC008	163289	1	CMOS	MC14053BCP
UP-0548	PC001	002739	1	PTR	PC810A
UP-0548	Q001-Q002	072066	2	TR	2SC1213AKDTZ
UP-0548	T001	036925	1	TF	T3772365 EP10PS transformer
UP-0548	T002	036916	1	TF	T3772356 EP10IS transformer
UP-0548	VR001	062807	1	VR	GF06P 10 KOHM

UP-0563 COM3 BOARD

UP-0563	CN101	089957	1	PCN	PCN10EA-90P-2.54DS(05)
UP-0563	CN102	089912	1	PCN	PCN10EA-32P-2.54DS(05)
UP-0563	CN103	081092	1	CN	RDCD-37SE-LNA F343
UP-0563	CN104	085934	1	PCN	HIF3BA-40PA-2.54DS
UP-0563	C001-C004	071236	4	CEC	TPD55Y5V1H104Z5-W 50V 0.1UF
UP-0563	C005-C010	070487	6	TAC	ECSZ35HS6R8B 35V 6.8UF
UP-0563	C020-C021	070487	2	TAC	ECSZ35HS6R8B 35V 6.8UF
UP-0563	C022	071236	1	CEC	TPD55Y5V1H104Z5-W 50V 0.1UF
UP-0563	C023-C024	070487	2	TAC	ECSZ35HS6R8B 35V 6.8UF
UP-0563	C025-C047	071236	23	CEC	TPD55Y5V1H104Z5-W 50V 0.1UF
UP-0563	C048	070487	1	TAC	ECSZ35HS6R8B 35V 6.8UF
UP-0563	C048-C051	071236	4	CEC	TPD55Y5V1H104Z5-W 50V 0.1UF
UP-0563	C052	070487	1	TAC	ECSZ35HS6R8B 35V 6.8UF
UP-0563	C053-C066	071236	14	CEC	TPD55Y5V1H104Z5-W 50V 0.1UF
UP-0563	C067-C068	070487	2	TAC	ECSZ35HS6R8B 35V 6.8UF
UP-0563	C101-C102	071245	2	CEC	DD05-989SL100D500 500V 10PF
UP-0563	C103	071343	1	CEC	DD05-989B471K500 500V 470PF
UP-0563	C104-C105	071236	2	CEC	TPD55Y5V1H104Z5-W 50V 0.1UF
UP-0563	C106	071076	1	FLC	ECQ-V 1H 683JZ3 (0.068MF)
UP-0563	C107	071094	1	FLC	ECQ-V 1H 104JZ3 (0.1MF)
UP-0563	C108-C111	071236	4	CEC	TPD55Y5V1H104Z5-W 50V 0.1UF
UP-0563	C112	070959	1	FLC	ECQ-B 1H 103JZ3 0.01MF
UP-0563	C113	071236	1	CEC	TPD55Y5V1H104Z5-W 50V 0.1UF
UP-0563	C115	071236	1	CEC	TPD55Y5V1H104Z5-W 50V 0.1UF
UP-0563	C116-C117	070487	2	TAC	ECSZ35HS6R8B 35V 6.8UF
UP-0563	C118	070879	1	FLC	ECQ-B1H222JZ3 50V 0.0022UF
UP-0563	C119	070487	1	TAC	ECSZ35HS6R8B 35V 6.8UF
UP-0563	C120	070834	1	FLC	ECQ-B 1H 102JZ3 0.001MF
UP-0563	C121	070487	1	TAC	ECSZ35HS6R8B 35V 6.8UF
UP-0563	D001-D002	071503	2	D	1S2076ATE
UP-0563	D101	071503	1	D	1S2076ATE
UP-0563	D901-D925	071512	25	D	1SS237(1)-T1
UP-0563	IC101-IC103	019463	3	CMOS	UPD74HCT240C
UP-0563	IC104	019472	1	CMOS	UPD74HCT244C
UP-0563	IC105-IC106	019525	2	CMOS	UPD74HCT640C
UP-0563	IC107-IC111	162771	5	CMOS	HD74HC138P
UP-0563	IC112	163823	1	ADIC	u PD74HC32C
UP-0563	IC113	018758	1	CMOS	UPD74HC30C
UP-0563	IC114	010953	1	TTL	74F04PC
UP-0563	IC115	011881	1	TTL	74F20PC
UP-0563	IC116	011007	1	TTL	74F164PC
UP-0563	IC117	011881	1	TTL	74F20PC
UP-0563	IC118	011319	1	TTL	74F10PC
UP-0563	IC120	008992	1	TTL	SN74LS74AN
UP-0563	IC121	008608	1	TTL	SN74LS04N
UP-0563	IC122	008902	1	TTL	SN74LS38
UP-0563	IC124	008653	1	TTL	SN74LS27N
UP-0563	IC125	008769	1	TTL	SN74LS08N
UP-0563	IC126	367416	1	CPU	MS62256CLL-10PC
UP-0563	IC127-IC130	008698	4	TTL	SN74LS157N
UP-0563	IC131-IC132	010142	2	TTL	SN74LS245N
UP-0563	IC133	018464	1	CPU	u PD8085AHC(AC,AC-2)
UP-0563	IC134	009901	1	TTL	SN74LS373
UP-0563	IC135	009884	1	TTL	SN74LS367AN
UP-0563	IC136	008608	1	TTL	SN74LS04N
UP-0563	IC137	008876	1	TTL	SN74LS32N
UP-0563	IC138	009251	1	TTL	SN74LS139AN
UP-0563	IC139	008876	1	TTL	SN74LS32N
UP-0563	IC140	009251	1	TTL	SN74LS139AN
UP-0563	IC141	011195	1	CPU	HN27C256G20 uPD27C256AD20
UP-0563	IC142	367416	1	CPU	MS62256CLL-10PC
UP-0563	IC143	018615	1	CPU	u PD8251AFC-D USART
UP-0563	IC144	008992	1	TTL	SN74LS74AN

ASSY	CKT NO.	PART NO.	QTY	DESCRIPTION	
UP-0563	IC145	008698	1	TTL	SN74LS157N
UP-0563	IC146	009697	1	TTL	SN74LS273
UP-0563	IC147	008992	1	TTL	SN74LS74AN
UP-0563	IC148	008769	1	TTL	SN74LS08N
UP-0563	IC149-IC150	008876	2	TTL	SN74LS32N
UP-0563	IC151	008591	1	TTL	SN74LS02N
UP-0563	IC152	008813	1	TTL	SN74LS14N
UP-0563	IC153	015529	1	CMOS	AM26LS33PC QUAD L.REC.AMD
UP-0563	IC154	012461	1	TTL	SN75174N LINE DRIVER
UP-0563	IC155	007832	1	TTL	SN7406N
UP-0563	IC156	016092	1	ADIC	HA-17012PB 12BIT DA
UP-0563	IC157-IC158	009697	2	TTL	SN74LS273
UP-0563	IC160	009251	1	TTL	SN74LS139AN
UP-0563	IC161	015993	1	REG	LT1009CZ 2.5VREF F418
UP-0563	IC162-IC163	016163	2	OPIC	UPC811C
UP-0563	IC164	009697	1	TTL	SN74LS273
UP-0563	IC165	010062	1	TTL	SN74LS244N
UP-0563	IC166	009991	1	TTL	SN74LS390N
UP-0563	IC167	009376	1	TTL	SN74LS163
UP-0563	IC168	162887	1	CMOS	HD74HC4040P
UP-0563	IC169-IC170	009189	2	TTL	SN74LS123N
UP-0563	IC171	009224	1	TTL	SN74LS132
UP-0563	IC172	072948	1	REG	u PC79L15J-T
UP-0563	IC173	072957	1	REG	u PC78L15J-T
UP-0563	IC176-IC179	367416	4	CPU	MS62256CLL-10PC
UP-0563	IC180	012969	1	RAM	MB8421-12LP
UP-0563	IC181	009919	1	TTL	SN74LS374N
UP-0563	IC182-IC184	010062	3	TTL	SN74LS244N
UP-0563	IC185	010846	1	TTL	SN74LS641
UP-0563	IC186	008608	1	TTL	SN74LS04N
UP-0563	IC187	008902	1	TTL	SN74LS38
UP-0563	LED101-LED109	342497	9	LED	GL3AR8 red
UP-0563	Q101	072066	1	TR	2SC1213AKDTZ
UP-0563	RA101-RA105	072387	5	RM	EXB-F9 E 104JYV
UP-0563	RA106	072369	1	RM	EXB-F9 E 472JYV
UP-0563	RA107	072387	1	RM	EXB-F9 E 104JYV
UP-0563	RA108	072369	1	RM	EXB-F9 E 472JYV
UP-0563	RA109	072173	1	RM	EXB-F5 E 472JYV
UP-0563	RA110	072369	1	RM	EXB-F9 E 472JYV
UP-0563	RA111	072173	1	RM	EXB-F5 E 472JYV
UP-0563	RA112	072369	1	RM	EXB-F9 E 472JYV
UP-0563	RA113	072173	1	RM	EXB-F5 E 472JYV
UP-0563	RA114	072324	1	RM	EXB-F9 E 102JYV
UP-0563	RA901-RA906	072592	6	RM	EXB-F8 V 471JYV
UP-0563	RA907-RA909	072333	3	RM	EXB-F9 E 152JYV
UP-0563	SK133	356606	1	CN	AXS204011(u -IC socket 40pin)
UP-0563	SK141	356598	1	CN	AXS202811(u -IC socket 28pin)
UP-0563	SK174-SK175	356598	2	CN	AXS202811(u -IC socket 28pin)
UP-0563	SW101	030673	1	DSW	B-8A-T
UP-0563	SW102	031039	1	DSW	B-4A-T
UP-0563	SW103	032484	1	SW	SKHCAD (KHC-10904)
UP-0563	VR102-VR103	072672	2	POT	GF06UT2 100 OHM
UP-0563	VR104	072734	1	POT	GF06UT2 10 KOHM
UP-0563	X101	023235	1	XTAL	NC-18C 6.144MHZ

UP-0571 MOTOR BOARD

UP-0571		140278	1	ETC	infrared filter 4.3u
UP-0571		140287	1	ETC	infrared filter 3.7u
UP-0571	C101	042624	1	TAC	ECSZ20MA4R7
UP-0571	C102-C103	047174	2	CEC	ECBA1E104ZF
UP-0571	C104	042633	1	TAC	ECSZ6MA10
UP-0571	C105	047183	1	CEC	ECBA1H221KB5
UP-0571	IC101	016644	1	OPIC	u PC822G2
UP-0571	M101	075366	1	MOTR	1616T012S-72 DC motor mini motor
UP-0571	P101	004675	1	D	PBSE P791-09
UP-0571	VR101	062469	1	POT	ST-4B 500KOHM

UP-0588 MAIN BOARD

UP-0588	CN001	089895	1	PCN	PCN10EA-20P-2.54DS(05)
UP-0588	CN002	089342	1	PCN	HKP-14FDS2-7,8,9T
UP-0588	C001-C002	070531	2	TAC	204M2002 106MB(10MF/20V)
UP-0588	C003-C007	071236	5	CEC	TPD55Y5V1H104Z5-W 50V 0.1UF
UP-0588	C008	070718	1	TAC	204M3502 105MB (1MF/35V)
UP-0588	C009	071236	1	CEC	TPD55Y5V1H104Z5-W 50V 0.1UF
UP-0588	C010-C011	070959	2	FLC	ECQ-B 1H 103JZ3 0.01MF
UP-0588	C012	070834	1	FLC	ECQ-B 1H 102JZ3 0.001MF

9. ELECTRICAL PARTS LIST

ASSY	CKT NO.	PART NO.	QTY	DESCRIPTION	
UP-0588	C013	071094	1	FLC	ECQ-V 1H 104JZ3 (0.1MF)
UP-0588	C014	070718	1	TAC	204M3502 105MB (1MF/35V)
UP-0588	D001-D004	071548	4	D	1S2076A RE
UP-0588	IC001	163128	1	ADIC	MC14094BCP
UP-0588	IC002	014495	1	ADIC	u F448PC624C
UP-0588	IC003	017973	1	CMOS	HD14538BP
UP-0588	IC004-IC005	017091	2	CMOS	HD14040BP (MC14040BCP)
UP-0588	IC006	015993	1	REG	LT1009CZ 2.5VREF
UP-0588	IC007	016181	1	OPIC	UPC812C
UP-0588	IC008-IC010	016083	3	OPIC	UPC4062C
UP-0588	PC001	002739	1	PTR	PC810A
UP-0588	Q001	071904	1	TR	2SA836 C or D TZ
UP-0588	T001	038068	1	TF	DC-DC converter DC-3826 transformer
UP-0588	VR001	164368	1	POT	ET-6S 5KOHM

UP-0589 SUB BOARD

UP-0589	CN050	089235	1	PCN	HKP-14M5S-7,8,9T
UP-0589	C050-C052	071236	3	CEC	TPD55Y5V1H104Z5-W 50V 0.1UF
UP-0589	C053	071174	1	FLC	ECQ-V 1H 474JZ3 (0.47MF)
UP-0589	C054	070834	1	FLC	ECQ-B 1H 102JZ3 0.001MF
UP-0589	C055-C056	071094	2	FLC	ECQ-V 1H 104JZ3 (0.1MF)
UP-0589	C057	070959	1	FLC	ECQ-B 1H 103JZ3 0.01MF
UP-0589	C058	070914	1	FLC	ECQ-B1H472JZ3 50V 0.0047UF
UP-0589	C059-C063	071094	5	FLC	ECQ-V 1H 104JZ3 (0.1MF)
UP-0589	C064	070718	1	TAC	204M3502 105MB (1MF/35V)
UP-0589	C065	071343	1	CEC	DD05-989B471K500 500V 470PF
UP-0589	D050	071548	1	D	1S2076A RE
UP-0589	D051	071539	1	D	1SS104,TPB2
UP-0589	D052	071548	1	D	1S2076A RE
UP-0589	IC050-IC051	016083	2	OPIC	UPC4062C
UP-0589	IC052	017973	1	CMOS	HD14538BP
UP-0589	IC053	016822	1	CMOS	MC14013BCP
UP-0589	IC054	163066	1	CMOS	MC14001BCP
UP-0589	IC055	163289	1	CMOS	MC14053BCP
UP-0589	IC056	017322	1	CMOS	HD-14066BP
UP-0589	IC057	163262	1	CMOS	MC14051BCP
UP-0589	IC058-IC061	016181	4	OPIC	UPC812C
UP-0589	IC062	010739	1	OPIC	HA17903PS
UP-0589	IC063	016083	1	OPIC	UPC4062C

UP-0592 O_2 HEAD AMP BOARD

UP-0592	CN001	089895	1	PCN	PCN10EA-20P-2.54DS(05)
UP-0592	CN002	079504	1	CN	HR16-13R-5S(04) green
UP-0592	CN003	090215	1	PCN	M60-04-30-114P (4P)
UP-0592	C001-C002	070531	2	TAC	204M2002 106MB(10MF/20V)
UP-0592	C003	071236	1	CEC	TPD55Y5V1H104Z5-W 50V 0.1UF
UP-0592	C004	070718	1	TAC	204M3502 105MB (1MF/35V)
UP-0592	C005	070959	1	FLC	ECQ-B 1H 103JZ3 0.01MF
UP-0592	C006	071236	1	CEC	TPD55Y5V1H104Z5-W 50V 0.1UF
UP-0592	C007	070959	1	FLC	ECQ-B 1H 103JZ3 0.01MF
UP-0592	C008	071236	1	CEC	TPD55Y5V1H104Z5-W 50V 0.1UF
UP-0592	C009	071343	1	CEC	DD05-989B471K500 500V 470PF
UP-0592	C010-C011	070959	2	FLC	ECQ-B 1H 103JZ3 0.01MF
UP-0592	D001-D006	071548	6	D	1S2076A RE
UP-0592	D007-D012	071539	6	D	1SS104,TPB2
UP-0592	GA001	026811	1	TUBE	Y08-2100B
UP-0592	IC001	072975	1	REG	u PC78L05J-T
UP-0592	IC002	072984	1	REG	u PC79L05J-T
UP-0592	IC003	163289	1	CMOS	MC14053BCP
UP-0592	IC004	021718	1	HIC	EHD-HA1270 ISOLATE
UP-0592	IC005	015993	1	REG	LT1009CZ 2.5VREF
UP-0592	IC006	017091	1	CMOS	HD14040BP (MC14040BCP)
UP-0592	IC007	163262	1	CMOS	MC14051BCP
UP-0592	IC008	016181	1	OPIC	UPC812C
UP-0592	IC009-IC010	016698	2	OPIC	LT1012CN8
UP-0592	PC001-PC002	002739	2	PTR	PC810A
UP-0592	Q001-Q002	072066	2	TR	2SC1213AKDTZ
UP-0592	T001	036925	1	TF	T3772365 EP10PS transformer
UP-0592	T002	036916	1	TF	T3772356 EP10IS transformer
UP-0592	VR001-VR002	062799	2	VR	GF06P 5 KOHM

ASSY	CKT NO.	PART NO.	QTY	DESCRIPTION	
UP-0629	**MAIN BOARD**				
UP-0629	CNJ102	090215	1	PCN	M60-04-30-114P (4P)
UP-0629	CNJ103	339884	1	PCN	M60-09-30-114P
UP-0629	CN101	089895	1	PCN	PCN10EA-20P-2.54DS(05)
UP-0629	CN104	092302	1	PCN	FSN-21.5A-9 flexible jumper
UP-0629	C101	159695	1	TAC	267M3502 106MR720 10MF35V
UP-0629	C102	368905	1	CEC	ECU V1H 104ZFX
UP-0629	C103	331107	1	FLC	ECW-U1H223JA5 50V 0.022UF
UP-0629	C104	161513	1	CEC	C4532X7R1H 334KT 0.33MF
UP-0629	C105	159695	1	TAC	267M3502 106MR720 10MF35V
UP-0629	C106	159775	1	CEC	GRM39SL 221K50PT 220PF50V
UP-0629	C107-C108	161513	2	CEC	C4532X7R1H 334KT 0.33MF
UP-0629	C109	331107	1	FLC	ECW-U1H223JA5 50V 0.022UF
UP-0629	C110	159695	1	TAC	267M3502 106MR720 10MF35V
UP-0629	C111	040591	1	EC	ECEAICGE471 470MF 16V
UP-0629	C112-C118	368905	7	CEC	ECU V1H 104ZFX
UP-0629	C119	159775	1	CEC	GRM39SL 221K50PT 220PF50V
UP-0629	C120	040591	1	EC	ECEAICGE471 470MF 16V
UP-0629	D101-D109	160078	9	D	HSK120TR
UP-0629	IC101-IC103	160309	3	ADIC	HA17903FP
UP-0629	IC104	160523	1	CMOS	MC14040BF
UP-0629	IC105	161558	1	CMOS	MC14094BF
UP-0629	IC106	160595	1	CMOS	MC14066BF
UP-0629	IC107	160817	1	CMOS	MC14538BF
UP-0629	IC108	160595	1	CMOS	MC14066BF
UP-0629	IC109	160523	1	CMOS	MC14040BF
UP-0629	IC110	160505	1	CMOS	MC14027BF
UP-0629	IC111-IC113	160452	3	CMOS	MC14011BF
UP-0629	IC114	160844	1	CMOS	MC14584BF
UP-0629	IC115	160603	1	CMOS	MC14068BF
UP-0629	IC116	160817	1	CMOS	MC14538BF
UP-0629	IC117	160497	1	CMOS	MC14025BF
UP-0629	Q101	161487	1	TR	2SC4181-T2
UP-0629	Q102	160149	1	TR	2SC2618 D TR
UP-0629	Q103-Q107	161496	5	TR	2SD1950-T1
UP-0629	Q108	160149	1	TR	2SC2618 D TR
UP-0629	RY101	033073	1	RY	G6A-274P 6V mini relay
UP-0630	**SUB BOARD**				
UP-0630	C201	368905	1	CEC	ECU V1H 104ZFX
UP-0630	C202	159695	1	TAC	267M3502 106MR720 10MF35V
UP-0630	C203-C204	331134	2	FLC	ECW-U1H103JA5 50V 0.01UF
UP-0630	C205	341471	1	FLC	ECW-U1H473JA5 50V 0.047UF
UP-0630	C206	357801	1	FLC	ECW-U1H104JB9 50V 0.1UF
UP-0630	C207	161513	1	CEC	C4532X7R1H 334KT 0.33MF
UP-0630	C208	331134	1	FLC	ECW-U1H103JA5 50V 0.01UF
UP-0630	C209	161513	1	CEC	C4532X7R1H 334KT 0.33MF
UP-0630	C210	331134	1	FLC	ECW-U1H103JA5 50V 0.01UF
UP-0630	C211-C212	368905	2	CEC	ECU V1H 104ZFX
UP-0630	C213	159775	1	CEC	GRM39SL 221K50PT 220PF50V
UP-0630	IC201	160407	1	REG	LT1009S8
UP-0630	IC202-IC204	160202	3	OPIC	LT1001CS8
UP-0630	IC205-IC206	160274A	2	OPIC	u PC4062G2-E2
UP-0630	IC207	160595	1	CMOS	MC14066BF
UP-0630	IC208	160568	1	CMOS	MC14051BF
UP-0630	IC209	160256	1	OPIC	u PC811G2
UP-0630	T201	366738	1	TD	FPM-07PG-NK1(red)
UP-0630	VR201	159828	1	POT	G4AT 200 OHM
UP-0630	VR202	161567	1	POT	ST-5TP 1 KOHM
UP-0643	**NIBP UNIT BOARD**				
UP-0643	DCC501	038077	1	TF	EX-7202B DC/DC converter

9. ELECTRICAL PARTS LIST

ASSY	CKT NO.	PART NO.	QTY	DESCRIPTION
UP-0670	**DPU BOARD (without ROM)**			
UP-0670		092614	2	CN RDBD
UP-0670	CN101	089957	1	PCN PCN10EA-90P-2.54DS(05)
UP-0670	CN102	089912	1	PCN PCN10EA-32P-2.54DS(05)
UP-0670	CN103	081092	1	CN RDCD-37SE-LNA
UP-0670	CN104	084356	1	PCN DF11-16DP-2DS receptacle male
UP-0670	C001-C010	070487	10	TAC ECSZ35HS6R8B 35V 6.8UF
UP-0670	C021-C022	070959	2	FLC ECQ-B 1H 103JZ3 0.01MF
UP-0670	C031-C050	368905	20	CEC ECU V1H 104ZFX
UP-0670	C052-C075	368905	24	CEC ECU V1H 104ZFX
UP-0670	C201	159668	1	TAC 267M3502 225MR533 2.2MF35
UP-0670	C202	368905	1	CEC ECU V1H 104ZFX
UP-0670	C701-C702	070834	2	FLC ECQ-B 1H 102JZ3 0.001MF
UP-0670	C703	071094	1	FLC ECQ-V 1H 104JZ3 (0.1MF)
UP-0670	C704-C715	070959	12	FLC ECQ-B 1H 103JZ3 0.01MF
UP-0670	C716-C719	368905	4	CEC ECU V1H 104ZFX
UP-0670	C721-C724	070959	4	FLC ECQ-B 1H 103JZ3 0.01MF
UP-0670	C731	159784	1	CEC GRM39SL 331K50PT 330PF50V
UP-0670	C732	368905	1	CEC ECU V1H 104ZFX
UP-0670	C733	043543	1	FLC ECQP1H102JZ 1000PF
UP-0670	C734-C737	368905	4	CEC ECU V1H 104ZFX
UP-0670	C801-C802	368905	2	CEC ECU V1H 104ZFX
UP-0670	C803	159748	1	CEC GRM39SL 470K50PT 50V 47PF
UP-0670	C804	071138	1	FLC ECQ-V 1H 224JZ3 (0.22MF)
UP-0670	C812	070959	1	FLC ECQ-B 1H 103JZ3 0.01MF
UP-0670	C813-C816	070977	4	FLC ECQ-B 1H 153JZ3 0.015MF
UP-0670	C817	070959	1	FLC ECQ-B 1H 103JZ3 0.01MF
UP-0670	C818-C819	070977	2	FLC ECQ-B 1H 153JZ3 0.015MF
UP-0670	C822	070879	1	FLC ECQ-B1H222JZ3 50V 0.0022UF
UP-0670	C823-C826	070923	4	FLC ECQ-B 1H 562JZ3 0.0056MF
UP-0670	C827	070879	1	FLC ECQ-B1H222JZ3 50V 0.0022UF
UP-0670	C828-C829	070923	2	FLC ECQ-B 1H 562JZ3 0.0056MF
UP-0670	C831-C832	071138	2	FLC ECQ-V 1H 224JZ3 (0.22MF)
UP-0670	C833	071058	1	FLC ECQ-V 1H 473JZ3 (0.047MF)
UP-0670	C834-C837	071138	4	FLC ECQ-V 1H 224JZ3 (0.22MF)
UP-0670	C838	071058	1	FLC ECQ-V 1H 473JZ3 (0.047MF)
UP-0670	C901	070879	1	FLC ECQ-B1H222JZ3 50V 0.0022UF
UP-0670	C902-C905	159632	4	TAC 267M2002 106MR533 10MF20V
UP-0670	C906	071174	1	FLC ECQ-V 1H 474JZ3 (0.47MF)
UP-0670	C907	070834	1	FLC ECQ-B 1H 102JZ3 0.001MF
UP-0670	C908-C910	071058	3	FLC ECQ-V 1H 473JZ3 (0.047MF)
UP-0670	C911	070977	1	FLC ECQ-B 1H 153JZ3 0.015MF
UP-0670	C912	070923	1	FLC ECQ-B 1H 562JZ3 0.0056MF
UP-0670	C913	071094	1	FLC ECQ-V 1H 104JZ3 (0.1MF)
UP-0670	C914	070834	1	FLC ECQ-B 1H 102JZ3 0.001MF
UP-0670	C915-C917	071058	3	FLC ECQ-V 1H 473JZ3 (0.047MF)
UP-0670	C918	070977	1	FLC ECQ-B 1H 153JZ3 0.015MF
UP-0670	C919	070923	1	FLC ECQ-B 1H 562JZ3 0.0056MF
UP-0670	C920	071094	1	FLC ECQ-V 1H 104JZ3 (0.1MF)
UP-0670	C921	070879	1	FLC ECQ-B1H222JZ3 50V 0.0022UF
UP-0670	C922-C925	159632	4	TAC 267M2002 106MR533 10MF20V
UP-0670	C926	071174	1	FLC ECQ-V 1H 474JZ3 (0.47MF)
UP-0670	C927	071094	1	FLC ECQ-V 1H 104JZ3 (0.1MF)
UP-0670	C928-C929	159632	2	TAC 267M2002 106MR533 10MF20V
UP-0670	C930	071094	1	FLC ECQ-V 1H 104JZ3 (0.1MF)
UP-0670	DA921	003613	1	D DAN401
UP-0670	DA922	003604	1	D DAP401
UP-0670	D001-D002	071548	2	D 1S2076A RE
UP-0670	D201	071548	1	D 1S2076A RE
UP-0670	D711-D714	071539	4	D 1SS104,TPB2
UP-0670	D901-D902	071557	2	D 1SS106RE schottky
UP-0670	D903-D904	071539	2	D 1SS104,TPB2
UP-0670	D905-D906	071557	2	D 1SS106RE schottky
UP-0670	D907-D908	071539	2	D 1SS104,TPB2
UP-0670	IC101	013941	1	CPU TMP68HC000N-16
UP-0670	IC102	013718	1	CPU HN27C1024HG-85 1MBIT(X16)
UP-0670	IC103-IC104	448089	2	RAM HM62256BLFP-8TZ
UP-0670	IC105	161317	1	TTL 74F04SJ
UP-0670	IC106	161326	1	TTL 74F32SJ
UP-0670	IC111-IC112	161353	2	TTL 74F138SJ
UP-0670	IC113	161772	1	CMOS HD74HCT138FP
UP-0670	IC114	161371	1	TTL SN74LS09NS
UP-0670	IC116	161433	1	TTL SN74LS01 NS
UP-0670	IC117	161398	1	TTL 74F74SJ
UP-0670	IC118	161353	1	TTL 74F138SJ
UP-0670	IC131	161638	1	TTL 74F00SJ
UP-0670	IC132	323018	1	TTL SN74LS11NS

ASSY	CKT NO.	PART NO.	QTY	DESCRIPTION	
UP-0670	IC133	161736	1	TTL	74F27SJ
UP-0670	IC134	161326	1	TTL	74F32SJ
UP-0670	IC135-IC136	161406	2	TTL	74F08SJ
UP-0670	IC201	161317	1	TTL	74F04SJ
UP-0670	IC202-IC204	161736	3	TTL	74F27SJ
UP-0670	IC205	161406	1	TTL	74F08SJ
UP-0670	IC206	161389	1	TTL	74F164SJ
UP-0670	IC207	161629	1	TTL	74F158SJ
UP-0670	IC208	161389	1	TTL	74F164SJ
UP-0670	IC209	161638	1	TTL	74F00SJ
UP-0670	IC210	161398	1	TTL	74F74SJ
UP-0670	IC221-IC222	161647	2	CMOS	HD74HCT244FP
UP-0670	IC223-IC224	161415	2	CMOS	HD74HCT240FP
UP-0670	IC225-IC226	161745	2	CPU	HM6264ALFP-15
UP-0670	IC227-IC228	161656	2	TTL	SN74LS245NS
UP-0670	IC229-IC230	161665	2	TTL	SN74LS640NS
UP-0670	IC301	161772	1	CMOS	HD74HCT138FP
UP-0670	IC302	160889	1	CMOS	HD74HC08FP
UP-0670	IC303	160978	1	CMOS	HD74HC74FP
UP-0670	IC304	161273	1	CMOS	HD74HC148FP
UP-0670	IC305	160898	1	CMOS	HD74HC10FP
UP-0670	IC401	161398	1	TTL	74F74SJ
UP-0670	IC402	161674	1	TTL	SN74LS393NS
UP-0670	IC403-IC404	161683	2	TTL	SN74LS390NS
UP-0670	IC405	160871	1	CMOS	HD74HC04FP
UP-0670	IC406	161264	1	CMOS	HD74HC4040FP
UP-0670	IC407	160978	1	CMOS	HD74HC74FP
UP-0670	IC409	160862	1	CMOS	HD74HC02FP
UP-0670	IC410	160853	1	CMOS	HD74HC00FP
UP-0670	IC421	161095	1	CMOS	HD74HC164FP
UP-0670	IC422-IC423	160978	2	CMOS	HD74HC74FP
UP-0670	IC424	160871	1	CMOS	HD74HC04FP
UP-0670	IC425	160889	1	CMOS	HD74HC08FP
UP-0670	IC426	160951	1	CMOS	HD74HC32FP
UP-0670	IC428	161282	1	CMOS	MC14504BF
UP-0670	IC429	160978	1	CMOS	HD74HC74FP
UP-0670	IC430	160951	1	CMOS	HD74HC32FP
UP-0670	IC501	160862	1	CMOS	HD74HC02FP
UP-0670	IC502-IC505	161291	4	CMOS	u PD74HC4094GS
UP-0670	IC507-IC510	161754	4	CMOS	HD74HC597FP
UP-0670	IC601-IC602	161647	2	CMOS	HD74HCT244FP
UP-0670	IC603-IC605	161219	3	CMOS	HD74HC374FP
UP-0670	IC606	161442	1	CPU	FRAMSYNC1208631
UP-0670	IC607	160951	1	CMOS	HD74HC32FP
UP-0670	IC608	161371	1	TTL	SN74LS09NS
UP-0670	IC609	161647	1	CMOS	HD74HCT244FP
UP-0670	IC701-IC704	323099	4	OPIC	u PC458G2
UP-0670	IC705-IC706	161763	2	CMOS	JLC1133F (MC14051 inspected)
UP-0670	IC711-IC715	160265	5	OPIC	u PC812G2
UP-0670	IC716-IC717	161763	2	CMOS	JLC1133F (MC14051 inspected)
UP-0670	IC721	160265	1	OPIC	u PC812G2
UP-0670	IC722	160407	1	REG	LT1009S8
UP-0670	IC723	161763	1	CMOS	JLC1133F (MC14051 inspected)
UP-0670	IC724	015886	1	IC	UPC-649C (sample hold)
UP-0670	IC725	016653	1	ADIC	ADC574AJH 12BITADC BB
UP-0670	IC726	323152	1	RAM	MB8421-90LPFQ-G 2port RAM
UP-0670	IC801-IC802	161219	2	CMOS	HD74HC374FP
UP-0670	IC803	016092	1	ADIC	HA-17012PB 12BIT DA
UP-0670	IC804	160265	1	OPIC	u PC812G2
UP-0670	IC805	161282	1	CMOS	MC14504BF
UP-0670	IC806	161763	1	CMOS	JLC1133F (MC14051 inspected)
UP-0670	IC807-IC810	160265	4	OPIC	u PC812G2
UP-0670	IC811	161291	1	CMOS	u PD74HC4094GS
UP-0670	IC812-IC813	160265	2	OPIC	u PC812G2
UP-0670	IC814	160586	1	CMOS	MC14053BF
UP-0670	IC815	160265	1	OPIC	u PC812G2
UP-0670	IC901	160586	1	CMOS	MC14053BF
UP-0670	IC902-IC903	160265	2	OPIC	u PC812G2
UP-0670	IC904-IC905	160586	2	CMOS	MC14053BF
UP-0670	IC906-IC907	160256	2	OPIC	u PC811G2
UP-0670	IC908-IC909	160265	2	OPIC	u PC812G2
UP-0670	IC910	160586	1	CMOS	MC14053BF
UP-0670	IC911	160265	1	OPIC	u PC812G2
UP-0670	IC912	010071	1	TR	TD62004P
UP-0670	IC913	160265	1	OPIC	u PC812G2
UP-0670	IC921	161193	1	CMOS	HD74HC367FP
UP-0670	IC922	160354	1	REG	HA178L15UATR
UP-0670	IC923	160399A	1	REG	HA179L15UTR
UP-0670	LED601-LED608	342497	8	LED	GL3AR8 red
UP-0670	L101	316882	1	NFLT	ferrite beads BL02RN2-R62
UP-0670	SKT102	356606	1	CN	AXS204011(u -IC socket 40pin)
UP-0670	SW101	032484	1	SW	SKHCAD (KHC-10904)
UP-0670	SW601	031039	1	DSW	B-4A-T

ASSY	CKT NO.	PART NO.	QTY	DESCRIPTION	
UP-0670	SW602	317319	1	SW	ATE1D-6M3-10
UP-0670	VR101	159873	1	POT	G4AT F76010 KOHM
UP-0670	VR102	159846	1	POT	G4AT 1 KOHM
UP-0670	VR103	159828	1	POT	G4AT 200 OHM
UP-0670	VR104-VR105	159819	2	POT	G4AT 100 OHM
UP-0670	VR106-VR107	159873	2	POT	G4AT 10 KOHM
UP-0670	VR108-VR109	159882	2	POT	G4AT 20 KOHM
UP-0670	VR110	159837	1	POT	G4AT 500 OHM
UP-0670	X101	024297	1	XTAL	TD308C 32MHZ CRISTAL

UP-0795 CRTC (CRT CONTROL) BOARD

UP-0795	CN101	089957	1	PCN	PCN10EA-90P-2.54DS(05)
UP-0795	CN102	354359	1	CN	DX10M-26SE
UP-0795	CN103	081118	1	CN	RDAD-15SE-LNA
UP-0795	CN104	089912	1	PCN	PCN10EA-32P-2.54DS(05)
UP-0795	C001-C004	159641	4	TAC	267M2002 226MR533 22MF20V
UP-0795	C005-C107	368905	103	CEC	ECU V1H 104ZFX
UP-0795	C201-C202	159659	2	TAC	267M3502 105MR 1MF35V
UP-0795	C701-C702	368905	2	CEC	ECU V1H 104ZFX
UP-0795	C703-C704	159632	2	TAC	267M2002 106MR533 10MF20V
UP-0795	C705	368905	1	CEC	ECU V1H 104ZFX
UP-0795	C706	159632	1	TAC	267M2002 106MR533 10MF20V
UP-0795	D703	160078	1	D	HSK120TR
UP-0795	FIL601	367381	1	NFLT	NFM61R30T472T1
UP-0795	FIL700-FIL702	367381	3	NFLT	NFM61R30T472T1
UP-0795	FIL703-FIL713	334149	11	NFLT	NFM52R20P506
UP-0795	FIL720	367381	1	NFLT	NFM61R30T472T1
UP-0795	FIL721-FIL736	341489	16	NFLT	BLM21A05PT
UP-0795	IC101-IC102	334096	2	CMOS	TD74BC640F
UP-0795	IC103-IC104	334087	2	CMOS	TD74BC240F
UP-0795	IC105-IC106	357445	2	CMOS	TC74AC175F
UP-0795	IC107	357409	1	CMOS	74ACT138SJ
UP-0795	IC109	334042	1	CMOS	HD74AC125FP
UP-0795	IC110	333836	1	CMOS	74AC04SJ
UP-0795	IC201	333916	1	CRTC	HD63484CP98
UP-0795	IC202-IC203	149937A	2	CMOS	74AC373SJ(CD74AC373M) SOP
UP-0795	IC206-IC207	149901A	2	CMOS	74AC74SJ(CD74AC74M) (SOP)
UP-0795	IC208	333836	1	CMOS	74AC04SJ
UP-0795	IC209, 211, 213, 215	334158A	4	RAM	TC528257J-80
UP-0795	IC217	357418	1	CMOS	HD74AC164FP
UP-0795	IC301-IC302	333854	2	CMOS	74AC244SJ
UP-0795	IC303-IC310	448089	8	RAM	HM62256BLFP-8TZ
UP-0795	IC311-IC318	357454	8	CMOS	TC74AC245F
UP-0795	IC319-IC322	013745A	4	CPU	gate array DCW
UP-0795	IC323-IC328	357463	6	CMOS	TC74AC374F
UP-0795	IC333	013754A	1	CPU	gate array ACW
UP-0795	IC334-IC336	357463	3	CMOS	TC74AC374F
UP-0795	IC338	333845	1	CMOS	74AC139SJ
UP-0795	IC339	333854	1	CMOS	74AC244SJ
UP-0795	IC344	149901A	1	CMOS	74AC74SJ(CD74AC74M) (SOP)
UP-0795	IC345	357418	1	CMOS	HD74AC164FP
UP-0795	IC346	149901A	1	CMOS	74AC74SJ(CD74AC74M) (SOP)
UP-0795	IC347	333863	1	CMOS	74AC08SJ
UP-0795	IC348-IC395	333907	48	RAM	HM53461JP-12
UP-0795	IC396-IC407	334069	12	CMOS	TC74AC299F
UP-0795	IC408	333854	1	CMOS	74AC244SJ
UP-0795	IC409	149901A	1	CMOS	74AC74SJ(CD74AC74M) (SOP)
UP-0795	IC502-IC503	333952	2	RAM	MB8441-55 QFP
UP-0795	IC504-IC505	149937A	2	CMOS	74AC373SJ(CD74AC373M) SOP
UP-0795	IC506-IC507	357436	2	CMOS	74AC174SJ
UP-0795	IC508-IC509	161264	2	CMOS	HD74HC4040FP
UP-0795	IC510	161237	1	CMOS	HD74HC390FP
UP-0795	IC514	334015	1	CMOS	HD74AC166FP
UP-0795	IC516	357418	1	CMOS	HD74AC164FP
UP-0795	IC520	161264	1	CMOS	HD74HC4040FP
UP-0795	IC521	357418	1	CMOS	HD74AC164FP
UP-0795	IC601	161317	1	TTL	74F04SJ
UP-0795	IC602	333997	1	TTL	74F163SJ
UP-0795	IC603	333988	1	TTL	74F175SJ
UP-0795	IC604	161398	1	TTL	74F74SJ
UP-0795	IC605	333702	1	CMOS	HD74HC273FP
UP-0795	IC606	161193	1	CMOS	HD74HC367FP
UP-0795	IC701	333925	1	CRTC	ADV471KP66
UP-0795	IC704	161469	1	TTL	SN74LS06 NS
UP-0795	IC705	334078	1	CMOS	TD74BC244F
UP-0795	IC707	160363	1	REG	HA179L05UTR
UP-0795	IC708	334113A	1	REG	LT1004CS8-1.2
UP-0795	Q701-Q707	334122A	7	TR	2SC3735-T2B
UP-0795	SK513	356598	1	CN	AXS202811(u-IC socket 28pin)
UP-0795	VC601	047637	1	VC	TZ03R 300ER 5.2-30PF

ASSY	CKT NO.	PART NO.	QTY	DESCRIPTION	
UP-0795	X601	354368	1	XTAL	1349-M1 64MHZ

UP-0797 I / O BOARD

UP-0797	CN101	089957	1	PCN	PCN10EA-90P-2.54DS(05)
UP-0797	CN102	089912	1	PCN	PCN10EA-32P-2.54DS(05)
UP-0797	CN103	089725	1	PCN	M60-06-30-134P (6P)
UP-0797	CN104	085934	1	PCN	HIF3BA-40PA-2.54DS
UP-0797	CN105	081092	1	CN	RDCD-37SE-LNA
UP-0797	CN106	089672	1	PCN	M60-06-30-114P (6P)
UP-0797	CN201	356767	1	PCN	HIF-6-68PA-1.27DS
UP-0797	CN401	091072	1	PCN	TCS7587-01-401
UP-0797	C101-C104	331134	4	FLC	ECW-U1H103JA5 50V 0.01UF
UP-0797	C105-C106	159632	2	TAC	267M2002 106MR533 10MF20V
UP-0797	C151-C160	368905	10	CEC	ECU V1H 104ZFX
UP-0797	C301-C304	331107	4	FLC	ECW-U1H223JA5 50V 0.022UF
UP-0797	C305	159641	1	TAC	267M2002 226MR533 22MF20V
UP-0797	C306	159632	1	TAC	267M2002 106MR533 10MF20V
UP-0797	C307	159677	1	TAC	267M3502 475MR 4.7MF35V
UP-0797	C308	159748	1	CEC	GRM39SL 470K50PT 50V 47PF
UP-0797	C309	159677	1	TAC	267M3502 475MR 4.7MF35V
UP-0797	C310	159632	1	TAC	267M2002 106MR533 10MF20V
UP-0797	C311-C312	357801	2	FLC	ECW-U1H104JB9 50V 0.1UF
UP-0797	C313	331134	1	FLC	ECW-U1H103JA5 50V 0.01UF
UP-0797	C314-C315	341471	2	FLC	ECW-U1H473JA5 50V 0.047UF
UP-0797	C316-C319	357801	4	FLC	ECW-U1H104JB9 50V 0.1UF
UP-0797	C320-C322	159784	3	CEC	GRM39SL 331K50PT 330PF50V
UP-0797	C323-C324	159739	2	CEC	GRM39SL 330K50PT 50V 33PF
UP-0797	C325	159632	1	TAC	267M2002 106MR533 10MF20V
UP-0797	C401-C408	159695	8	TAC	267M3502 106MR720 10MF35V
UP-0797	C409	159632	1	TAC	267M2002 106MR533 10MF20V
UP-0797	C410-C411	159739	2	CEC	GRM39SL 330K50PT 50V 33PF
UP-0797	C412	159632	1	TAC	267M2002 106MR533 10MF20V
UP-0797	C413	368905	1	CEC	ECU V1H 104ZFX
UP-0797	C414	331134	1	FLC	ECW-U1H103JA5 50V 0.01UF
UP-0797	C415	357801	1	FLC	ECW-U1H104JB9 50V 0.1UF
UP-0797	C416	159659	1	TAC	267M3502 105MR 1MF35V
UP-0797	C417	159632	1	TAC	267M2002 106MR533 10MF20V
UP-0797	C451-C454	368905	4	CEC	ECU V1H 104ZFX
UP-0797	C601-C602	159632	2	TAC	267M2002 106MR533 10MF20V
UP-0797	C603-C642	368905	40	CEC	ECU V1H 104ZFX
UP-0797	D301	160078	1	D	HSK120TR
UP-0797	D302	005389	1	ZD	HZ2C1
UP-0797	D401-D402	160104	2	D	HSM123 TR
UP-0797	D403-D410	357597	8	LED	LT1L51A
UP-0797	D411-D412	160096	2	D	1SS294 TE85R
UP-0797	FIL101-FIL104	323223	4	NFLT	BLA81A01T1
UP-0797	FIL105-FIL107	323232	3	NFLT	NFM61T20T472T1
UP-0797	FIL201-FIL207	323223	7	NFLT	BLA81A01T1
UP-0797	FIL208	323232	1	NFLT	NFM61T20T472T1
UP-0797	FIL401	323223	1	NFLT	BLA81A01T1
UP-0797	FIL402-FIL403	323232	2	NFLT	NFM61T20T472T1
UP-0797	IC101	160256	1	OPIC	u PC811G2
UP-0797	IC102	160238	1	OPIC	u PC1458G2
UP-0797	IC103	160256	1	OPIC	u PC811G2
UP-0797	IC104	161469	1	TTL	SN74LS06
UP-0797	IC201-IC202	161424	2	CMOS	u PD74HCT640GS
UP-0797	IC203-IC205	161415	3	CMOS	HD74HCT240FP
UP-0797	IC206	161023	1	CMOS	HD74HC138FP
UP-0797	IC208	161647	1	CMOS	HD74HCT244FP
UP-0797	IC209-IC210	357507	2	CMOS	HD74HCT245FP
UP-0797	IC211-IC214	161219	4	CMOS	HD74HC374FP
UP-0797	IC301-IC302	323036	2	CMOS	HD74HC 14FP
UP-0797	IC303	160871	1	CMOS	HD74HC04FP
UP-0797	IC304-IC308	161112	5	CMOS	HD74HC174FP
UP-0797	IC309	160853	1	CMOS	HD74HC00FP
UP-0797	IC310	160817	1	CMOS	MC14538BF
UP-0797	IC311	370225	1	CPU	u PD75004GB-777-3B4
UP-0797	IC312	160817	1	CMOS	MC14538BF
UP-0797	IC313	160229A	1	OPIC	u PC358G2-E2
UP-0797	IC314	160586	1	CMOS	MC14053BF
UP-0797	IC315	015431	1	CMOS	melody IC 7910I
UP-0797	IC316	160265	1	OPIC	u PC812G2
UP-0797	IC317	160586	1	CMOS	MC14053BF
UP-0797	IC318	160265	1	OPIC	u PC812G2
UP-0797	IC319	160586	1	CMOS	MC14053BF
UP-0797	IC320	160265	1	OPIC	u PC812G2
UP-0797	IC401	160978	1	CMOS	HD74HC74FP
UP-0797	IC403	161095	1	CMOS	HD74HC164FP
UP-0797	IC404	323205	1	CPU	u PD72001GC-3B6
UP-0797	IC405	161469	1	TTL	SN74LS06 NS

9. ELECTRICAL PARTS LIST

ASSY	CKT NO.	PART NO.	QTY	DESCRIPTION
UP-0797	IC406-IC407	161023	2	CMOS HD74HC138FP
UP-0797	IC408	323205	1	CPU u PD72001GC-3B6
UP-0797	IC409	161647	1	CMOS HD74HCT244FP
UP-0797	IC410-IC411	334202	2	ADIC MAX232CWE-T
UP-0797	IC412	160871	1	CMOS HD74HC04FP
UP-0797	IC413	370225	1	CPU u PD75004GB-777-3B4
UP-0797	IC414	161692	1	ADIC TL7705ACPS
UP-0797	IC415	161219	1	CMOS HD74HC374FP
UP-0797	IC417	161469	1	TTL SN74LS06 NS
UP-0797	IC418	323036	1	CMOS HD74HC 14FP
UP-0797	IC419	161264	1	CMOS HD74HC4040FP
UP-0797	IC420	160978	1	CMOS HD74HC74FP
UP-0797	IC421	160817	1	CMOS MC14538BF
UP-0797	IC422	161219	1	CMOS HD74HC374FP
UP-0797	IC501-IC503	160951	3	CMOS HD74HC32FP
UP-0797	IC504	160889	1	CMOS HD74HC08FP
UP-0797	IC505-IC508	334185	4	CMOS HD74HC595FP
UP-0797	IC511-IC512	161166	2	CMOS HD74HC244FP
UP-0797	Q301	160149	1	TR 2SC2618 D TR
UP-0797	Q302	160122	1	TR 2SA1122 CORD TR
UP-0797	VR101	159873	1	POT G4AT 10 KOHM
UP-0797	VR102	159837	1	POT G4AT 500 OHM
UP-0797	VR103	159873	1	POT G4AT 10 KOHM
UP-0797	VR104	159837	1	POT G4AT 500 OHM
UP-0797	X301	357552	1	XTAL CSAC 4.19MGCM-TC ceramic oscillator
UP-0797	X401	357552	1	XTAL CSAC 4.19MGCM-TC ceramic oscillator

UP-0798 MOTHER BOARD

UP-0798	CN101-CN105	089966	5	PCN PCN10EA-90S-2.54DSA(05)
UP-0798	CN106-CN110	089921	5	PCN PCN10EA-32S-2.54DSA(05)
UP-0798	CN111	268069	1	PCN 171457-1
UP-0798	CN112	090206	1	PCN M60-02-30-114P (2P)
UP-0798	CN113	091232A	1	PCN FFC-20BSM1#02ST
UP-0798	C101-C102	046861	2	C EECF5R5U105 1F/5.5V
UP-0798	D101	160078	1	D HSK120TR
UP-0798	FIL001	341489	1	NFLT BLM21A05PT
UP-0798	FIL002	367381	1	NFLT NFM61R30T472T1
UP-0798	FIL003-FIL007	341489	5	NFLT BLM21A05PT

UP-0799 MEMORY CARD BOARD

UP-0799	CN101	356767	1	PCN HIF-6-68PA-1.27DS
UP-0799	CN102	352628	1	PCN JC20EA-J68P-V4LT-A1
UP-0799	D101	356838	1	LED HLMP-5050 green
UP-0799	FIL101-FIL108	341489	8	NFLT BLM21A05PT
UP-0799	FIL109-FIL110	367381	2	NFLT NFM61R30T472T1
UP-0799	FIL111-FIL164	341489	54	NFLT BLM21A05PT

UP-0801 OPERATION CONTROL BOARD

UP-0801	CN101	356829	1	CN DX20M-26S
UP-0801	CN102	081083	1	CN HD-LNA D sub lock fitting
UP-0801	CN102	362724	1	CN SDAB-15S-SL-LNK(02)
UP-0801	CN103	081118	1	CN RDAD-15SE-LNA
UP-0801	CN104	085899	1	PCN HIF3BA-20PA-2.54DSA
UP-0801	CN105	089663	1	PCN M60-03-30-114P (3P)
UP-0801	CN106	369441	1	PCN HR212-10RB-8SD
UP-0801	CN107	091205A	1	PCN FFC-14BSM1#02ST
UP-0801	CN108	356785	1	PCN HR212-10R-5SD(02)
UP-0801	C201-C202	159695	2	TAC 267M3502 106MR720 10MF35V
UP-0801	C203	368905	1	CEC ECU V1H 104ZFX
UP-0801	C204	159632	1	TAC 267M2002 106MR533 10MF20V
UP-0801	C205-C206	159695	2	TAC 267M3502 106MR720 10MF35V
UP-0801	C207	159632	1	TAC 267M2002 106MR533 10MF20V
UP-0801	C208-C211	159739	4	CEC GRM39SL 330K50PT 50V 33PF
UP-0801	C301	159766	1	CEC GRM39SL 101K50PT 100PF50V
UP-0801	C302	159748	1	CEC GRM39SL 470K50PT 50V 47PF
UP-0801	C303	159632	1	TAC 267M2002 106MR533 10MF20V
UP-0801	C304	350728	1	EC ECEA1VU101 35V100M
UP-0801	C305	159632	1	TAC 267M2002 106MR533 10MF20V
UP-0801	C306	159695	1	TAC 267M3502 106MR720 10MF35V
UP-0801	C307	368905	1	CEC ECU V1H 104ZFX
UP-0801	C308	350728	1	EC ECEA1VU101 35V100M
UP-0801	C309	159739	1	CEC GRM39SL 330K50PT 50V 33PF
UP-0801	C310	350728	1	EC ECEA1VU101 35V100M

ASSY	CKT NO.	PART NO.	QTY	DESCRIPTION	
UP-0801	C311	159739	1	CEC	GRM39SL 330K50PT 50V 33PF
UP-0801	C312-C313	331107	2	FLC	ECW-U1H223JA5 50V 0.022UF
UP-0801	C314-C315	159632	2	TAC	267M2002 106MR533 10MF20V
UP-0801	C316-C317	159695	2	TAC	267M3502 106MR720 10MF35V
UP-0801	C318-C327	368905	10	CEC	ECU V1H 104ZFX
UP-0801	C328	159766	1	CEC	GRM39SL 101K50PT 100PF50V
UP-0801	C330	159632	1	TAC	267M2002 106MR533 10MF20V
UP-0801	C331-C333	368905	3	CEC	ECU V1H 104ZFX
UP-0801	C401	368905	1	CEC	ECU V1H 104ZFX
UP-0801	C402	159695	1	TAC	267M3502 106MR720 10MF35V
UP-0801	D101-D108	334461	8	D	HSK83 TR
UP-0801	D109-D116	160078	8	D	HSK120TR
UP-0801	D119-D120	160078	2	D	HSK120TR
UP-0801	D121-D122	160096	2	D	1SS294 TE85R
UP-0801	D401-D402	160078	2	D	HSK120TR
UP-0801	FIL101-FIL112	334149	12	NFLT	NFM52R20P506
UP-0801	FIL120-FIL127	341489	8	NFLT	BLM21A05PT
UP-0801	FIL136	334149	1	NFLT	NFM52R20P506
UP-0801	IC101	161469	1	TTL	SN74LS06 NS
UP-0801	IC104	160586	1	CMOS	MC14053BF
UP-0801	IC201	370243A	1	CPU	u PD78214GC-414-AB8
UP-0801	IC202	334202	1	ADIC	MAX232CWE-T
UP-0801	IC203	161469	1	TTL	SN74LS06 NS
UP-0801	IC204	374168	1	CPU	u PD75402AGB-543-3B4
UP-0801	IC205	161692	1	ADIC	TL7705ACPS
UP-0801	IC301	160265	1	OPIC	u PC812G2
UP-0801	IC302	010801	1	ADIC	u PC1316C AUDIO AMP
UP-0801	IC303	160265	1	OPIC	u PC812G2
UP-0801	IC402	160336	1	REG	HA178L08UATR
UP-0801	IC403	160372	1	REG	HA179L08UATR
UP-0801	IC404	160265	1	OPIC	u PC812G2
UP-0801	Q101-Q106	334443	6	TR	2SA1213-Y TE12R
UP-0801	Q107	160122	1	TR	2SA1122 CORD TR
UP-0801	RY101-RY103	356847	3	RY	G6A-274P-ST-US 5V
UP-0801	SW201	357605	1	DSW	CHS-04TB
UP-0801	X102	357552	1	XTAL	CSAC 4.19MGCM-TCceramic oscillator

UP-0802 ORERATION (VR) BOARD

UP-0802	CN101	085899	1	PCN	HIF3BA-20PA-2.54DSA
UP-0802	CN102	313377	1	PCN	B5B-EH
UP-0802	CN103	085515	1	PCN	HKP-6ML-3BT
UP-0802	D101	160078	1	D	HSK120TR
UP-0802	IC105	160336	1	REG	HA178L08UATR
UP-0802	Q101-Q102	160149	2	TR	2SC2618 D TR
UP-0802	VR101-VR102	357819	2	VR	EVJ-02AF15B14 10K OHM
UP-0802	VR103	359942	1	VR	RA12S 10K OHM
UP-0802	VR105	359951	1	VR	EVJ-02AF15B53 5K OHM

UP-0806 LED BOARD

UP-0806	CN101	085515	1	PCN	HKP-6ML-3BT
UP-0806	C101	368905	1	CEC	ECU V1H 104ZFX
UP-0806	C102	159632	1	TAC	267M2002 106MR533 10MF20V
UP-0806	IC101	357837	1	IC	SBX1610-52
UP-0806	LED101-LED102	006245	2	LED	LT-9000N (yellow-green)

UP-0807 CONNECTOR BOARD

UP-0807	CN101	091232A	1	PCN	FFC-20BSM1#02ST
UP-0807	CN102	092775	1	CN	jackHLJ0527-01-030 with nut
UP-0807	CN103	094497	1	CN	HLJ2308-01-3030
UP-0807	CN104	356811	1	PCN	HR212-10RA-8SDL(03)
UP-0807	D101-D102	007075	2	LED	GL3KG8 3 green
UP-0807	SW101	360004	1	PSW	SKHHLR
UP-0807		105147	2	LAMP	PC PCL-490

UP-0813 REGULATOR BOARD

UP-0813	CN102	083401	1	PCN	172034-1
UP-0813	CN103	090206	1	PCN	M60-02-30-114P (2P)
UP-0813	CN105	268069	1	PCN	171457-1
UP-0813	C109	243069	1	FLC	ECQ-V1H104JZ 50V 0.1UF
UP-0813	C111	325702	1	EC	ECEA1HGE010

9. ELECTRICAL PARTS LIST

ASSY	CKT NO.	PART NO.	QTY	DESCRIPTION	
UP-0813	C112	044818	1	FLC	ECQ-V1H224JZ 50V 0.22UF
UP-0813	C120-C121	325702	2	EC	ECEA1HGE010
UP-0813	D103-D105	003649	3	D	1SS81
UP-0813	D106	005362	1	ZD	HZ6LB1
UP-0813	D109-D110	003649	2	D	1SS81
UP-0813	D112	003943	1	D	V06C (1.1A200V)
UP-0813	D113-D117	003649	5	D	1SS81
UP-0813	D120-D121	003649	2	D	1SS81
UP-0813	F103-F106	346207	4	FUSE	23902.5 LITTLE
UP-0813	IC101	021674	1	HIC	SWC-01
UP-0813	IC102	195245	1	REG	UPC7808H
UP-0813	IC103	015788	1	REG	UPC7908H
UP-0813	L101	035891	1	COIL	SKP-5-50 5A 150UH
UP-0813	L103-L104	037791	2	COIL	2643-000301
UP-0813	Q103	071922	1	TR	2SA1015-Y,TPE2 (2SA495)
UP-0813	Q105	002356	1	TR	2SD717-Y
UP-0813	Q107	002026	1	TR	2SC2324K
UP-0813	Q109-Q110	072003	2	TR	2SC1815-Y,TPE2 (2SC372)
UP-0813	Q114-Q115	072003	2	TR	2SC1815-Y,TPE2 (2SC372)
UP-0813	R103	156573	1	R	ERG-1SJ 470
UP-0813	VR101	062781	1	VR	GF06P 1 KOHM
UP-0813	VR102	062923	1	VR	GF06P 200 OHM
UP-0813	VR103	062781	1	VR	GF06P 1 KOHM

UR-3023 CPU BOARD (with ROM)

UR-3023	BAT101	105842	1	BATT	CR17335SE-T-C7 lithium battery 3V
UR-3023	CN101	089957	1	PCN	PCN10EA-90P-2.54DS(05)
UR-3023	CN102	089912	1	PCN	PCN10EA-32P-2.54DS(05)
UR-3023	CN103	081109	1	CN	RDBD-25SE-LNA
UR-3023	CN104	092864	1	PCN	IL-2P-S3FP2-1
UR-3023	C101	159641	1	TAC	267M2002 226MR533 22MF20V
UR-3023	C102	368905	1	CEC	ECU V1H 104ZFX
UR-3023	C103	159632	1	TAC	267M2002 106MR533 10MF20V
UR-3023	C104	357801	1	FLC	ECW-U1H104JB9 50V 0.1UF
UR-3023	C105	331134	1	FLC	ECW-U1H103JA5 50V 0.01UF
UR-3023	C106	159632	1	TAC	267M2002 106MR533 10MF20V
UR-3023	C107	159721	1	CEC	GRM39SL 220K50PT 50V 22PF
UR-3023	C109	159632	1	TAC	267M2002 106MR533 10MF20V
UR-3023	C110-C119	368905	10	CEC	ECU V1H 104ZFX
UR-3023	C122-C124	159632	3	TAC	267M2002 106MR533 10MF20V
UR-3023	C125-C141	368905	17	CEC	ECU V1H 104ZFX
UR-3023	C142-C149	159695	8	TAC	267M3502 106MR720 10MF35V
UR-3023	D101	160087	1	D	1SS307 TE85R
UR-3023	D102	160096	1	D	1SS294 TE85R
UR-3023	D103	071637	1	ZD	HZ3C3TE (3.3-3.5V)
UR-3023	D104	003667	1	D	HP5082-2835
UR-3023	D107-D108	160087	2	D	1SS307 TE85R
UR-3023	FIL101-FIL104	334149	4	NFLT	NFM52R20P506
UR-3023	IC101	013941	1	CPU	TMP68HC000N-16
UR-3023	IC102	161398	1	TTL	74F74SJ
UR-3023	IC104	357427	1	CMOS	TC74ACT164F
UR-3023	IC105	357472	1	CMOS	HD74AC393FP
UR-3023	IC111	357409	1	CMOS	74ACT138SJ
UR-3023	IC112	161709	1	CMOS	74AC138SJ
UR-3023	IC113	357409	1	CMOS	74ACT138SJ
UR-3023	IC114	333863	1	CMOS	74AC08SJ
UR-3023	IC115	161594	1	TTL	SN74LS27NS
UR-3023	IC116	161692	1	ADIC	TL7705ACPS
UR-3023	IC117	323027	1	CMOS	HD74HC123AFP
UR-3023	IC118	160978	1	CMOS	HD74HC74FP
UR-3023	IC119	160889	1	CMOS	HD74HC08FP
UR-3023	IC120	357525	1	TTL	74F14SJ
UR-3023	IC121	352192	1	CMOS	HD74HC01FP
UR-3023	IC122	357499	1	CMOS	HD74HC21FP
UR-3023	IC123	161772	1	CMOS	HD74HCT138FP
UR-3023	IC124	160889	1	CMOS	HD74HC08FP
UR-3023	IC125-IC126	160978	2	CMOS	HD74HC74FP
UR-3023	IC127	161273	1	CMOS	HD74HC148FP
UR-3023	IC128	160889	1	CMOS	HD74HC08FP
UR-3023	IC129	160978	1	CMOS	HD74HC74FP
UR-3023	IC130	359906	1	CMOS	HD74HCT534FP
UR-3023	IC131	161273	1	CMOS	HD74HC148FP
UR-3023	IC132	161415	1	CMOS	HD74HCT240FP
UR-3023	IC133	161772	1	CMOS	HD74HCT138FP
UR-3023	IC134-IC135	160889	2	CMOS	HD74HC08FP
UR-3023	IC136-IC139	160978	4	CMOS	HD74HC74FP
UR-3023	IC140	357516	1	CMOS	HD74HCT374FP
UR-3023	IC141	161273	1	CMOS	HD74HC148FP
UR-3023	IC142	161415	1	CMOS	HD74HCT240FP
UR-3023	IC143	161772	1	CMOS	HD74HCT138FP

ASSY	CKT NO.	PART NO.	QTY	DESCRIPTION	
UR-3023	IC148	448098A	1	RAM	HM628128BLFP-8Z
UR-3023	IC150	448098A	1	RAM	HM628128BLFP-8Z
UR-3023	IC152	448098A	1	RAM	HM628128BLFP-8Z
UR-3023	IC154	448098A	1	RAM	HM628128BLFP-8Z
UR-3023	IC156	448098A	1	RAM	HM628128BLFP-8Z
UR-3023	IC158	448098A	1	RAM	HM628128BLFP-8Z
UR-3023	IC160	448098A	1	RAM	HM628128BLFP-8Z
UR-3023	IC162	448098A	1	RAM	HM628128BLFP-8Z
UR-3023	IC168	323045	1	CMOS	HD74HC132FP
UR-3023	IC169	323179A	1	CPU	MSM6242GS-VKR2
UR-3023	IC170	323188A	1	CPU	HM58C65FP-25 TZ
UR-3023	IC172	365302	1	CPU	TMP82C51AM-10(CELZ
UR-3023	IC173	323197	1	CPU	u PD71054GB-3B4
UR-3023	IC174-IC175	334202	2	ADIC	MAX232CWE-T
UR-3023	IC176	357623	1	CPU	TMP82C79M-2
UR-3023	IC177	333827	1	CMOS	74AC32SJ
UR-3023	IC178	160309	1	ADIC	HA17903FP
UR-3023	IC179-IC180	161415	2	CMOS	HD74HCT240FP
UR-3023	IC181	161255	1	CMOS	HD74HC534FP
UR-3023	IC182-IC184	357481	3	CMOS	TD74BC533F
UR-3023	IC185-IC186	334096	2	CMOS	TD74BC640F
UR-3023	IC187-IC188	161415	2	CMOS	HD74HCT240FP
UR-3023	IC191	333836	1	CMOS	74AC04SJ
UR-3023	IC192-IC193	149901A	2	CMOS	74AC74SJ(CD74AC74M) (SOP)
UR-3023	IC197-IC198	357418	2	CMOS	HD74AC164FP
UR-3023	IC199	365231	1	CMOS	74AC158SJ
UR-3023	IC200	161469	1	TTL	SN74LS06 NS
UR-3023	IC202	149901A	1	CMOS	74AC74SJ(CD74AC74M) (SOP)
UR-3023	IC203	323036	1	CMOS	HD74HC 14FP
UR-3023	IC204	333854	1	CMOS	74AC244SJ
UR-3023	LED101-LED110	357597	10	LED	LT1L51A
UR-3023	Q101	160149	1	TR	2SC2618 D TR
UR-3023	SKT144	356606	1	CN	AXS204011(u -IC socket 40pin)
UR-3023	SKT146	356606	1	CN	AXS204011(u -IC socket 40pin)
UR-3023	SW102-SW104	357605	3	DSW	CHS-04TB
UR-3023	VC101	047637	1	VC	TZ03R 300ER 5.2-30PF
UR-3023	X101	369887	1	XTAL	1343-M1 32MHZ
UR-3023	X102	022931	1	XTAL	KF-38G

UR-3025 OPERATION RY BOARD

UR-3025	CN101	356811	1	PCN	HR212-10RA-8SDL(03)
UR-3025	C001	159632	1	TAC	267M2002 106MR533 10MF20V
UR-3025	C002-C003	368905	2	CEC	ECU V1H 104ZFX
UR-3025	C005-C006	368905	2	CEC	ECU V1H 104ZFX
UR-3025	C101-C104	159695	4	TAC	267M3502 106MR720 10MF35V
UR-3025	C105	368905	1	CEC	ECU V1H 104ZFX
UR-3025	C106	159632	1	TAC	267M2002 106MR533 10MF20V
UR-3025	C401-C402	159739	2	CEC	GRM39SL 330K50PT 50V 33PF
UR-3025	D101-D108	160078	8	D	HSK120TR
UR-3025	D201-D207	160078	7	D	HSK120TR
UR-3025	D301-D308	160078	8	D	HSK120TR
UR-3025	D401-D403	160078	3	D	HSK120TR
UR-3025	D501-D502	160078	2	D	HSK120TR
UR-3025	D504-D505	160078	2	D	HSK120TR
UR-3025	FIL101-FIL105	341489	5	NFLT	BLM21A05PT
UR-3025	IC101	370243A	1	CPU	u PD78214GC-414-AB8
UR-3025	IC102	334202	1	ADIC	MAX232CWE-T
UR-3025	IC103	161469	1	TTL	SN74LS06 NS
UR-3025	IC104	161692	1	ADIC	TL7705ACPS
UR-3025	LED101-LED102	006593	2	LED	LD101YY
UR-3025	L101	037559	1	COIL	SF-T8-50D 125MH 2A
UR-3025	Q301	334443	1	TR	2SA1213-Y TE12R
UR-3025	SP101	073671	1	SP	EFB-RD24C411
UR-3025	SW101-SW108	032484	8	SW	SKHCAD (KHC-10904)
UR-3025	SW201-SW207	032484	7	SW	SKHCAD (KHC-10904)
UR-3025	SW301-SW308	032484	8	SW	SKHCAD (KHC-10904)
UR-3025	SW401-SW403	032484	3	SW	SKHCAD (KHC-10904)
UR-3025	SW501	357605	1	DSW	CHS-04TB

UR-3105 SpO_2 HEAD AMP MAIN BOARD

UR-3105	CN001	089895	1	PCN	PCN10EA-20P-2.54DS(05)
UR-3105	CN003	088512	1	PCN	HKP-20FDS2
UR-3105	CN005	319576	1	PCN	HKP-6FD2-3BT
UR-3105	C001	331179A	1	FLC	ECW-U1H472JA5 50V 0.0047UF
UR-3105	C002	159748	1	CEC	GRM39SL 470K50PT 50V 47PF
UR-3105	C003	331179A	1	FLC	ECW-U1H472JA5 50V 0.0047UF

9. ELECTRICAL PARTS LIST

ASSY	CKT NO.	PART NO.	QTY	DESCRIPTION
UR-3105	C004	159748	1	CEC GRM39SL 470K50PT 50V 47PF
UR-3105	C005	331197A	1	FLC ECW-U1H332JA5 50V 0.0033UF
UR-3105	C006	339607A	1	FLC ECW-U1H222JA5 50V 0.0022UF
UR-3105	C008-C009	357801	2	FLC ECW-U1H104JB9 50V 0.1UF
UR-3105	C010	159712	1	CEC GRM39SL 100D50PT 50V10PF
UR-3105	C013-C015	368905	3	CEC ECU V1H 104ZFX
UR-3105	C016-C017	159632	2	TAC 267M2002 106MR533 10MF20V
UR-3105	C018	331134	1	FLC ECW-U1H103JA5 50V 0.01UF
UR-3105	C019	331072	1	FLC ECW-U1H102JA5 50V 0.001UF
UR-3105	C020	331179A	1	FLC ECW-U1H472JA5 50V 0.0047UF
UR-3105	C021-C022	368905	2	CEC ECU V1H 104ZFX
UR-3105	C023	070148	1	EC ECEA1CU101B 16V 100UF
UR-3105	C024	372544	1	CEC ECKDNS101MBX 100PF
UR-3105	C101-C104	368905	4	CEC ECU V1H 104ZFX
UR-3105	D001-D004	160078	4	D HSK120TR
UR-3105	D005-D006	071548	2	D 1S2076A RE
UR-3105	D007-D009	160078	3	D HSK120TR
UR-3105	FIL001-FIL003	316882	3	NFLT ferrite beads BL02RN2-R62
UR-3105	GA001	026811	1	TUBE Y08-2100B
UR-3105	IC001-IC005	160265	5	OPIC u PC812G2
UR-3105	IC006	160568	1	CMOS MC14051BF
UR-3105	IC007	160407	1	REG LT1009S8
UR-3105	IC008	160327	1	REG HA178L05UATR
UR-3105	IC009	160363	1	REG HA179L05UTR
UR-3105	IC010	160586	1	CMOS MC14053BF
UR-3105	IC011	021718	1	HIC EHD-HA1270 ISOLATE
UR-3105	PC001	002739	1	PTR PC810A
UR-3105	Q001-Q002	160185	2	TR 2SD1418 DB OR DC TR
UR-3105	Q003-Q004	072066	2	TR 2SC1213AKDTZ
UR-3105	T001	036925	1	TF T3772365 EP10PS transformer
UR-3105	T002	036916	1	TF T3772356 EP10IS transformer

UR-3106 SpO_2 HEAD AMP SUB BOARD

UR-3106	CN004	088441	1	PCN HKP-20M5S
UR-3106	CN006	262075	1	PCN HKP-6M2-3BT
UR-3106	C030-C032	368905	3	CEC ECU V1H 104ZFX
UR-3106	C051	331134	1	FLC ECW-U1H103JA5 50V 0.01UF
UR-3106	C052	341471	1	FLC ECW-U1H473JA5 50V 0.047UF
UR-3106	C054	331107	1	FLC ECW-U1H223JA5 50V 0.022UF
UR-3106	C055	331134	1	FLC ECW-U1H103JA5 50V 0.01UF
UR-3106	C056	341471	1	FLC ECW-U1H473JA5 50V 0.047UF
UR-3106	C058	331107	1	FLC ECW-U1H223JA5 50V 0.022UF
UR-3106	C059	341471	1	FLC ECW-U1H473JA5 50V 0.047UF
UR-3106	C060	331134	1	FLC ECW-U1H103JA5 50V 0.01UF
UR-3106	C061	341462A	1	FLC ECW-U1H333JA5 50V 0.033UF
UR-3106	C062	341471	1	FLC ECW-U1H473JA5 50V 0.047UF
UR-3106	C063	331134	1	FLC ECW-U1H103JA5 50V 0.01UF
UR-3106	C064	341462A	1	FLC ECW-U1H333JA5 50V 0.033UF
UR-3106	C065-C066	331107	2	FLC ECW-U1H223JA5 50V 0.022UF
UR-3106	C067-C070	159632	4	TAC 267M2002 106MR533 10MF20V
UR-3106	C071-C072	331107	2	FLC ECW-U1H223JA5 50V 0.022UF
UR-3106	C075-C076	161522	2	CEC C3216JB1H 103KT 0.01MF
UR-3106	C078	159632	1	TAC 267M2002 106MR533 10MF20V
UR-3106	C079-C080	368905	2	CEC ECU V1H 104ZFX
UR-3106	C081-C082	159739	2	CEC GRM39SL 330K50PT 50V 33PF
UR-3106	C083	331134	1	FLC ECW-U1H103JA5 50V 0.01UF
UR-3106	C151-C176	368905	26	CEC ECU V1H 104ZFX
UR-3106	D051-D055	160087	5	D 1SS307 TE85R
UR-3106	D056	160078	1	D HSK120TR
UR-3106	IC050	160577	1	CMOS MC14052BF
UR-3106	IC051-IC053	386289	3	OPIC TLC27M7CPS power sourse
UR-3106	IC054	160265	1	OPIC u PC812G2
UR-3106	IC056	160595	1	CMOS MC14066BF
UR-3106	IC057-IC058	160265	2	OPIC u PC812G2
UR-3106	IC059	160568	1	CMOS MC14051BF
UR-3106	IC060	160523	1	CMOS MC14040BF
UR-3106	IC061	160318	1	ADIC HA17901FP
UR-3106	IC062-IC064	381222	3	CMOS MC14520BF
UR-3106	IC065-IC066	160568	2	CMOS MC14051BF
UR-3106	IC067	160844	1	CMOS MC14584BF
UR-3106	IC068	160701	1	CMOS MC14081BF
UR-3106	IC069	160452	1	CMOS MC14011BF
UR-3106	IC070	160416	1	CMOS MC14001BF
UR-3106	IC071	161264	1	CMOS HD74HC4040FP
UR-3106	IC072	160889	1	CMOS HD74HC08FP
UR-3106	IC073	351032A	1	CMOS TC74HCU04AF
UR-3106	IC075	160327	1	REG HA178L05UATR
UR-3106	PC050	002739	1	PTR PC810A
UR-3106	Q050	160149	1	TR 2SC2618 D TR
UR-3106	SW050	380651	1	SW SW SSSS2-12-11

ASSY	CKT NO.	PART NO.	QTY	DESCRIPTION	
UR-3106	X050	381213	1	XTAL	DS-HC-49U3H 4.032MHZ

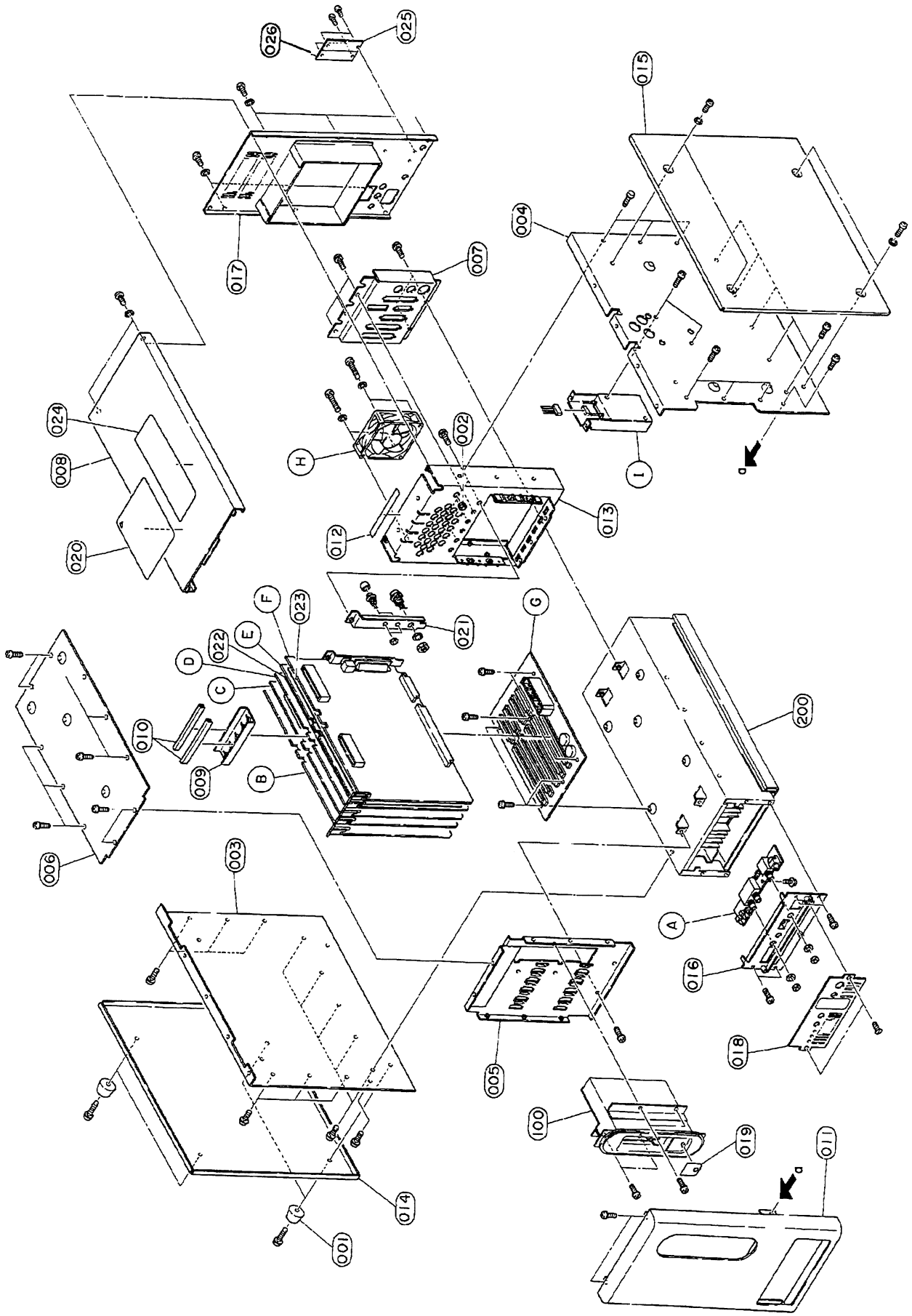
UP-31551 SpO_2 HEAD AMP BOARD

UR-31551		079594A	1	CN	HR16-18R-10S(05) blue

Section 10 MECHANICAL PARTS LIST

10-1 Main Unit

No.	Code No.	Description	
001	111345	Rubber foot	ゴム足 K-30 (ワツシャ入り)
002	297839	Grommet bush.G84	グロメツトゴムブツシュ G84
003	1112-021275B	Left side chassis	サイド シャーシ (L)
004	1112-021284B	Right side chassis	サイド シャーシ (R)
005	1112-021604B	Front chassis	フロント シャーシ
006	1113-063798A	Shield board	シールド板
007	1113-064128D	Rear holder	リア ホルダ
008	1113-064137B	Top cover	トツプ カバ
009	1114-234139	Circuit board holder	P板 押え
010	1114-234166	U-type rubber	Uガタ ゴム
011	1123-020736B	Front frame (6)	フロントフレーム
012	1124-052165A	Color display nameplate	カラー表示銘板
013	1143-008178B	Rear chassis ASSY	リア シャーシASSY
014	6113-002199A	Left side cover	サイド カバ (L)
015	6113-002207A	Right side cover	サイド カバ (R)
016	1114-234148A	Jack holder	ジャック ホルダ
017	1122-007976B	Rear panel	リア パネル
	6122-000879	Rear panel A	リア パネル A
018	6123-001653A	Front panel A	フロント パネル A
020	6123-001751	BSM warning panel	BSM 注意パネル
021	6114-006522	Antenna connector holder	コネクタ ホルダ (ANT)
022	1113-064155A	CRTC shield cover.2	CRTC シールド カバ.2
023	1113-064173A	CRTC shield cover.1	CRTC シールド カバ.1
25	1124-036441	BSM System nameplate	BSM システム銘板
26	1124-036432	BSM Main Unit nameplate	BSM 本体銘板
100	UP-0799	MEMORY CARD Board	
200	SC-018R	Power Transformer Unit	
A	UP-0807	CONNECTOR Board	コネクタ ボード
B	UP-0670	DPU Board	DPU ボード
C	UP-0563	COM3 Board	COM3 ボード
D	UR-3027	CPU Board	CPU ボード
E	UP-0795	CRTC Board	CRTC ボード
F	UP-0797	I/O Board	I/O ボード
G	UP-0798	MOTHER Board	マザー ボード
H	367737	Fan, ASF-84371	ファン, ASF-84371
I	ZR-800P	Receiver Unit	レシーバーユニット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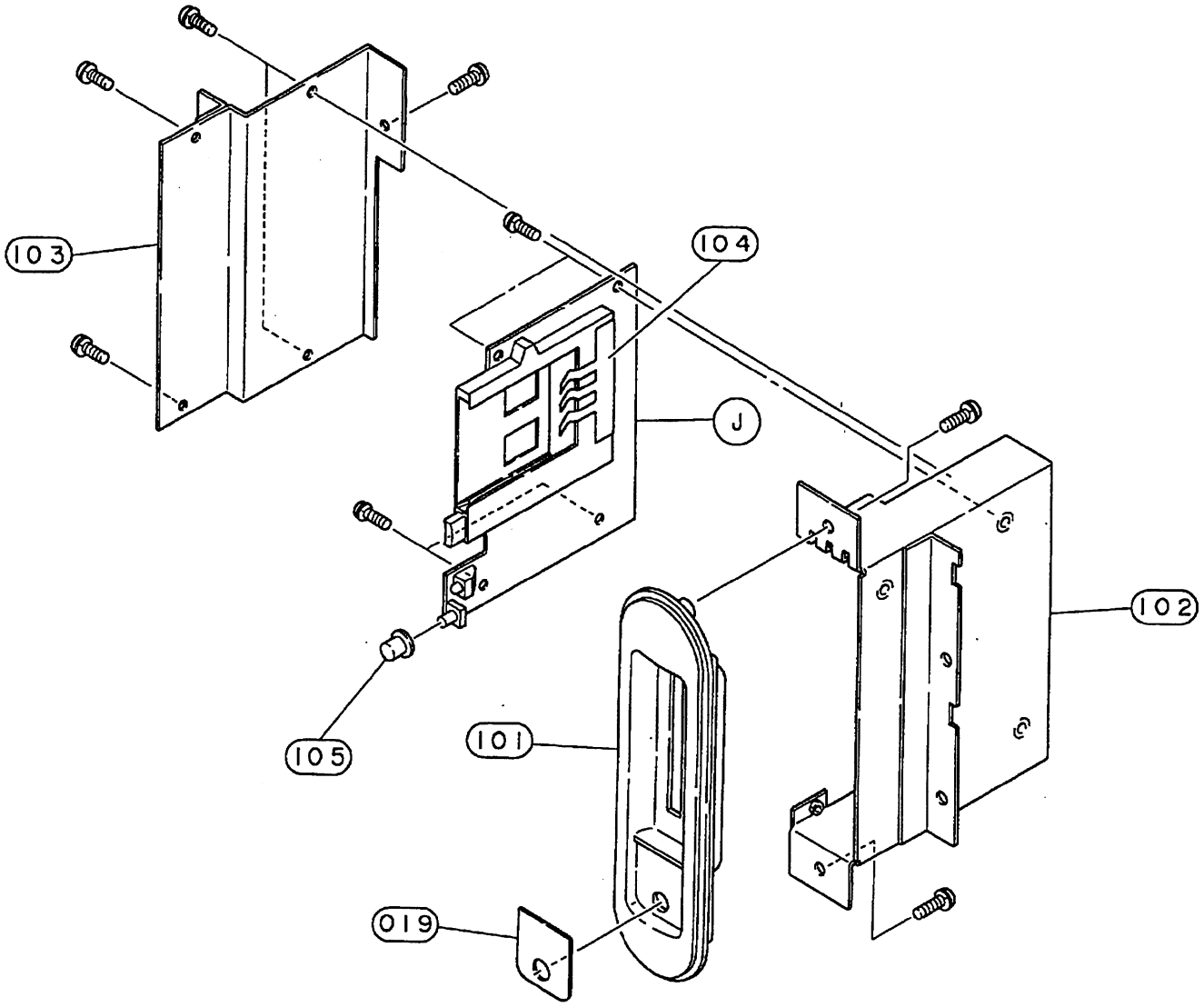
10. MECHANICAL PARTS LIST

No.	Code No.	Description	
019	6124-004051A	MC panel A	MC パネル A
101	1112-021622C	MC front panel	MC フロント パネル
102	1113-064164C	MC shield case.2	MC シールド ケース.2
103	1114-234184C	MC shield case.1	MC シールド ケース.1
104	6114-002161	MC shield spring	MC シールド バネ
105	6114-002179	Memory SW key top	メモリーSWキートップ
J	UP-0799	MEMORY CARD Board	メモリカード ボード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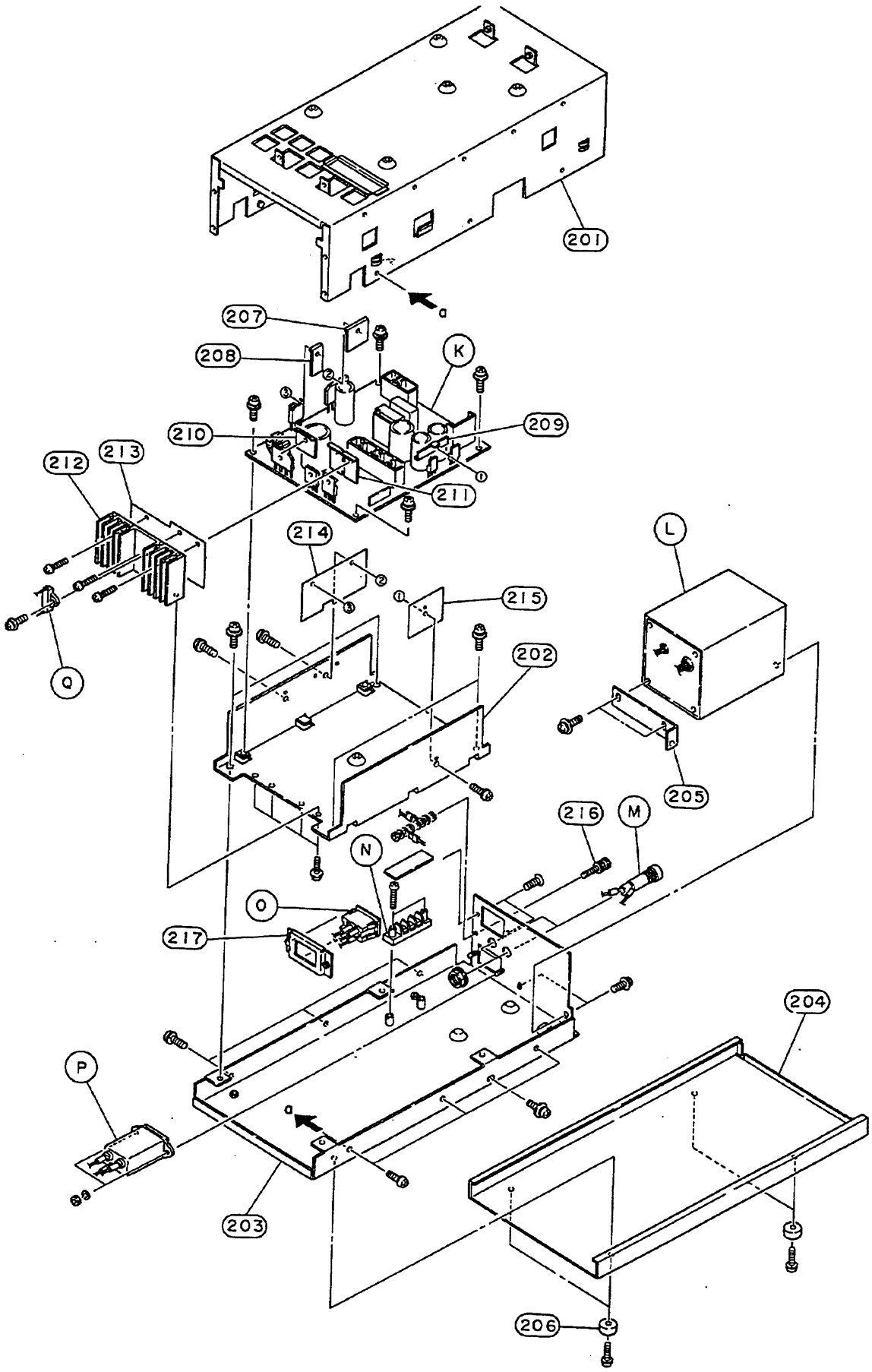
10-2 Power Transformer Unit

No.	Code No.	Description	
201	1112-021266A	Internal chassis	内部シャーシ
202	1113-063789A	Chassis.2	電源シャーシ.2
203	113-063771A	Chassis.1	電源シャーシ.1
204	6113-002956	Bottom cover	ボトム カバ
205	1114-233434A	Transformer holder	トランス ホ･ルダ
206	367835	Flat type rubber foot CK-17	平型ゴム足 CK-17
207	6114-000395	D fixing plate	D 取付け板
208	6114-000484	TR fixing plate (2)	TR 取付け板 (2)
209	1114-151175	Transistor fixing plate 2A	トランジスタ固定金具 2A
210	6114-000395	D fixing plate	D 取付け板
211	6114-000475	TR fixing plate (1)	TR 取付け板 (1)
212	6114-000038	Radiator	放熱器
213	6114-000493	Radiation sheet.1	放熱シート.1
214	6114-000564	Radiation sheet.2	放熱シート.2
215	6114-000617	Radiation sheet.3	放熱シート.3
216	1144-010734A	Equipotential terminal ASSY	アースターミナル ASSY
217	1114-234157A	Switch holder	スイッチ ホ･ルダ
K	UP-0813	Regulator Board	レギュレータユニット ボード
L	365828 365837	Power Transformer for SC-018RJ Power Transformer for SC-018RK	トランス
M	104825	Fuse holder	ヒューズ ホルダFEU031-1681
N	103131	Power terminal	端子台 ULC-505-3P-C
O	370368	Power switch	電源 スイッチ, JW-M22-RKK
P	024252	AC inlet	AC インレット, SUP-E3G-E2
Q	325854	Thermal switch	サーマルスイッチ,OHD3-90MU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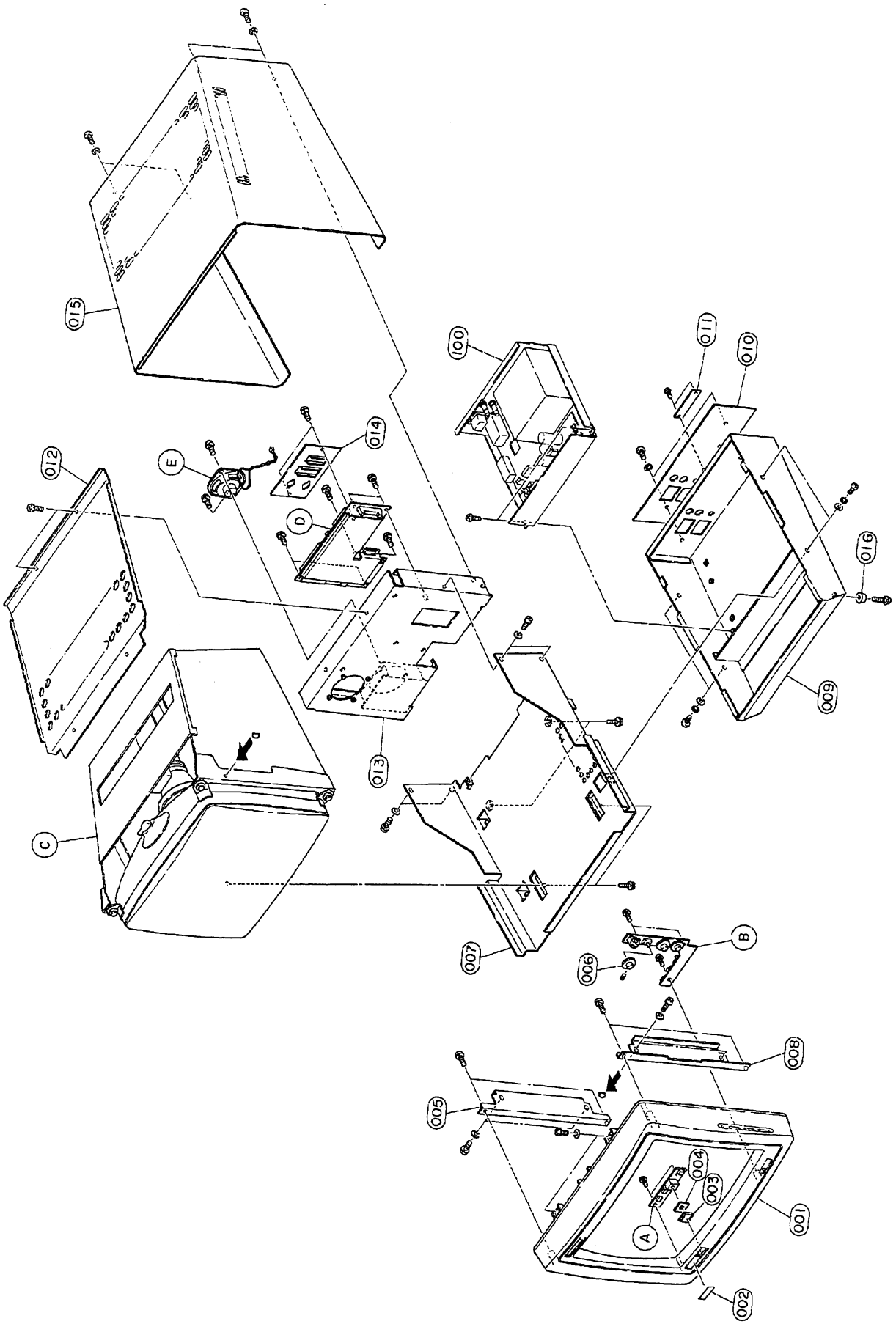
10-3 Display Unit

No.	Code No.	Description	
001	6142-000191A	Front panel ASSY	フロント パネル ASSY
002	6124-004006	LED panel A	LED パネル.A
003	6114-007111A	Filter	フィルタ
004	6114-007352A	Fixed sponge	固定 スポンジ
005	6113-002457B	CRT unit fixing plate	CRT 取付け金具
006	6114-005559	VR knob	VR ツマミ
007	6112-001103B	Bottom chassis	ボトム シャーシ
008	6113-002457B	CRT unit fixing plate	CRT 取付け金具
009	6112-001095A	Bottom cover	ボトム カバ
010	6123-001395	Power supply panel	電源 パネル
011	1124-024632	Display unit nameplate	本体銘板
012	6113-002448	Reinforcement plate	補強板
013	6112-001121	Rear chassis	リヤ シャーシ
014	6124-003239	Connector panel	コネクタ パネル
015	6112-001112A	Display unit cover	カバ
016	111345	Rubber foot with washer	ゴム足 K-30 (ワッシャイリ)
100	SC-019R	Power Supply Unit	
A	UP-0806	LED Board	
B	UP-0802	OPERATION (VR) Board	
C	410325	CRT unit, QA1465	
D	UP-0801	OPERATION CONTROL Board	
E	073662	Speaker EAS-65P34S 160Ω	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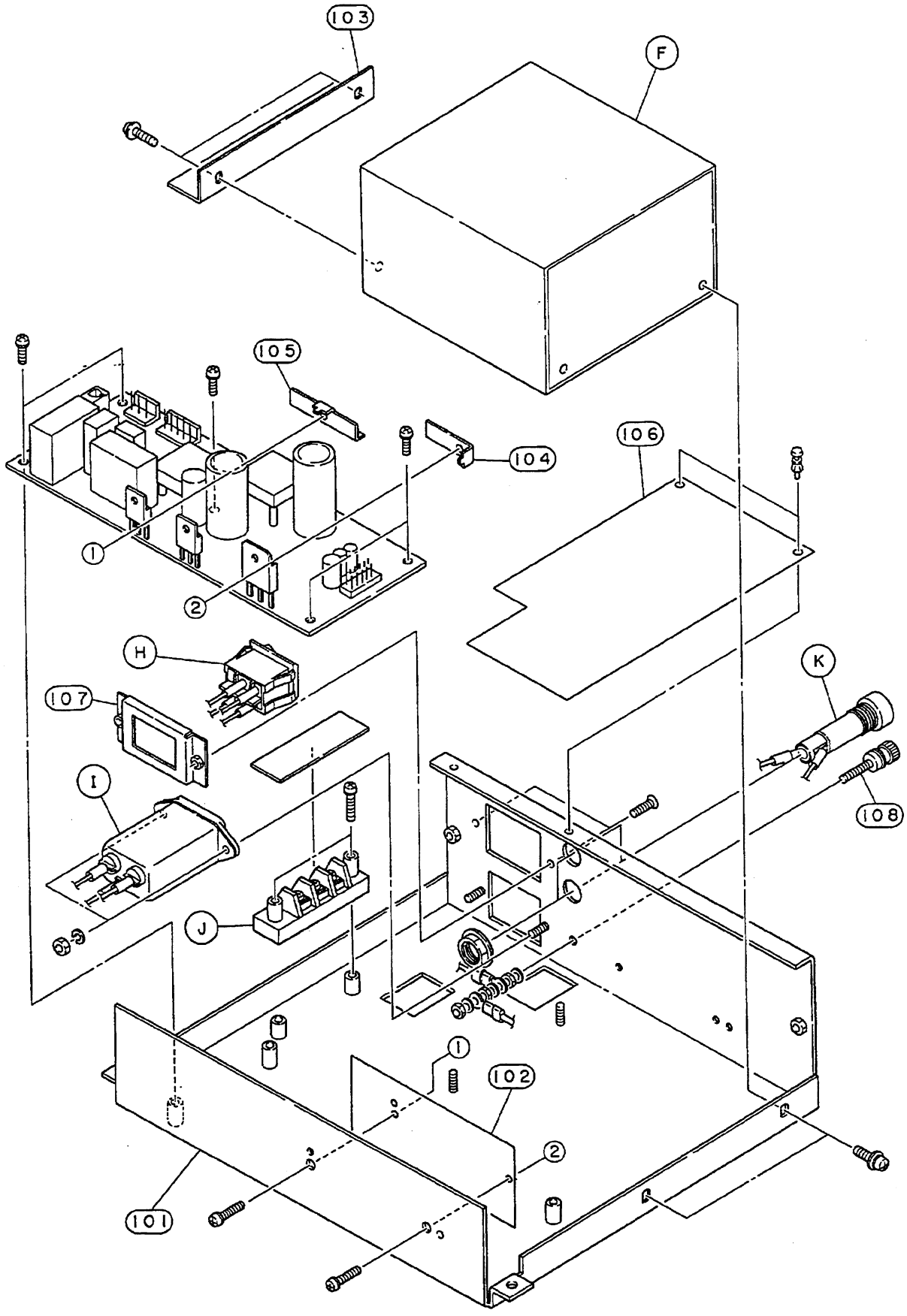
10-4 Power Supply Unit

No.	Code No.	Description	
101	6112-000541	Chassis	シャーシ
102	6114-002562	Heat insulation sheet	放熱シート
103	6114-002312	Transformer fixing plate	トランス金具
104	6114-002116	TR fixing plate	TR取付け板
105	1114-151175	Transistor fixing plate.2A	トランジスタ固定金具.2A
106	6114-003196	Insulation sheet	絶縁 シート
107	1114-234157A	Switch holder	スイッチ ホルダ
108	1114-010734A	Equipotential terminal ASSY	アースタミナル ASSY
F	365864	Power Transformer for SC-019RJ	トランス
	365873	Power Transformer for SC-019RK	
H	370368	Power switch	JW-M22RKK
I	024252	Line filter	ラインフィルタ SUP-E3G-E-2
J	103131	Power terminal	端子台コウワ ULC-505-3P-C
K	104825	Fuse holder	ヒューズホルダ FEU031 1681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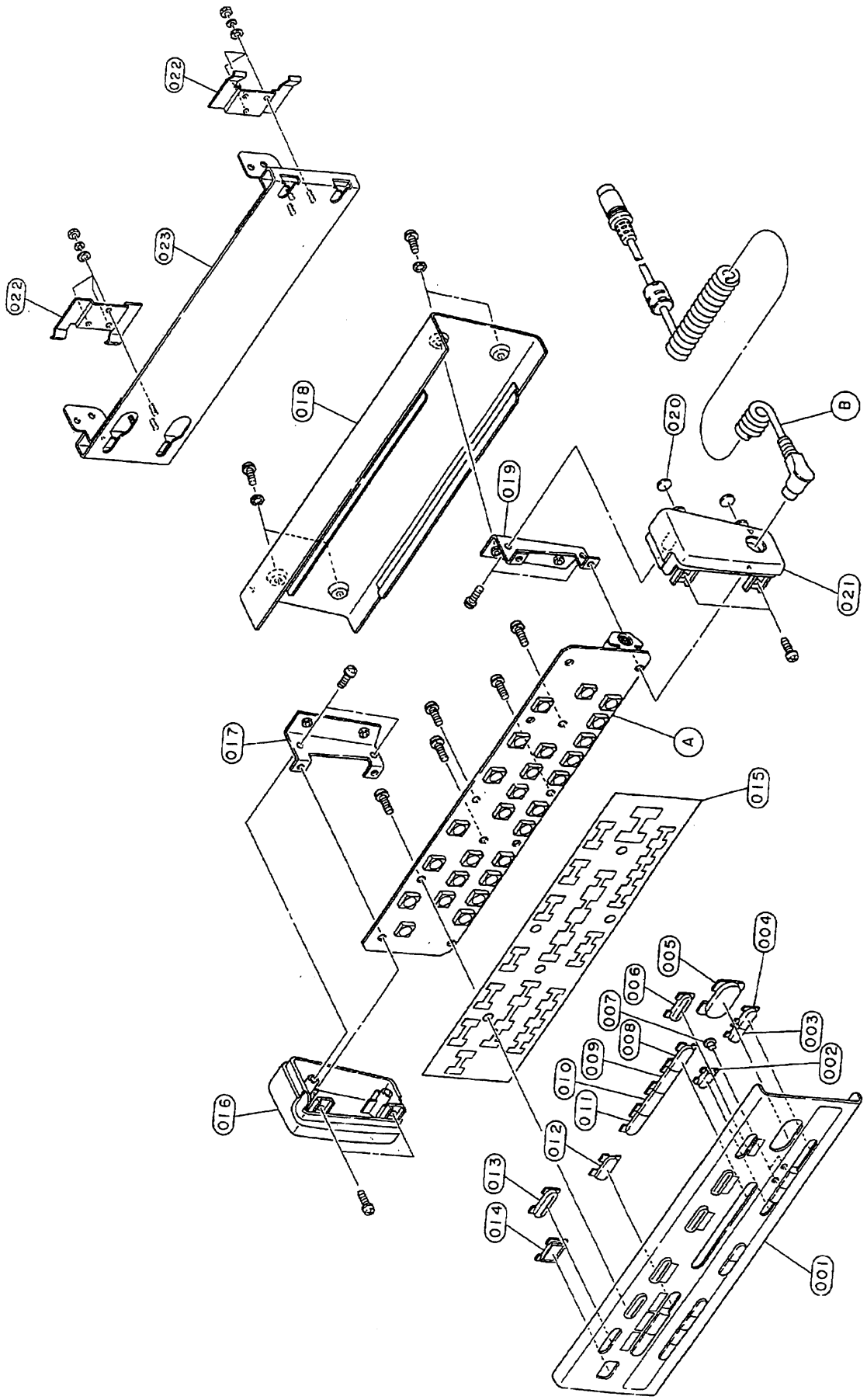
10-5 Keypad

No.	Code No.	Description	
001	6122-000389A	Operation panel	操作部 本体シルク図
002	6114-003124B	Key top 4	キートップ 4
003	2114-081268	Key top 5×15 (L.Gray)	キートップ5×15(ライトグレー)
004	6114-003124B	Key top 4	キートップ 4
005	6124-002276	Key top 2	キートップ 2 シルク図
006	6124-003702A	Key top 6A.2	キートップ 6Aシルク図.2
007	6114-003151	LED spacer	LED スペーサ
008	6124-002267B	Key top 3	キートップ 3 シルク図
009	6114-006879	Key top 8×20 (XL.Gray)	キートップ8×20(エキストライトグレー)
010	6124-002294A	Key top 5	キートップ 5シルク図
011	6114-003098B	Key top 3	キートップ 3
012		Instruction label (6-2A)	取り説パネル。(6-2A)
013	6124-003694A	Key top 6A.1	キートップ 6Aシルク図.1
014	6124-002285A	Key top 1	キートップ 1 シルク図
015	6112-000461B	Key top positioning sheet	位置決めシート
016	6112-000514C	Left side cover	サイド カバ (左)
017	6113-001101D	Operation board holder.2	操作部固定板.2
018	6112-000523B	Keypad bottom frame	操作部ソコイタ
019	6113-001093C	Operation board holder.1	操作部固定板.1
020	6114-008805	Rubber foot	ゴムパツト
021	6112-000505C	Right side cover	サイド カバ (右)
022	6114-009377	Click spring	クリックバネ
023	6112-000488B	Keypad holder	操作部結合金具
A	UR-3025	OPERATION RY Board	
B	359996	Keypad connecting cable	キーパット接続ケーブル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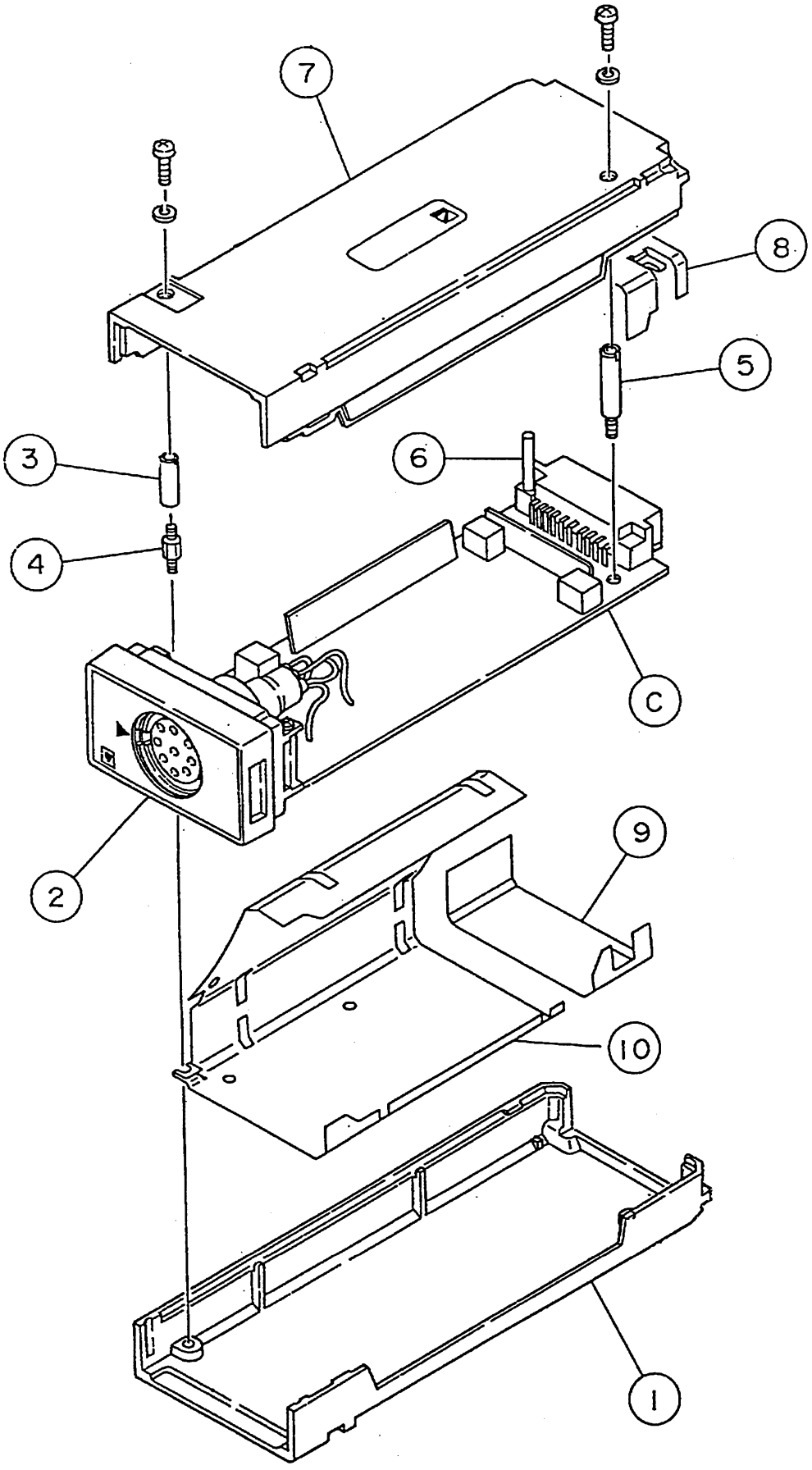
10-6 Head Amplifiers

10-6-1 ECG/Respiration Head Amplifier, AC-800P

Index	Code No.	Description	
1	1112-013569	Head amp housing (right)	アンプユニットケース(右)
2	1112-013542A	ECG Input connector case	ECGアンプユニット本体
3	1114-190025B	PCB Support-2	P板支柱2
4	1114-190052	PCB Support-1	P板支柱1
5	1114-169397	PCB Support	
6	1114-177281	Spacer	反り防止スペーサ
7	1112-013533A	Head amp housing (left)	アンプユニットケース(左)
8	1114-171055B	Shielding cover DDG	
9	1114-179448B	Shielding cover DMG	
10	1113-049831A	Shielding cover F	
C	UP-0272	ECG Head Amp board	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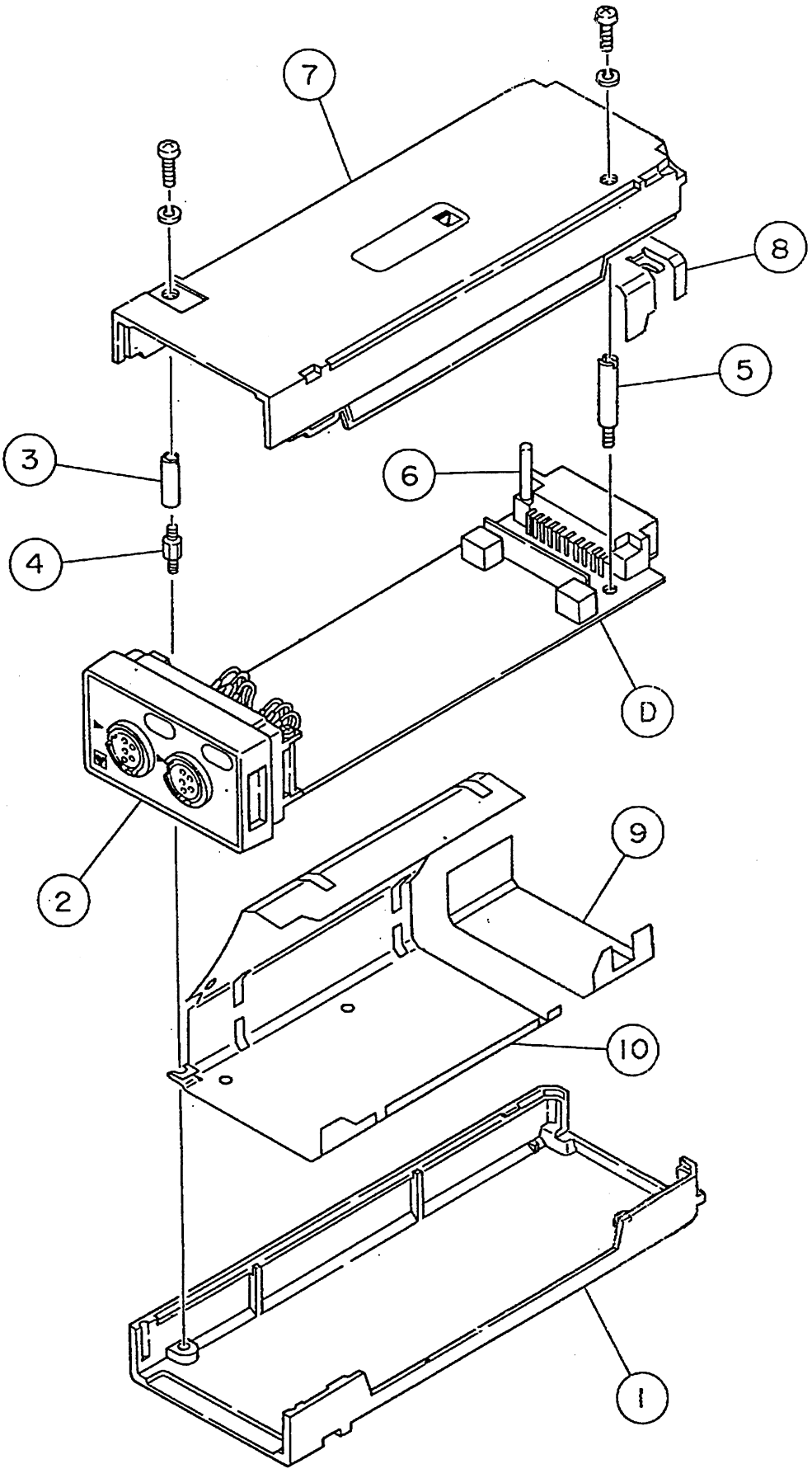
10-6-2 Blood Pressure Head Amplifier, AP-800PA

Index	Code No.	Description	
1	1112-013569A	Head amp housing (right)	アンプユニットケース(右)
2	1112-014238A	BP Input connector case	5Px2 アンプユニット本体
3	1114-190025B	PCB Support-2	P板支柱.2
4	1114-190052	PCB Support-1	P板支柱.1
5	1114-169397	PCB Support	
6	1114-177281	Spacer	反り防止スペーサ
7	1112-013533A	Head amp housing (left)	アンプユニットケース(左)
8	1114-171055B	Shielding cover DDG	
9	1114-179448B	Shielding cover DMG	
10	1113-049831A	Shielding cover F	
D	UP-0369	Blood Pressure Head Amp board	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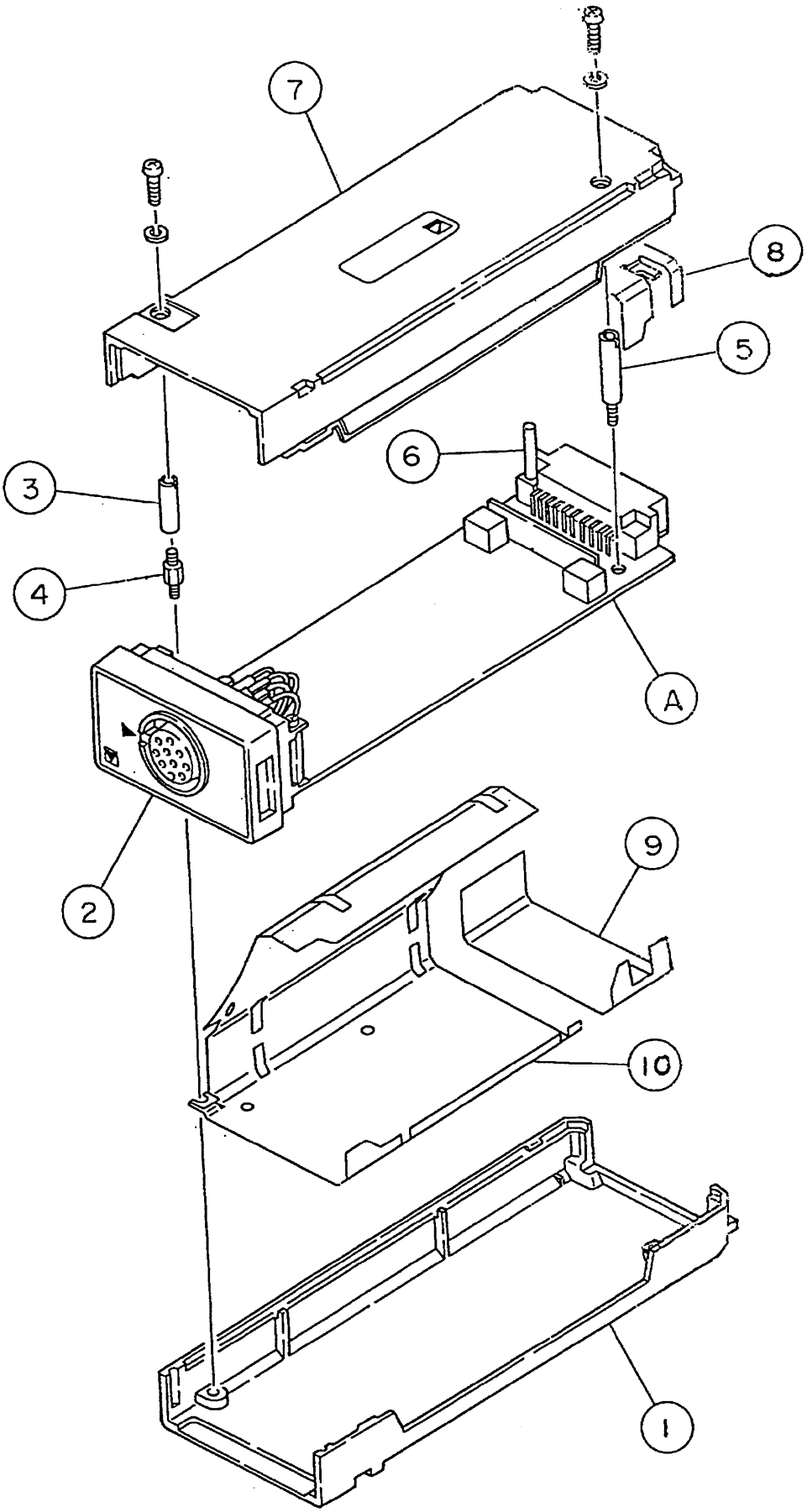
10-6-3 Cardiac Output Head Amplifier, AH-800PA

Index	Code No.	Description	
1	1112-013569A	Head amp housing (right)	アンプユニトケース(右)
2	1112-014211A	CO Input connector case	10P, 15P アンプユニット本体
3	1114-190025B	PCB Support-2	P板支柱.2
4	1114-190052	PCB Support-1	P板支柱.1
5	1114-169397	PCB Support	
6	1114-177281	Spacer	反り防止スペーサ
7	1112-013533A	Head amp housing (left)	アンプユニットケース(左)
8	1114-171055B	Shielding cover DDG	
9	1114-179448B	Shielding cover DMG	
10	1113-049831A	Shielding cover F	
A	UP-0318	Cardiac Output Head Amp board	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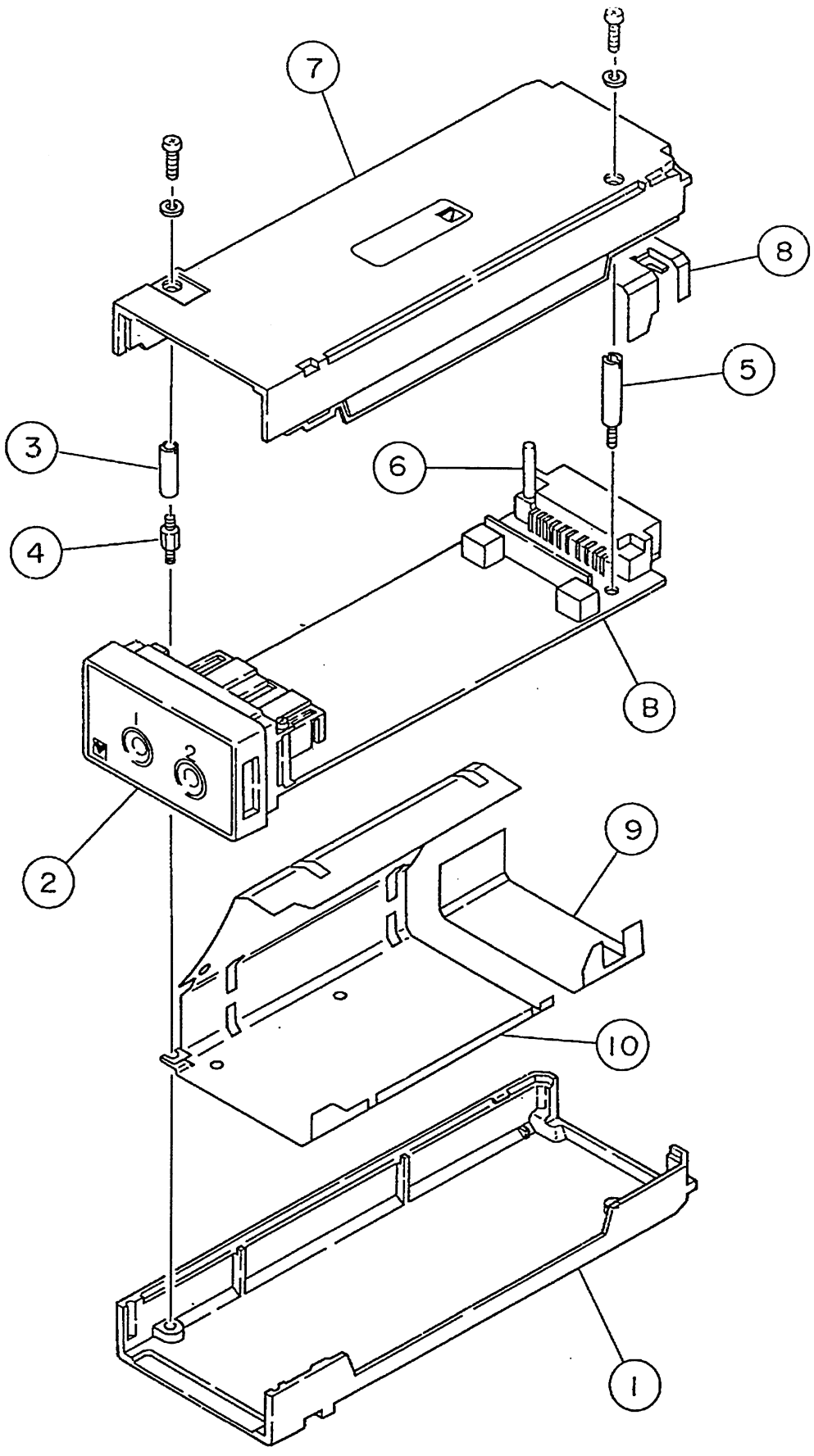
10-6-4 Temperature Head Amplifier, AW-800PA

Index	Code No.	Description	
1	1112-013569A	Head amp housing (right)	アンプユニットケース(右)
2	1112-013587	TEMP Input connector case	TEMP アンプユニット本体
3	1114-190025B	PCB Support-2	P板支柱 2
4	1114-190052	PCB Support-1	P板支柱 1
5	1114-169397	PCB Support	
6	1114-177281	Spacer	反り防止スペーサ
7	1112-013533A	Head amp housing (left)	アンプユニットケース(左)
8	1114-171055B	Shielding cover DDG	
9	1114-179448B	Shielding cover DMG	
10	1113-049831A	Shielding cover F	
B	UP-0319	Temp Head Amp board	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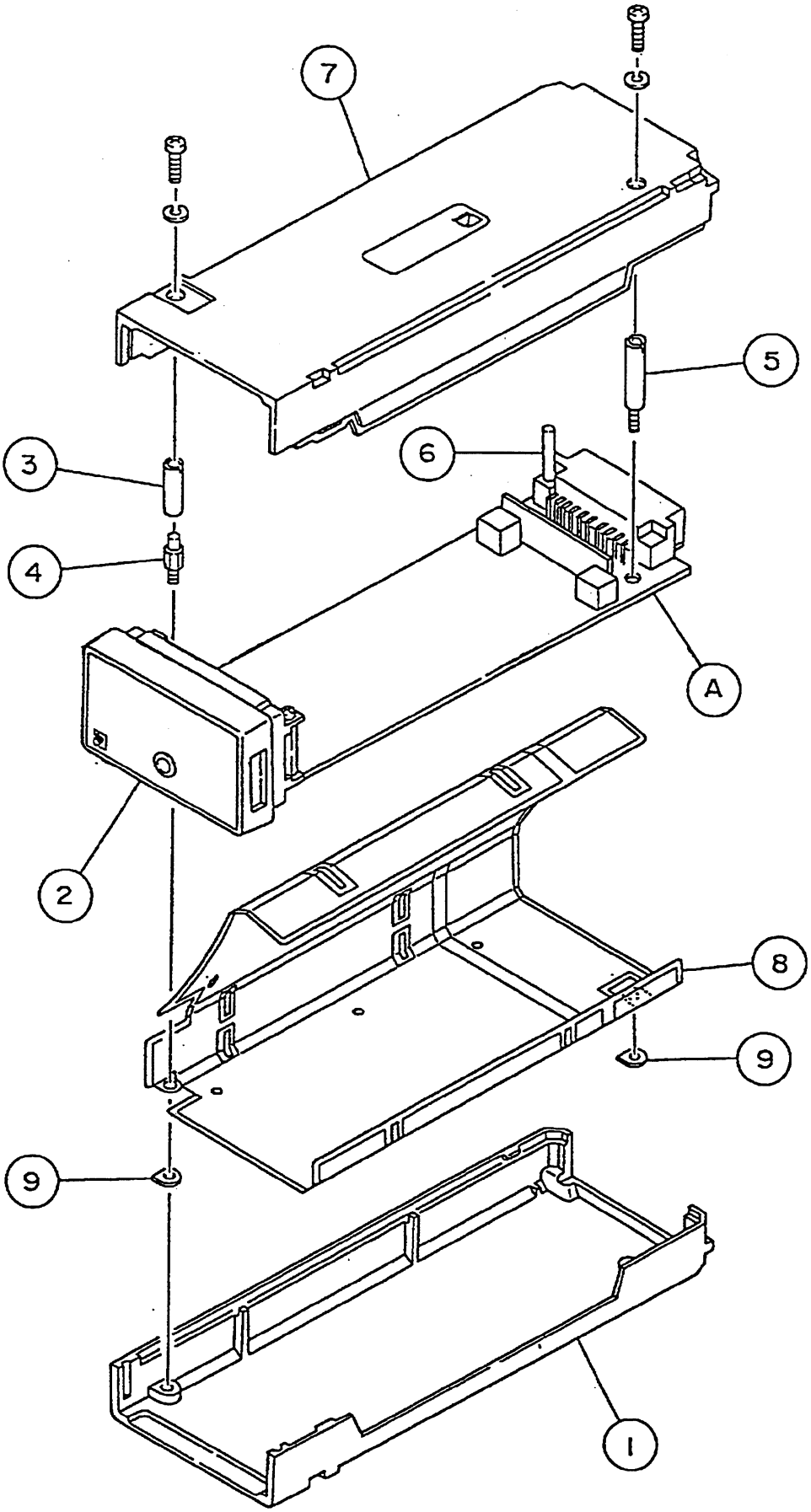
10-6-5 Respiration Head Amplifier, AR-800PA

Index	Code No.	Description	
1	1112-013569A	Head amp housing (right)	アンプユニットケース(右)
2	1112-014211A	10P, 15P amp main unit	10P, 15P アンプユニット本体
3	1114-190025B	PCB Support-2	P板支柱.2
4	1114-190052	PCB Support-1	P板支柱.1
5	1114-169397	PCB Support	
6	1114-177281	Spacer	反り防止スペーサ
7	1112-013533A	Head amp housing (left)	アンプユニットケース(左)
8	1113-047299	Laminated shielding plate	ラミネート シールド板
9	1114-205946	Spacer	スペーサ
10	1124-038778B	AR-800PA front panel	AR-800PA 表パネル
A	UP-0548	Respiration Head Amp board	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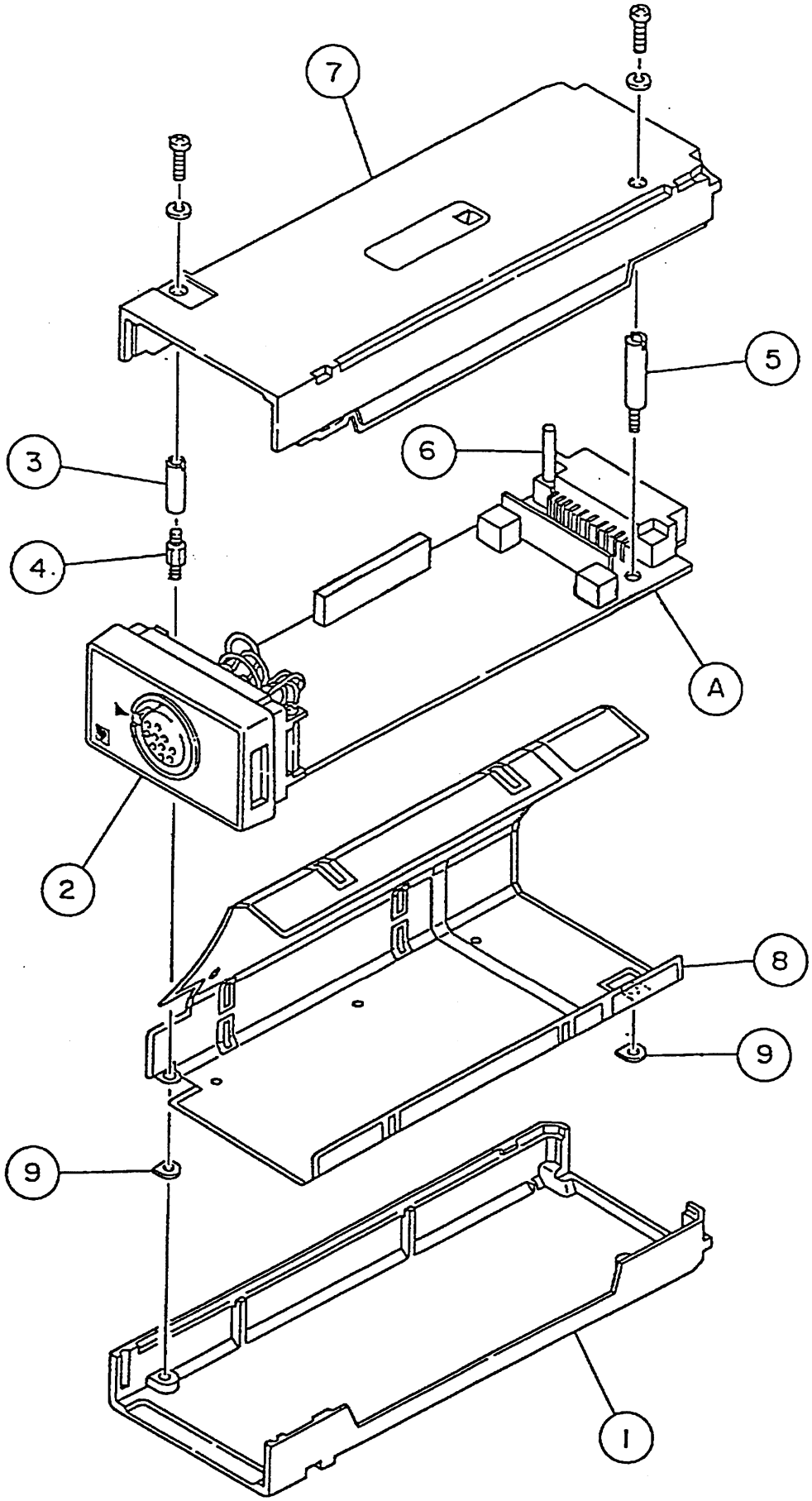
10-6-6 SpO_2 Head Amplifier, AL-800PA

Index	Code No.	Description	
1	1112-013569A	Head amp housing (right)	アンプユニットケース(右)
2	1112-014211A	10P, 15P amp main unit	10P,15Pアンプユニット本体
3	1114-190025B	PCB Support-2	P板支柱.2
4	1114-190052	PCB Support-1	P板支柱.1
5	1114-169397	PCB Support	
6	1114-199738	Spacer	反り防止 スペーサ.B
7	1112-013533A	Head amp housing (left)	アンプユニットケース(左)
8	1113-047299	Laminated shielding plate	ラミネートシールド板
9	1114-205946	Spacer	スペーサ
10	1124-038537A	AL-800PA front panel	AL-800PA 表パネル
A	UP-0551	SpO_2 Main board	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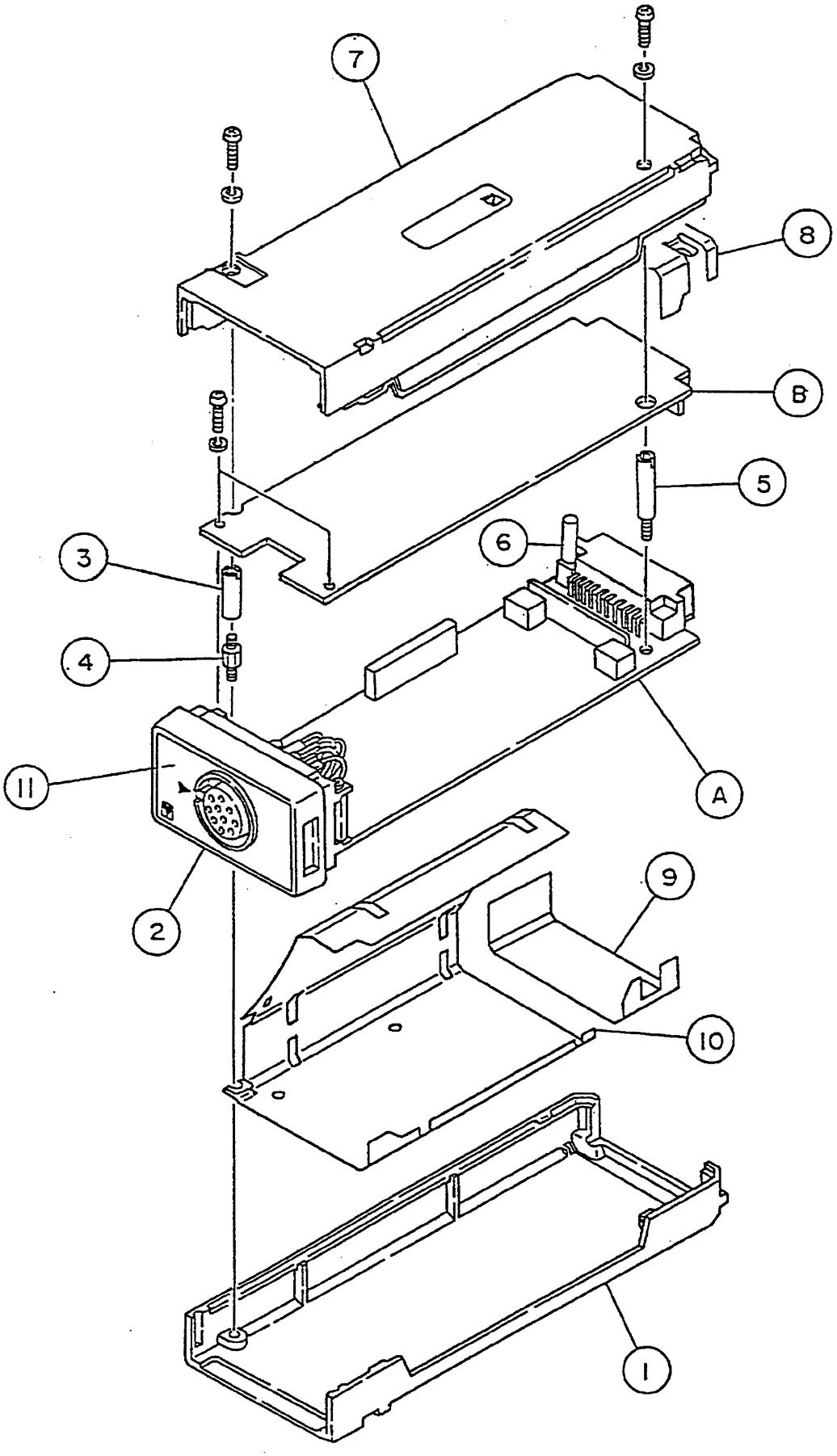
10-6-7 EEG Head Amplifier, AE-800PA

Index	Code No.	Description	
1	1112-013569A	Head amp housing (right)	アンプユニットケース(右)
2	1112-014211A	EEG input connector case	10P, 15P アンプユニット本体
3	1114-190025B	PCB Support-2	P板支柱.2
4	1114-190052	PCB Support-1	P板支柱.1
5	1114-169397	PCB Support	
6	1114-199738	Spacer	反り防止スペーサ.B
7	1112-013533A	Head amp housing (left)	アンプユニットケース(左))
8	1114-171055B	Shielding cover DDG	
9	1114-179448B	Shielding cover DMG	
10	1113-049831A	Shielding cover F	
11	1124-033132A	AE-800PA front panel	AE-800PA表パネル
A	UP-0421	EEG main board	
B	UP-0422	EEG sub board	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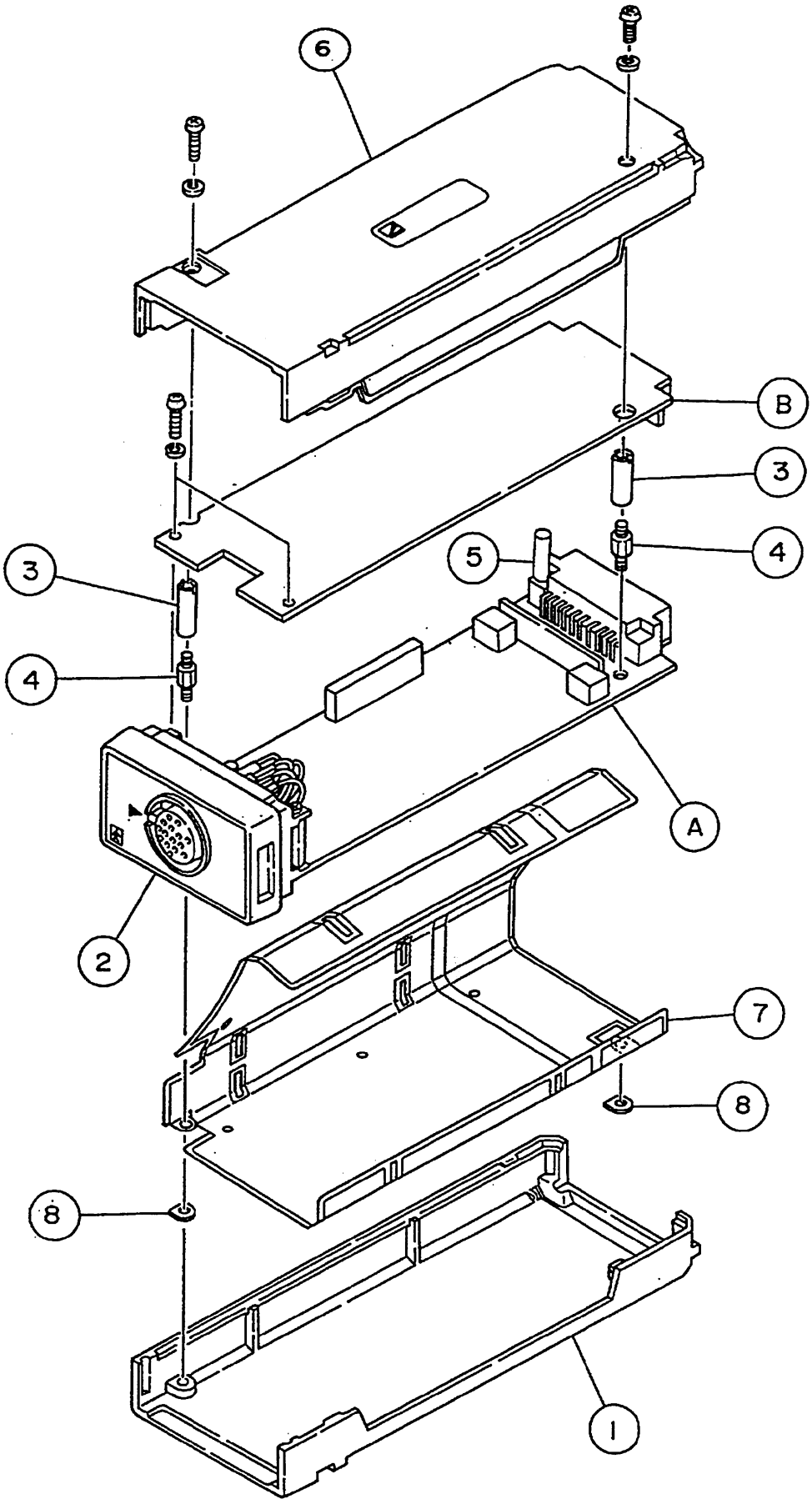
10-6-8 CO_2 Head Amplifier, AG-800PA

Index	Code No.	Description	
1	1112-013569A	Head amp housing (right)	アンプユニットケース(右)
2	1112-014211A	Amp. unit front frame (10P, 14P)	10P,15P アンプユニット本体
	1124-038796A	AG-800PA front panel	AG-800PA 表パネル
3	1114-190025B	PCB Support-2	P板支柱.2
4	1114-190052	PCB Support-1	P板支柱.1
5	1114-199738	Spacer	反り防止 スペーサ.B
6	1112-013533A	Head amp housing (left)	アンプユニットケース(左)
7	1113-047299	Laminated shielding plate	ラミネート シールド板
8	1114-205946	Spacer	スペーサ
A	UP-0588	CO_2 main board	
B	UP-0589	CO_2 sub board	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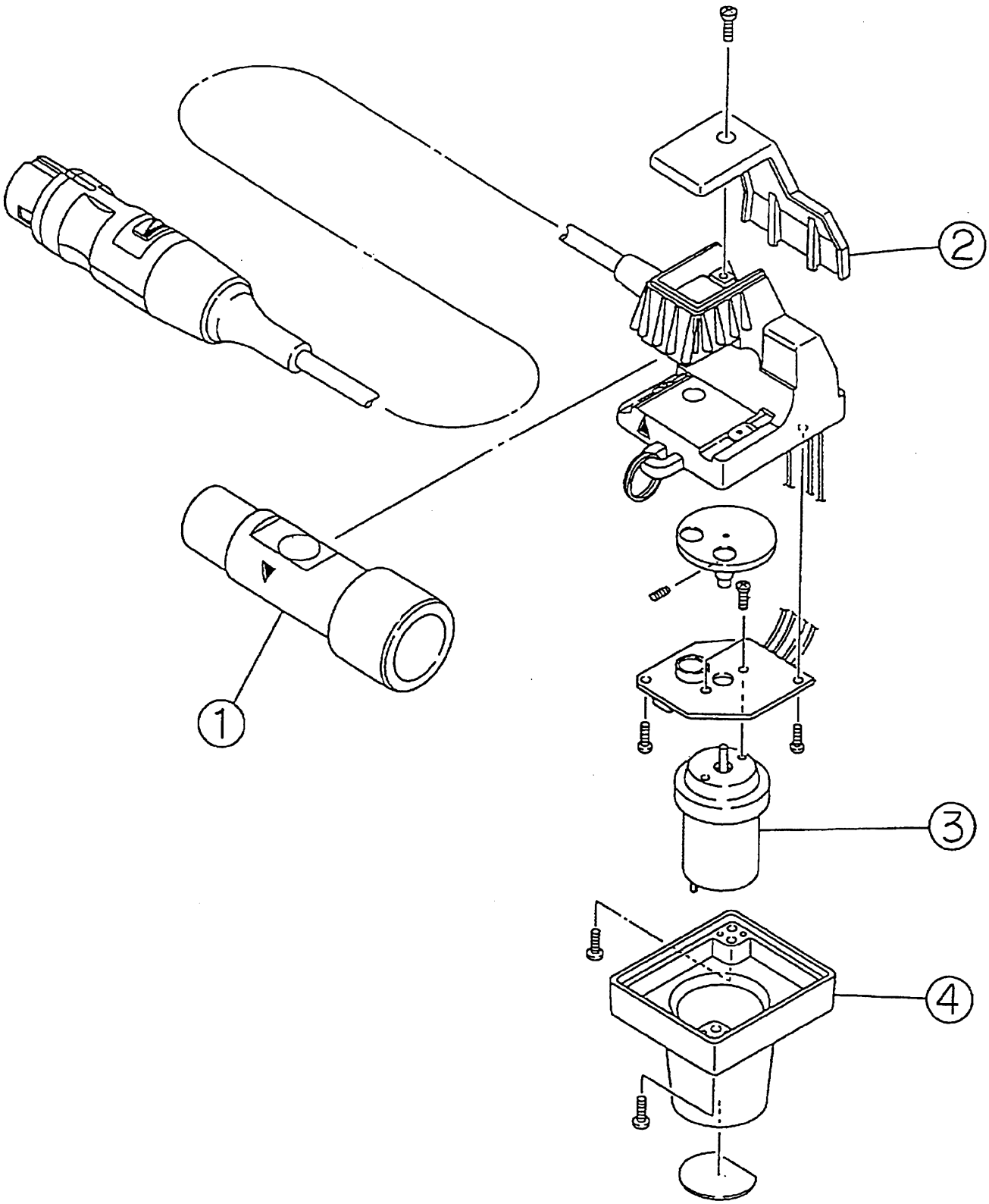
10-6-9 CO_2 Sensor, TG-706P

Index	Code No.	Description
1	YG-706P	CO_2 cell
2	1113-043588C	RG-706P housing TC
3	YS-017P4	RG-706P motor Assy
4	1113-052943	RG-706P housing TA.2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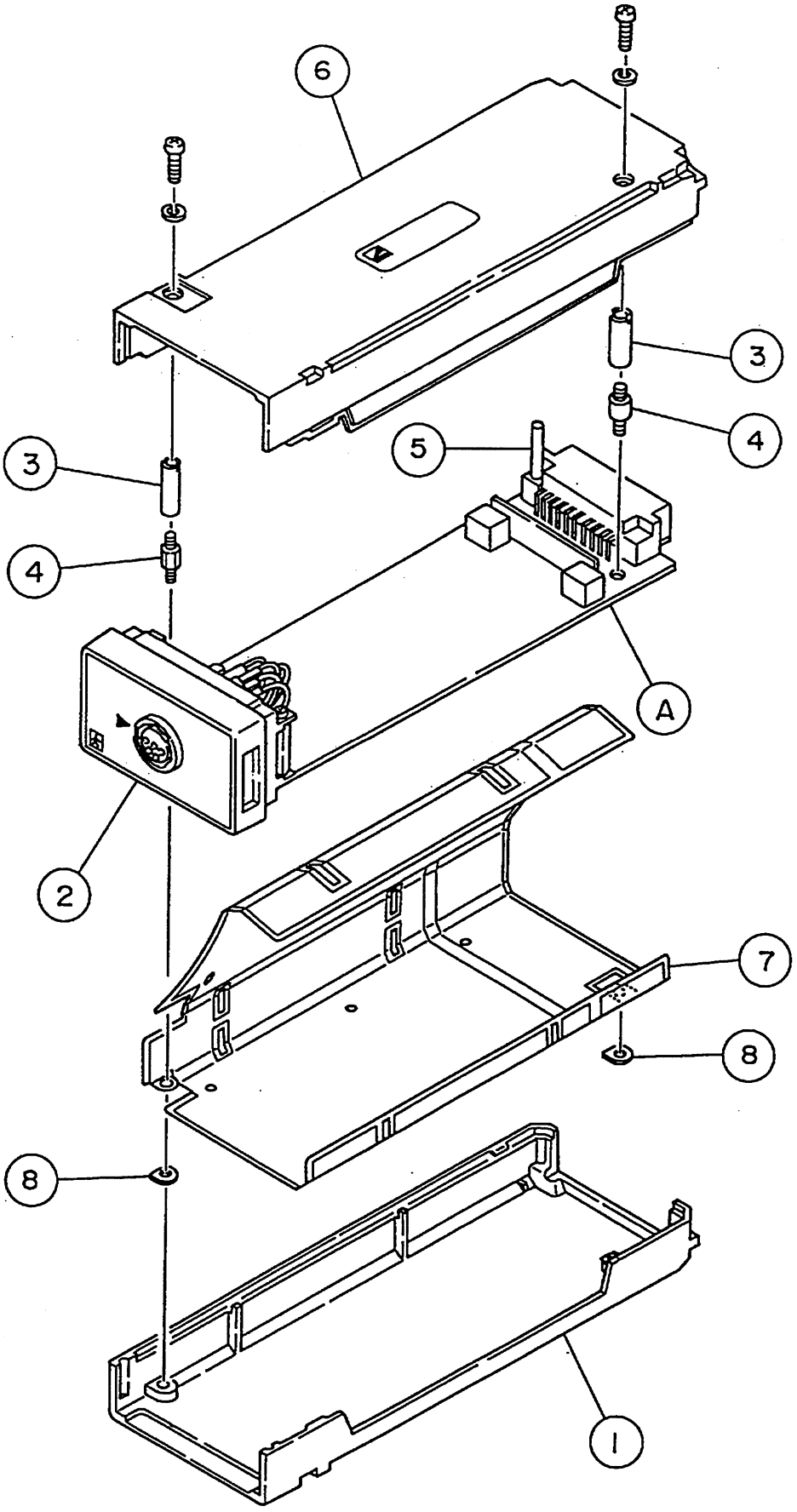
10-6-10 O_2 Head Amplifier, AG-820PA

Index	Code No.	Description	
1	1112-013569A	Head amp housing (right)	アンプユニットケース(右)
2	1112-014238A	Amplifier unit front frame (5P×2)	5Px2 アンプユニット本体
	1124-039206B	AG-820PA front panel	AG-800PA 表パネル
3	1114-190025B	PCB Support-2	P板支柱.2
4	1114-190052	PCB Support-1	P板支柱.1
5	1114-177281	Spacer	反り防止スペーサ
6	1112-013533A	Head amp housing (left)	アンプユニットケース(左)
7	1113-047299	Laminated shielding panel	ラミネート シールド板
8	1114-205946	Spacer	スペーサ
A	UP-0592	O_2 Head Amp board	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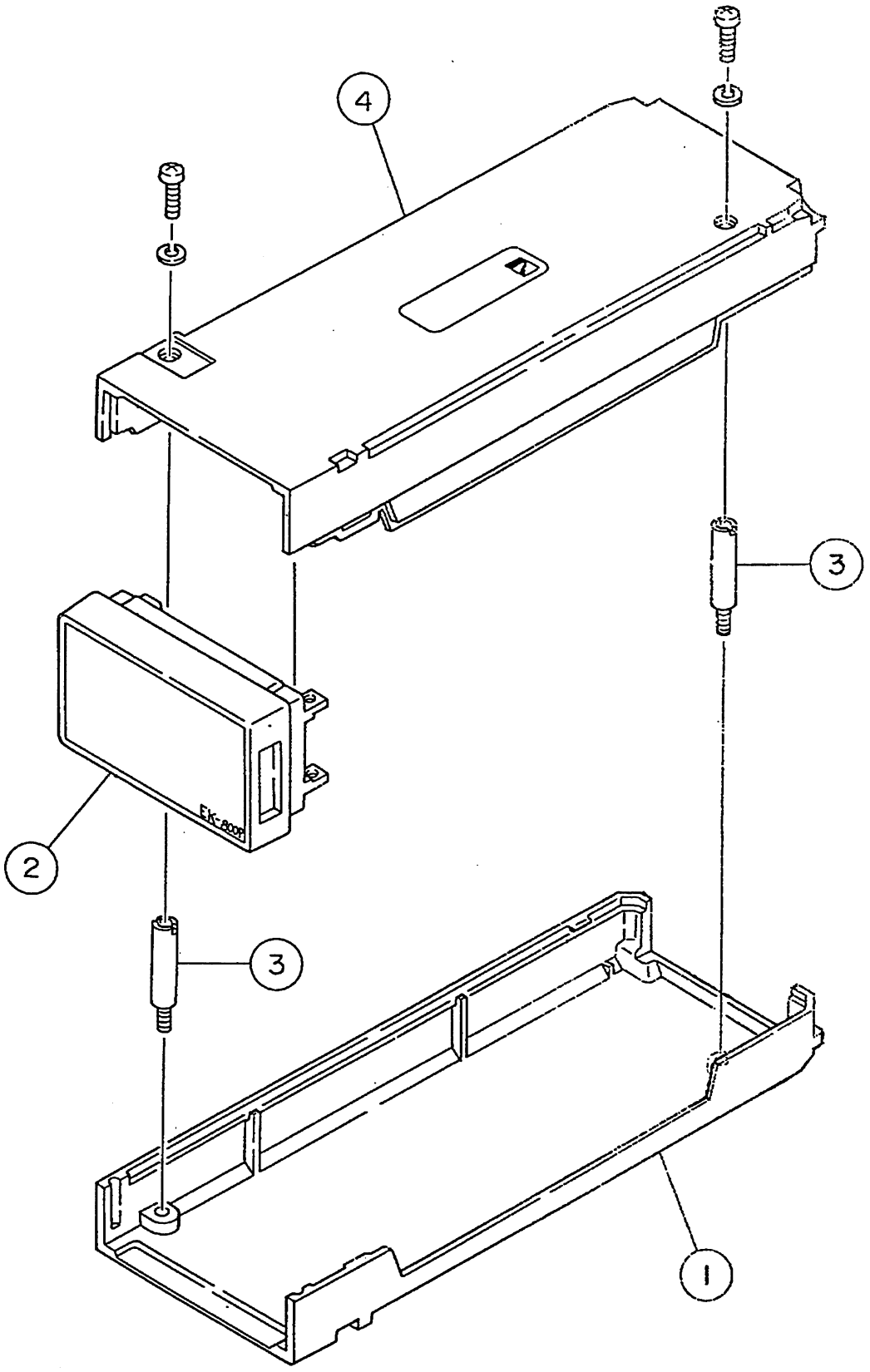
10-6-11 Blank Module, EK-800P

Index	Code No.	Description
1	1112-013569A	Head amp housing (right) アンプユニットケース(右)
2	1112-013587	TEMP Input connector case
3	1114-171376	Housing spacer
4	1112-013533A	Head amp housing (left) アンプユニットケース(左)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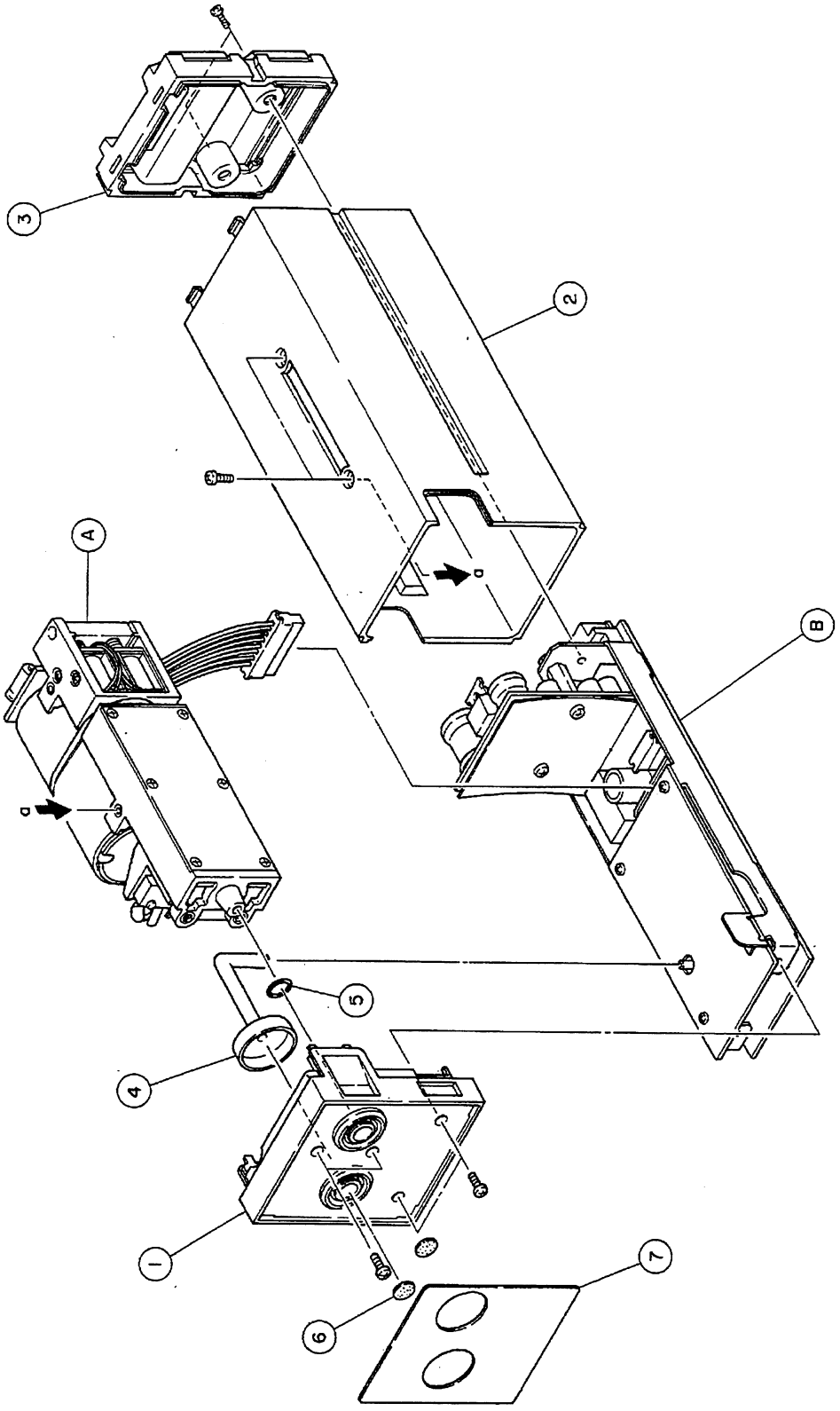
10-6-12 NIBP Head Amplifier, AP-860PA

Index	Code No.	Description	
1	6112-000122A	NIBP main unit	NIBP ユニット本体
2	1112-018243B	NIBP case	NIBP ケース
3	1112-018297D	NIBP unit cover	NIBP ユニットカバ
4	6114-000546	L-shaped tube (sensor)	L形 チューブ (センサ)
5	108893	O Ring P-5	O リング P-5
6	1114-210316	Filter.4	フィルタ.4
7	1124-042229B	Panel for AP-860PA	AP-860PA 表パネル
A	SG-001P	AIR unit	空気系ユニット
B		NIBP Head Amplifier's chassis	NIBP ユニットアンプシャーシ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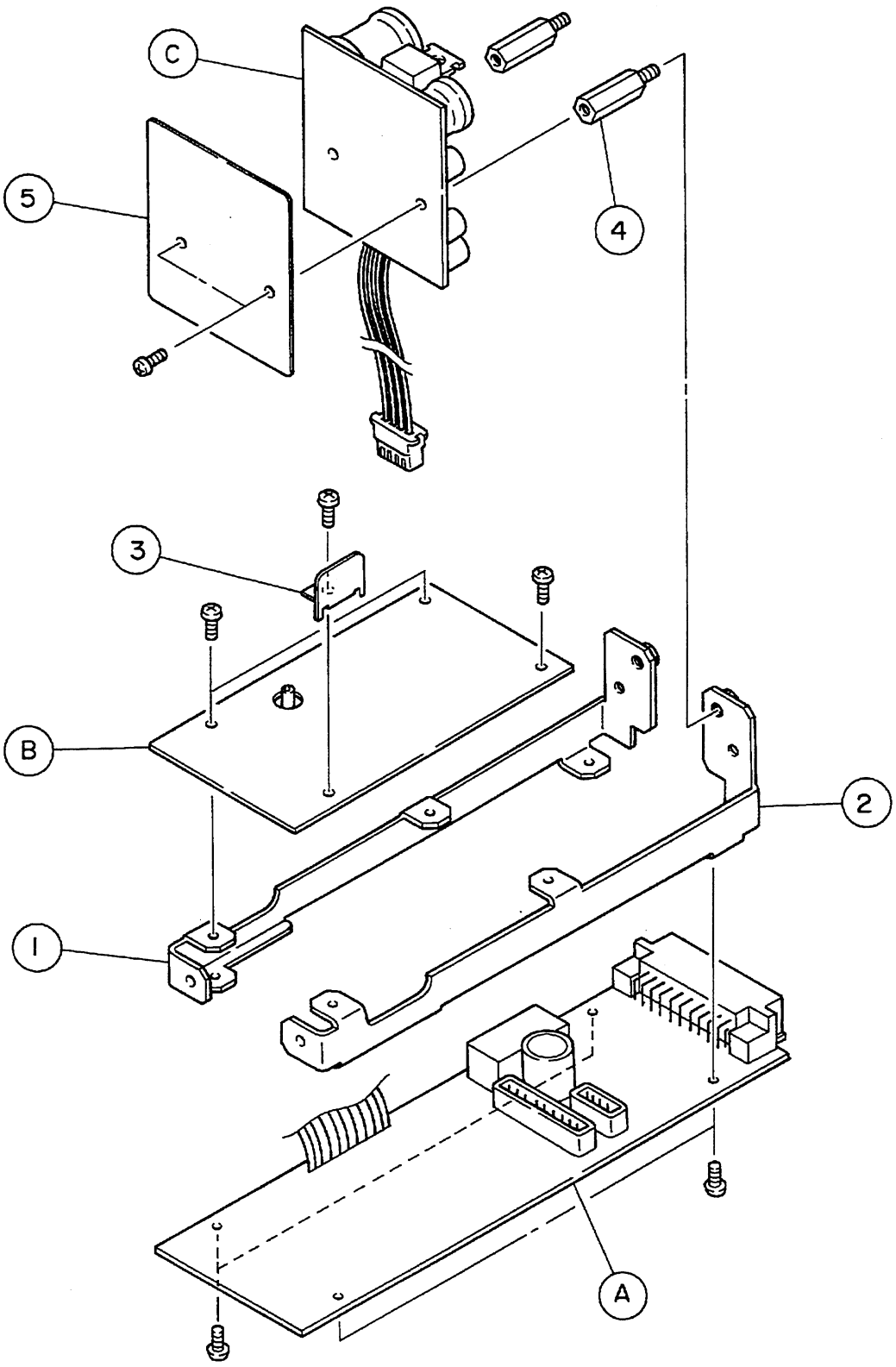
NIBP Head Amplifier's Chassis

Index	Code No.	Description	
1	1114-219896A	PCB board holder.1	P板ホルダ.1
2	1114-219904A	PCB board holder.2	P板ホルダ.2
3	1114-222482	Suspension spring	導通バネ
4	128176	Spacer Bolt (L=14)	間隔ボルド(L=14)
5	1114-221474	Converter Insulation sheet	コンバータ絶縁シート
A	UP-0629	Main board	メイン ボード
B	UP-0630	Sub board	サブ ボード
C	038077	DC/DC Converter	DC/DC コンバータ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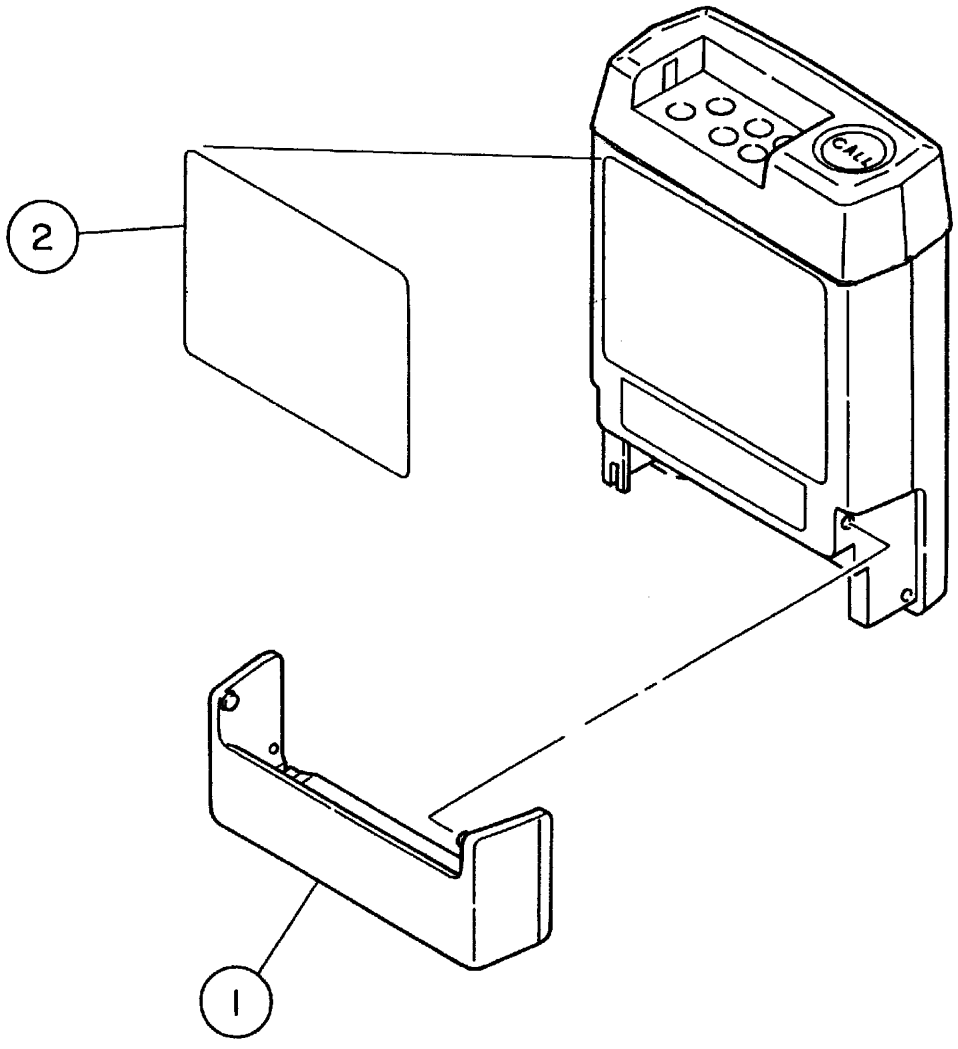
10-7 Transmitter

10-7-1 ZB-810PK/ZB-820PK/ZB-821PK

Index	Code No.	Description	
1	1112-020222	Battery cover	バッテリカバ
2	1124-051585A	ZB-810PK Label	ZB-810PK メイバン
	1124-051834	ZB-820PK Label	ZB-820PK メイバン
	6124-011907	ZB-821PK Label	ZB-821PK メイバン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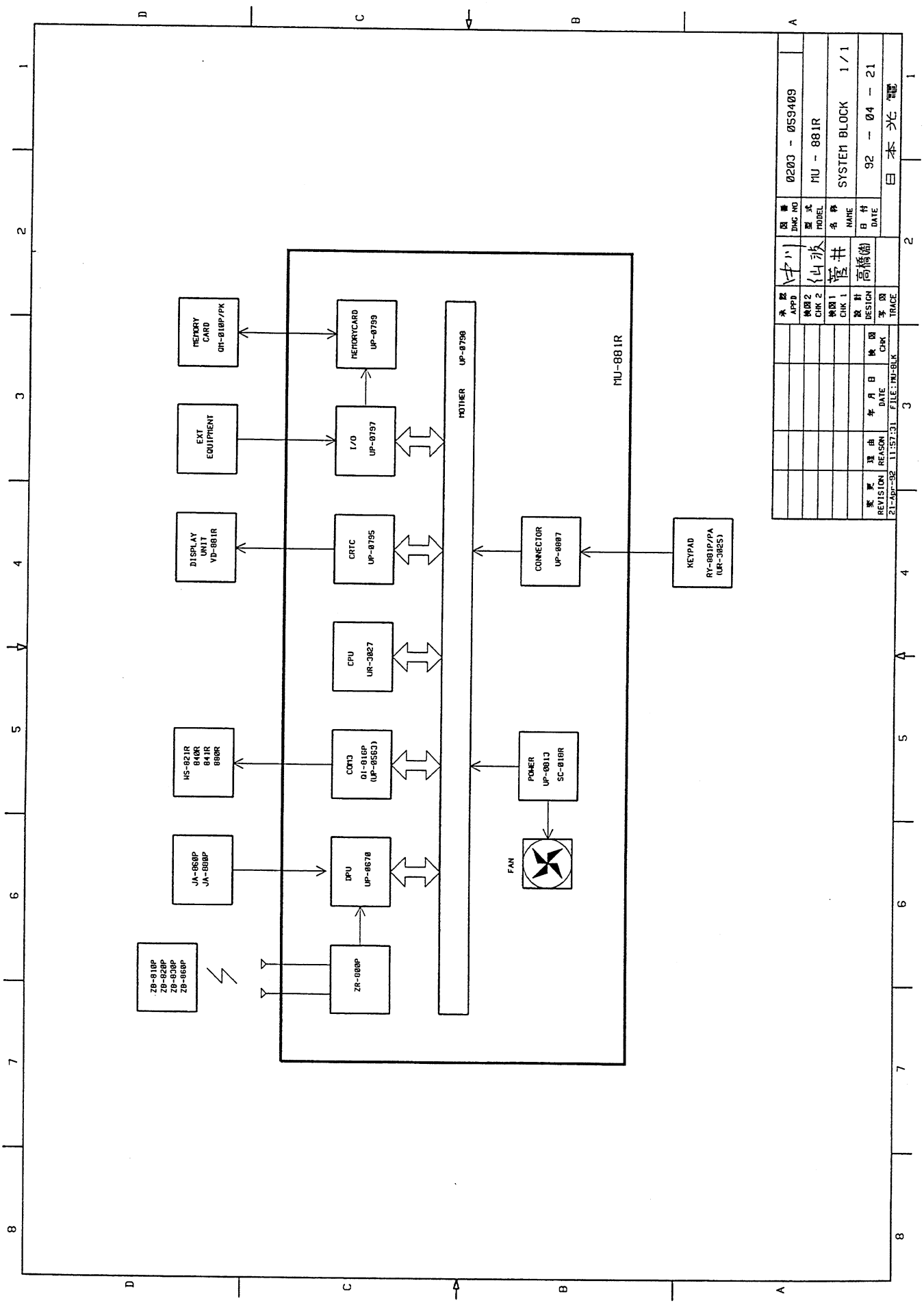
Section 11 BLOCK DIAGRAM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MOTHER UP-8798
MEMORY CARD GM-010P/PK
MEMORYCARD UP-8799
EXT EQUIPMENT
I/O UP-8797
DISPLAY UNIT VD-881R
CRTC UP-8795
CPU UR-3827
CONNECTOR UP-8897
KEYPAD RY-881P/PA (UR-3825)
HS-821R 840R 841R 880R
COM3 01-816P (UP-8563)
POWER UP-881J SC-816R
FAN
JA-860P JA-880P
DPU UP-8678
ZR-080P
ZD-810P ZD-820P ZD-830P ZD-860P
0203 - 059409
MU - 881R
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日本光電
REVISION 21-Apr-92
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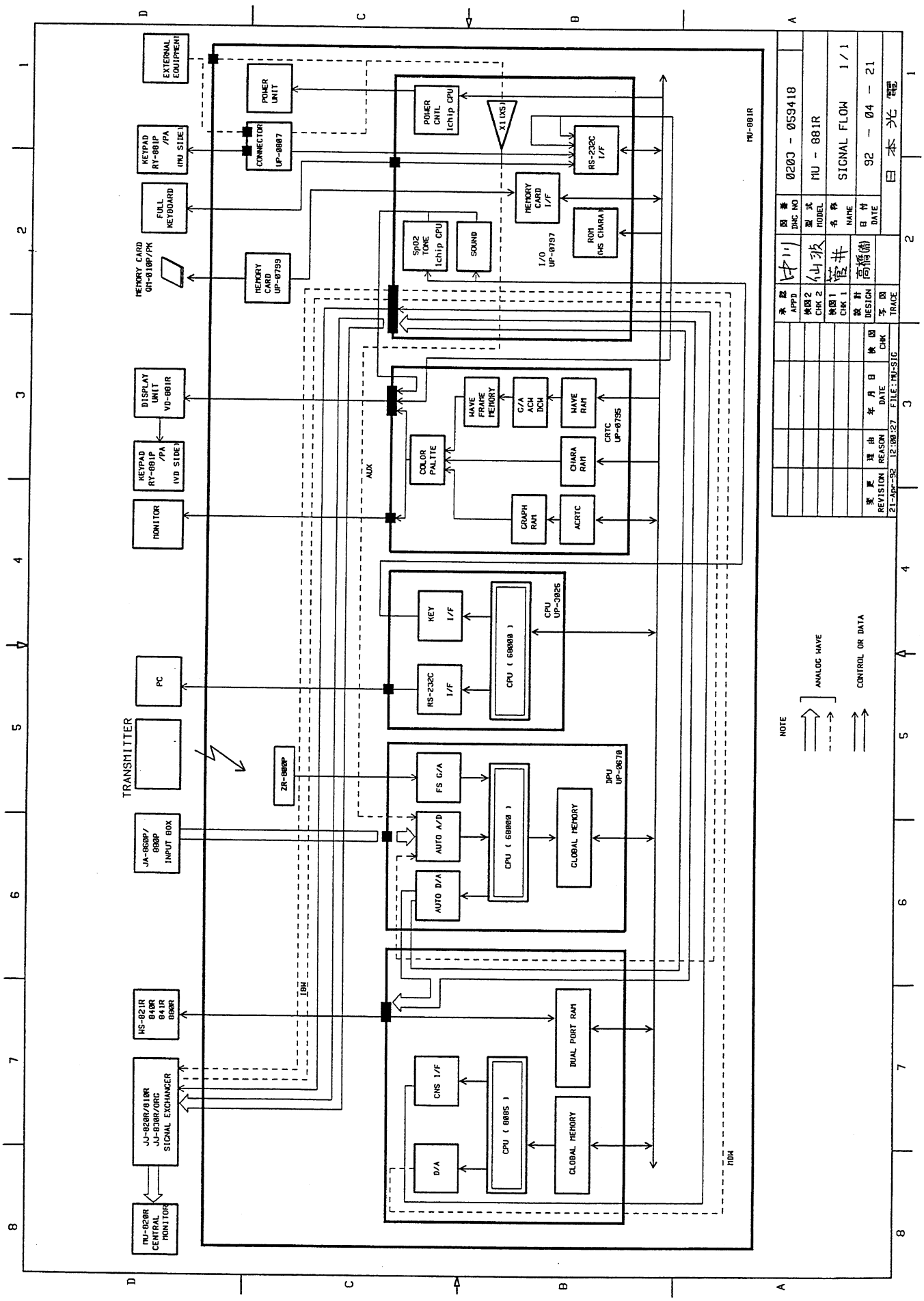

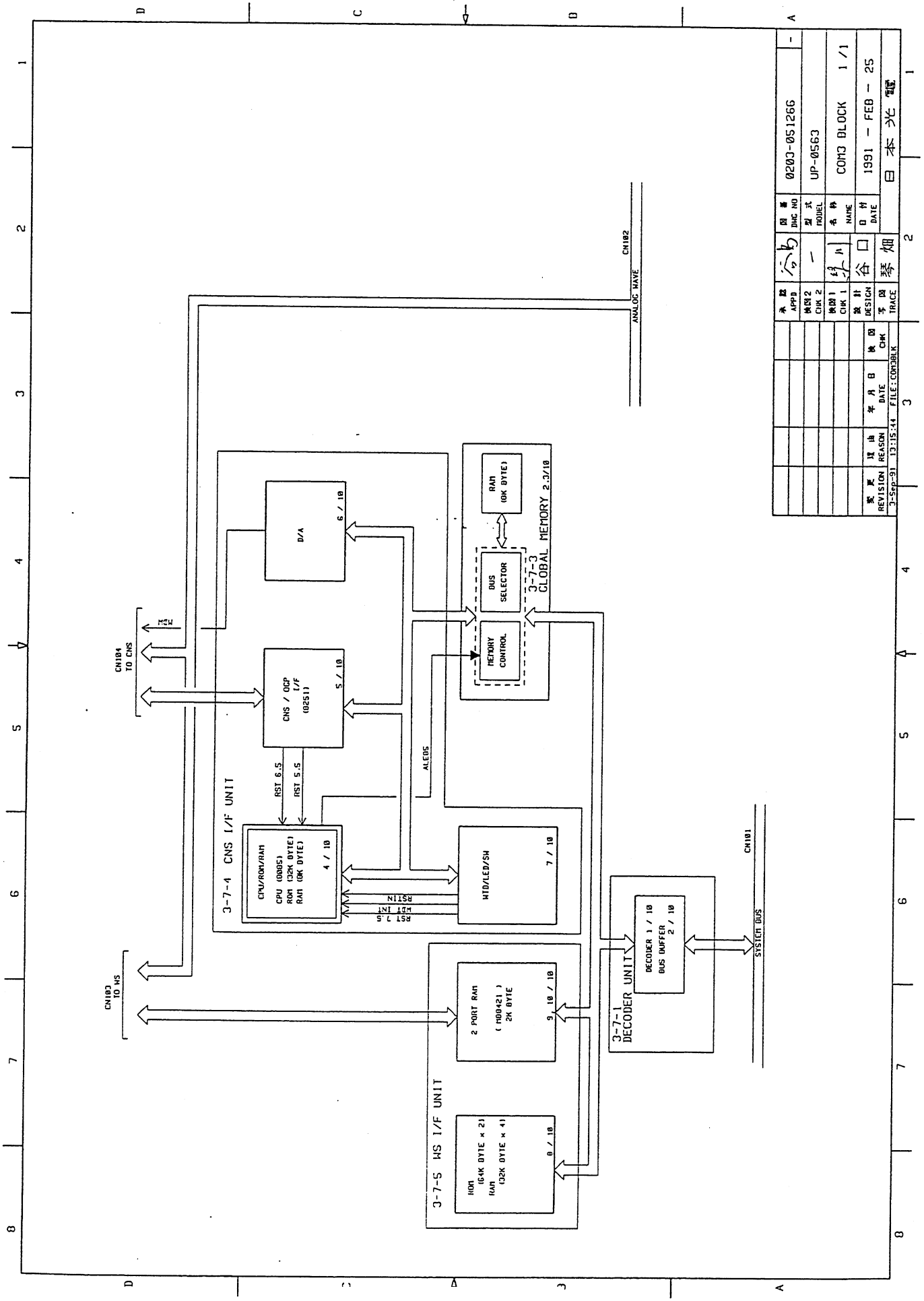
3-7-4 CNS I/F UNIT
CPU/ROM/RAM
CPU (8085)
ROM (32K BYTE)
RAM (8K BYTE)
4 / 10
CNS / OCP I/F (8251)
5 / 10
D/A
6 / 10
RST 6.5
RST 5.5
RST7.5
INT
RSTIN
WTD/LED/SW
7 / 10
3-7-3 GLOBAL MEMORY 2.3/10
MEMORY CONTROL
BUS SELECTOR
RAM (8K BYTE)
ALE0S
3-7-5 WS I/F UNIT
2 PORT RAM
(M00421)
2K BYTE
9, 10 / 10
ROM (64K BYTE × 2)
RAM (32K BYTE × 4)
8 / 10
3-7-1 DECODER UNIT
DECODER 1 / 10
BUS BUFFER 2 / 10
CN102
ANALOG WAVE
CN104 TO CNS
CN103 TO WS
CN101
SYSTEM BUS
0203-051266
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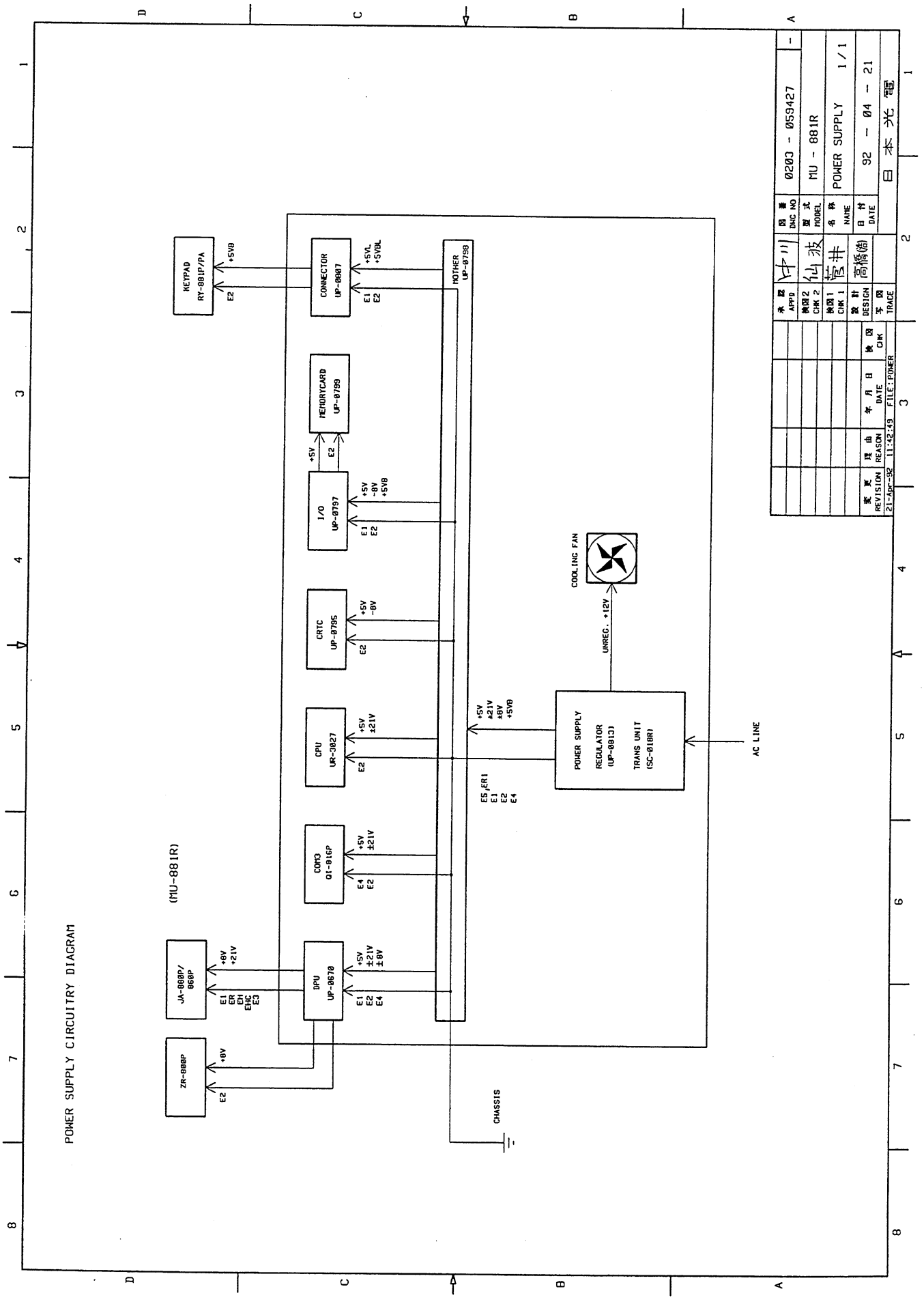
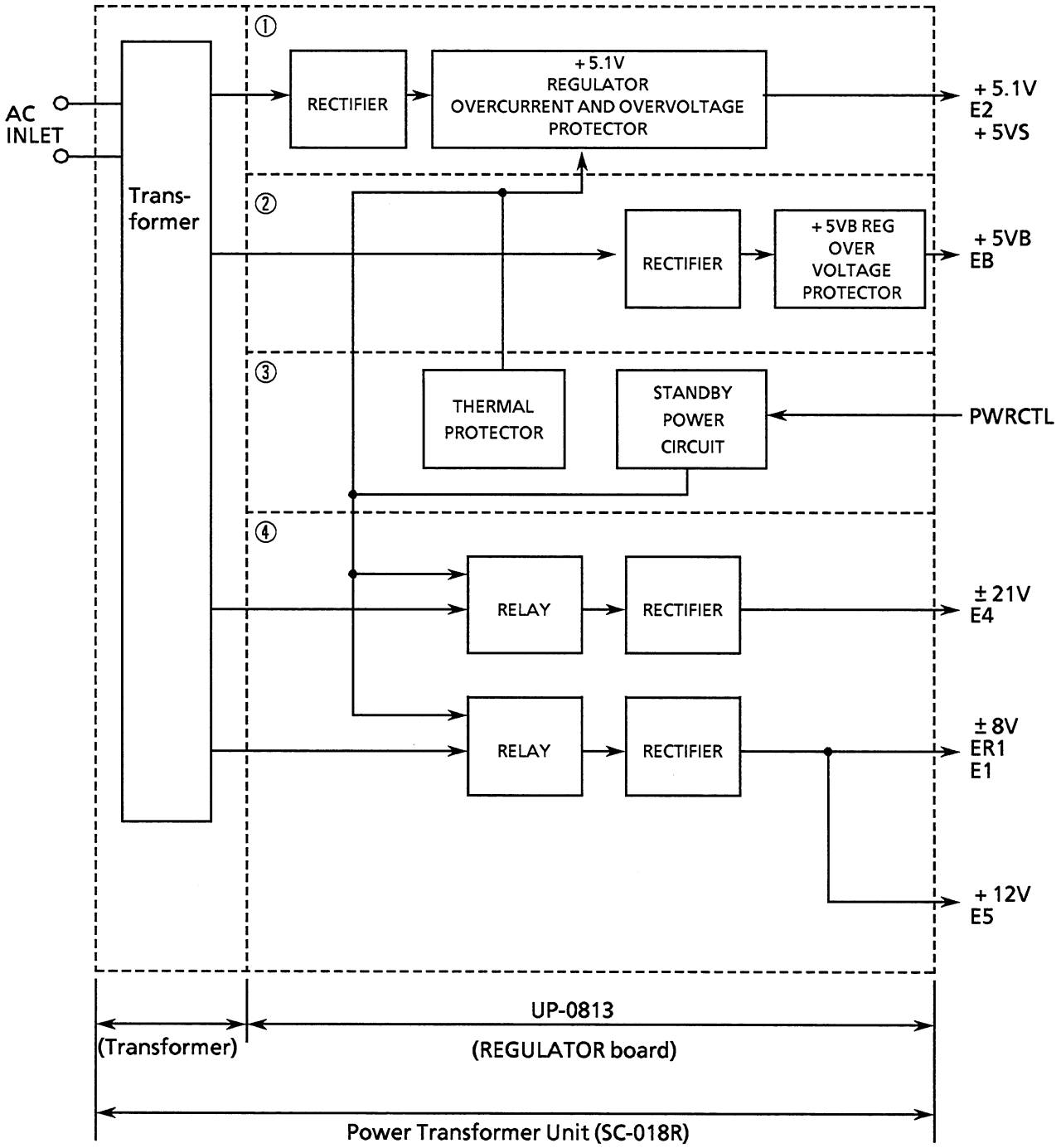
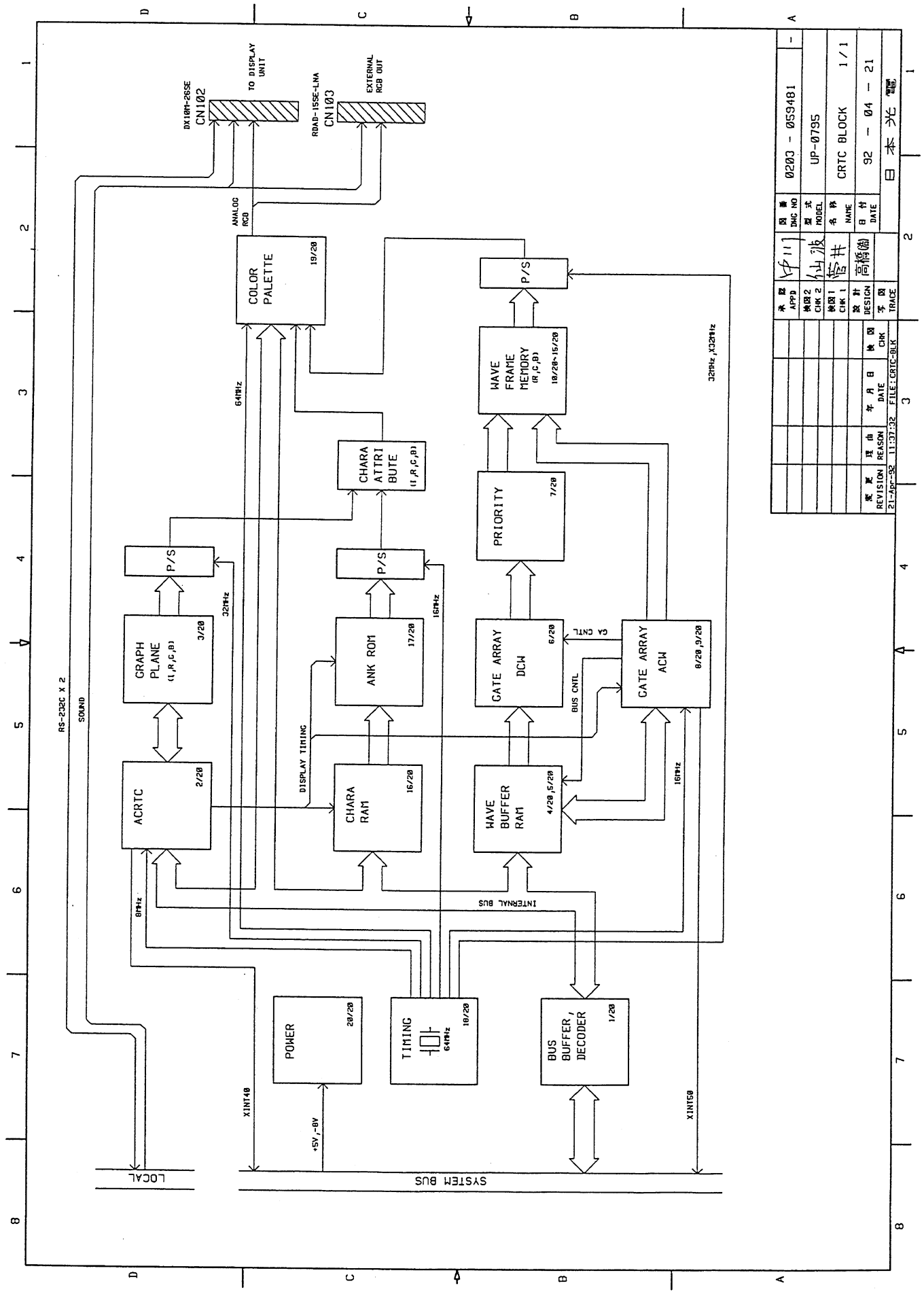
11. BLOCK DIAGRAM

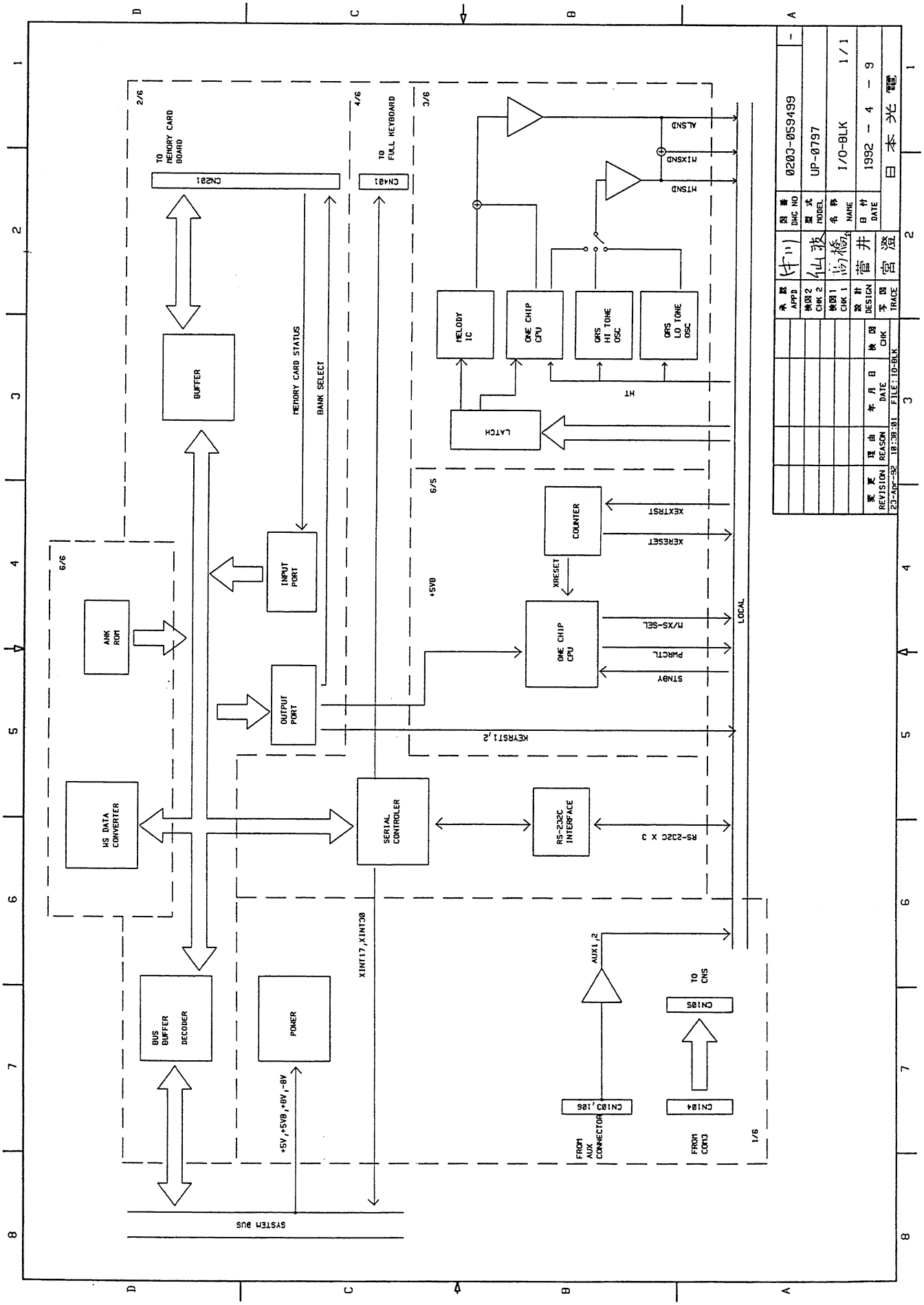


Power Tranfrormer Unit, SC-018R



11. BLOCK DIAGRAM

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CN201
TO FULL KEYBOARD
CN431
BUFFER
MEMORY CARD STATUS
BANK SELECT
ALSND
MIXSND
MTSND
MELODY IC
ONE CHIP CPU
ORS HI TONE OSC
ORS LO TONE OSC
MT
LATCH
COUNTER
XEXTRST
XERESET
XRESET
+5VB
INPUT PORT
ANK ROM
OUTPUT PORT
M/XS-SEL
PWRCTL
STNBY
ONE CHIP CPU
LOCAL
KEYRST1,2
HS DATA CONVERTER
SERIAL CONTROLER
RS-232C INTERFACE
RS-232C X 3
XINT17,XINT30
AUX1,2
TO CNS
CN105
CN103,106
CN104
FROM AUX CONNECTOR
FROM CONS
BUS BUFFER DECODER
POWER
+5V,+5VB,+8V,-8V
SYSTEM BUS
1/6
2/6
3/6
4/6
5/6
6/6
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UP-0797
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1992 - 4 - 9
日本光電
REVISION
REASON
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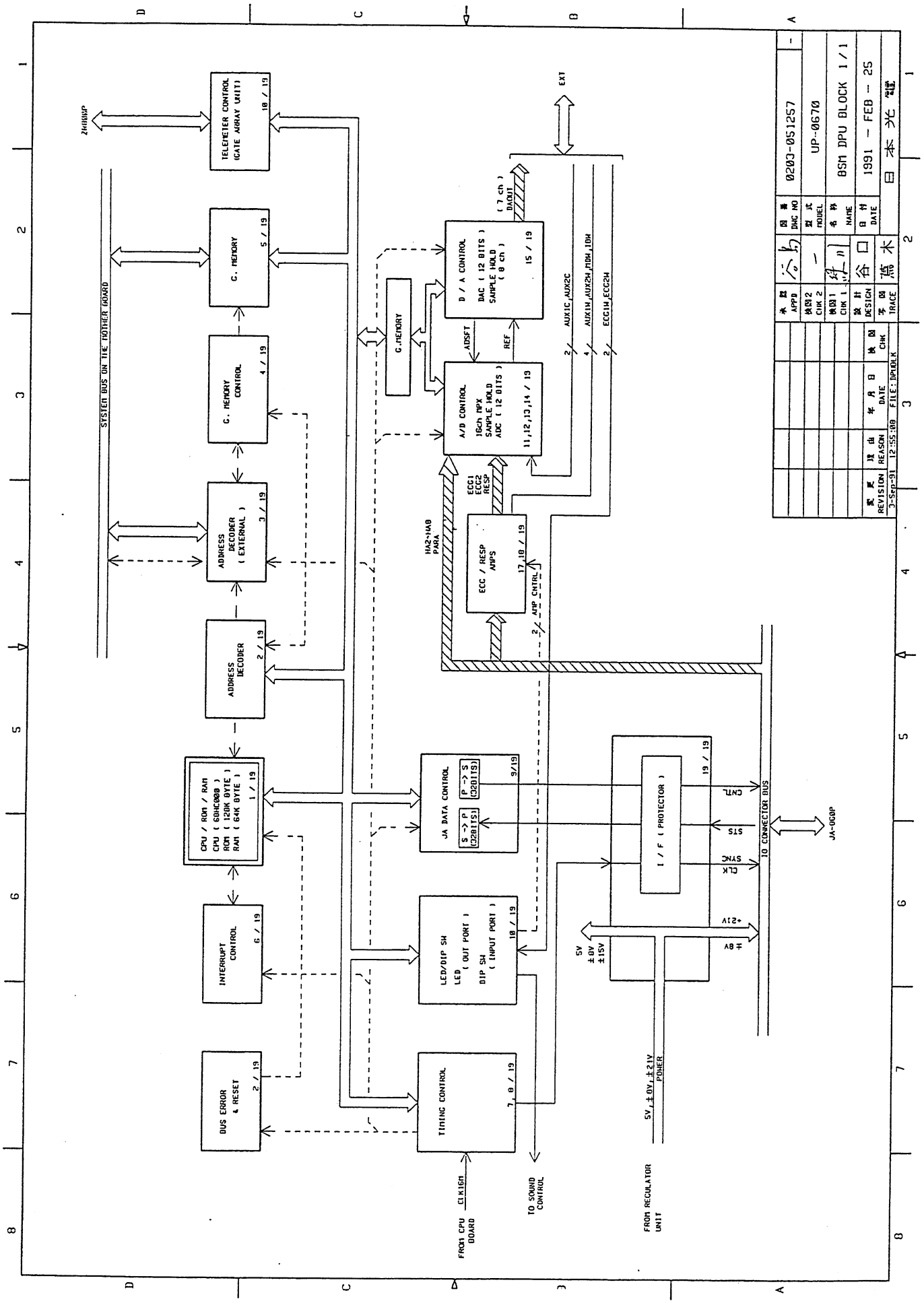
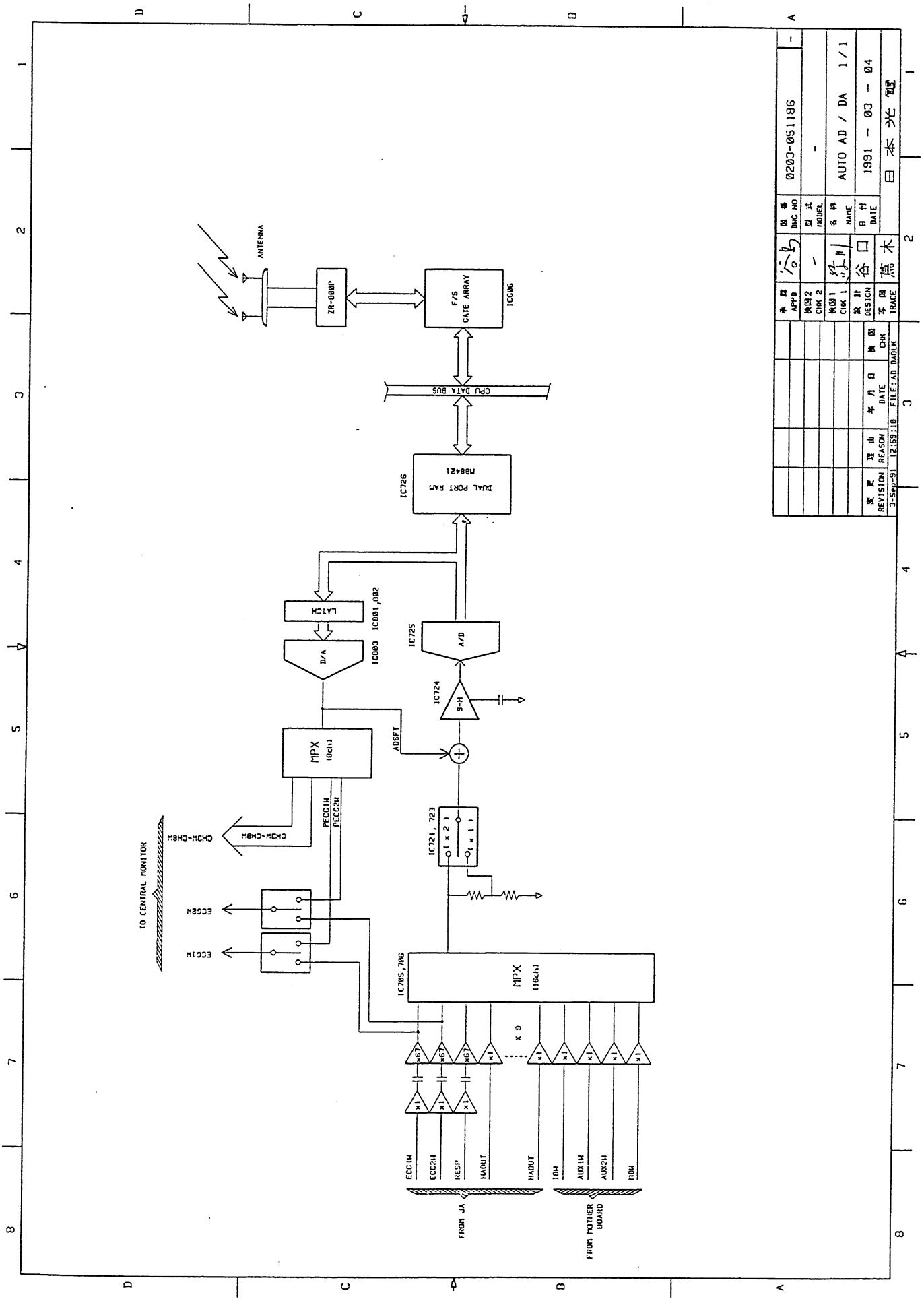
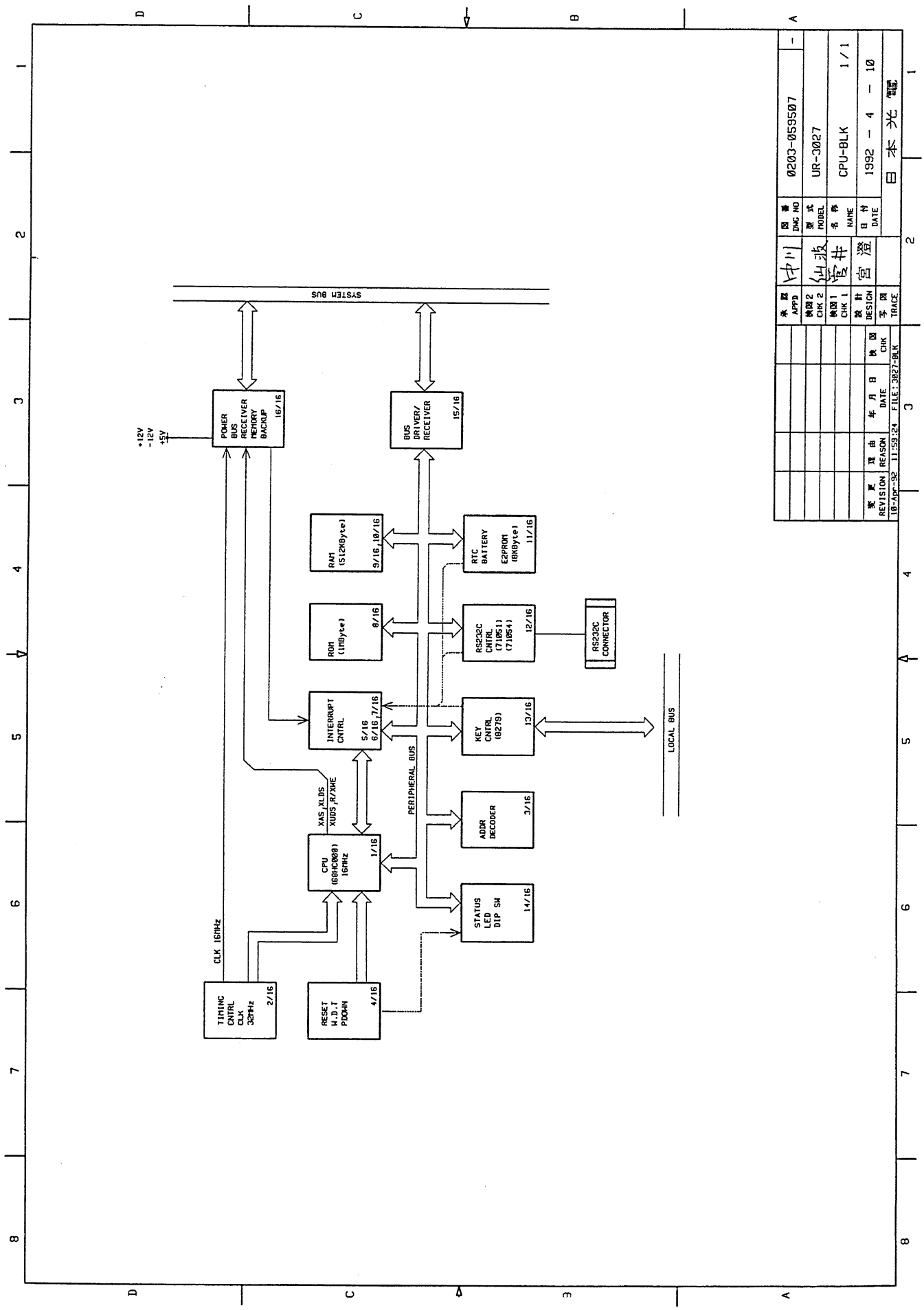
23-Apr-92 10:38:01

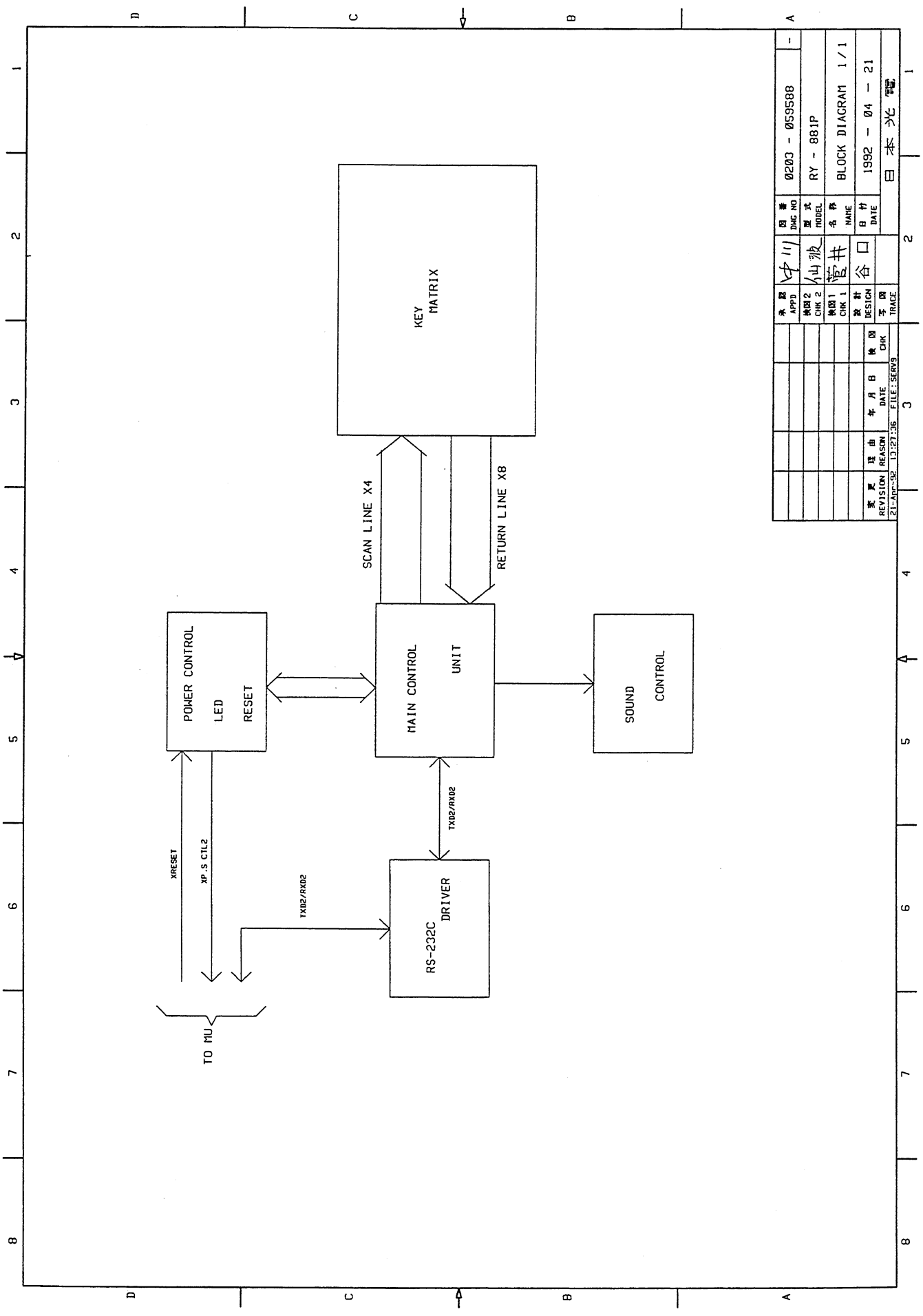
11. BLOCK DIAGRAM




ANTENNA
ZR-000P
F/S GATE ARRAY
IC006
CPU DATA BUS
DUAL PORT RAM
M88421
IC726
LATCH
IC001,002
D/A
IC003
A/D
IC725
S-H
IC724
MPX (8ch)
ADSFT
IC721, 723
(1 x 2)
(1 x 1)
CH1H~CH8H
CH1H~CH8H
PECG1H
PECG2H
TO CENTRAL MONITOR
ECG2H
ECG1H
IC705,706
MPX (16ch)
x 9
x1
ECG1H
ECG2H
RESP
HAOUT
HAOUT
IOH
AUX1H
AUX2H
MOH
FROM JA
FROM MOTHER BOARD
APP'D
CHK 2
CHK 1
DESIGN
TRACE
CHK
DWG NO
0203-051186
MODEL
-
NAME
AUTO AD / DA 1/1
DATE
1991 - 03 - 04
日本光電
REVISION
REASON
DATE
CHK
3-Sep-91
12:59:18
FILE:AD DARLK

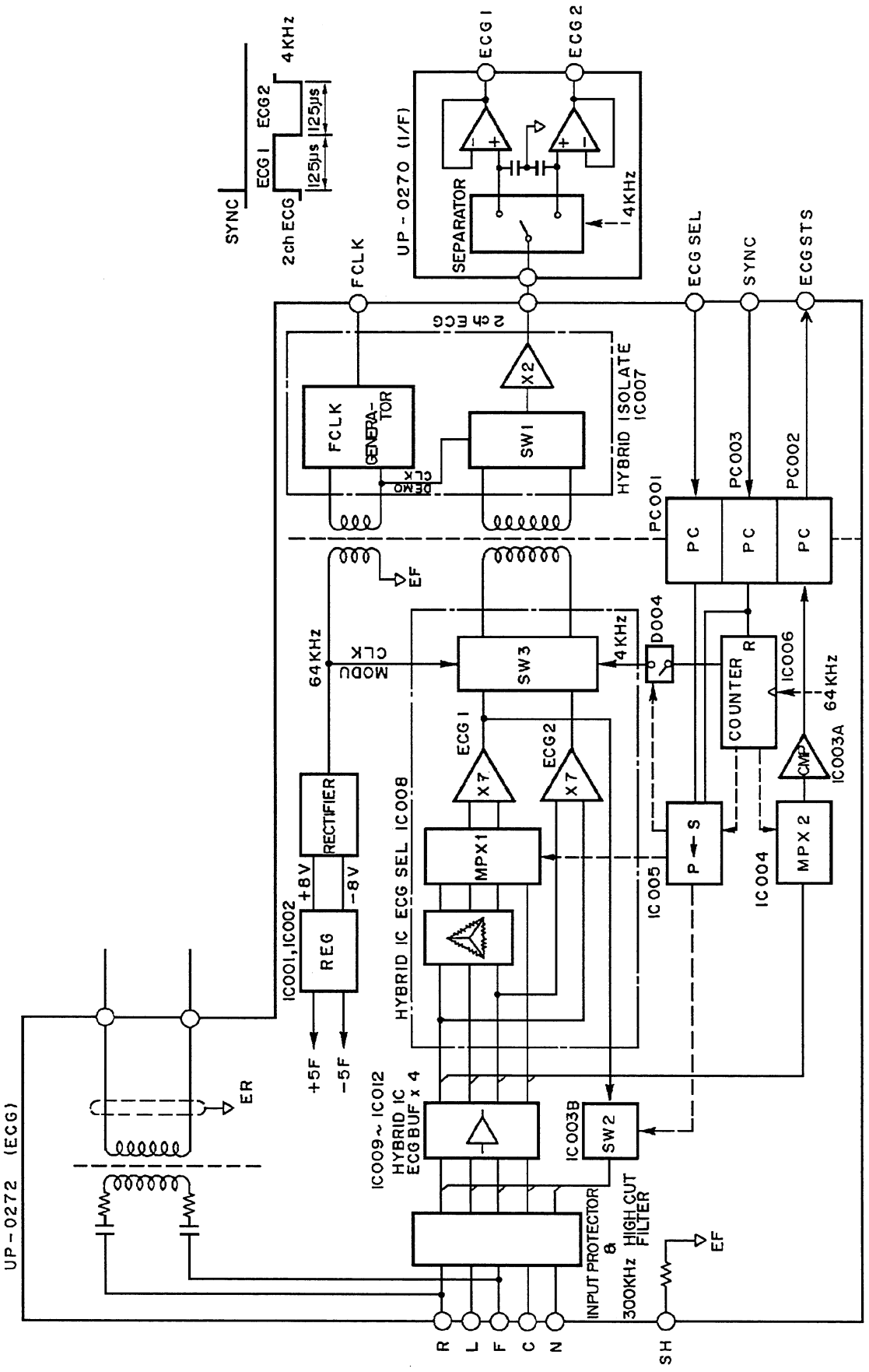
11. BLOCK DIAGRAM



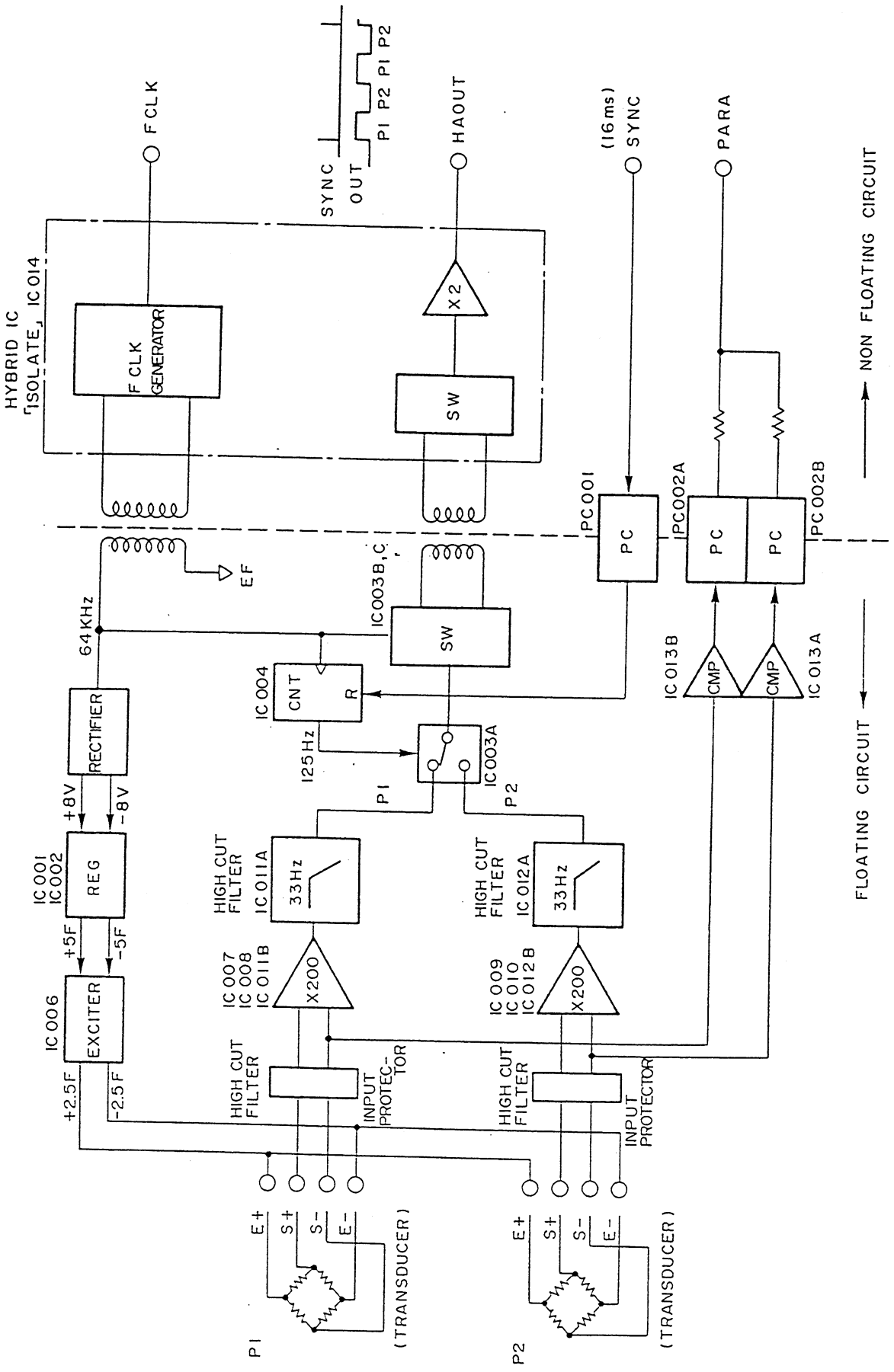

KEY MATRIX
SCAN LINE X4
RETURN LINE X8
POWER CONTROL
LED
RESET
MAIN CONTROL UNIT
SOUND CONTROL
TXD2/RXD2
XRESET
XP.S CTL2
TXD2/RXD2
RS-232C DRIVER
TO MU
0203 - 059588
RY - 881P
BLOCK DIAGRAM 1/1
1992 - 04 - 21
日本光電

11. BLOCK DIAGRAM

ECG/Respiration Head Amp, AC-800P

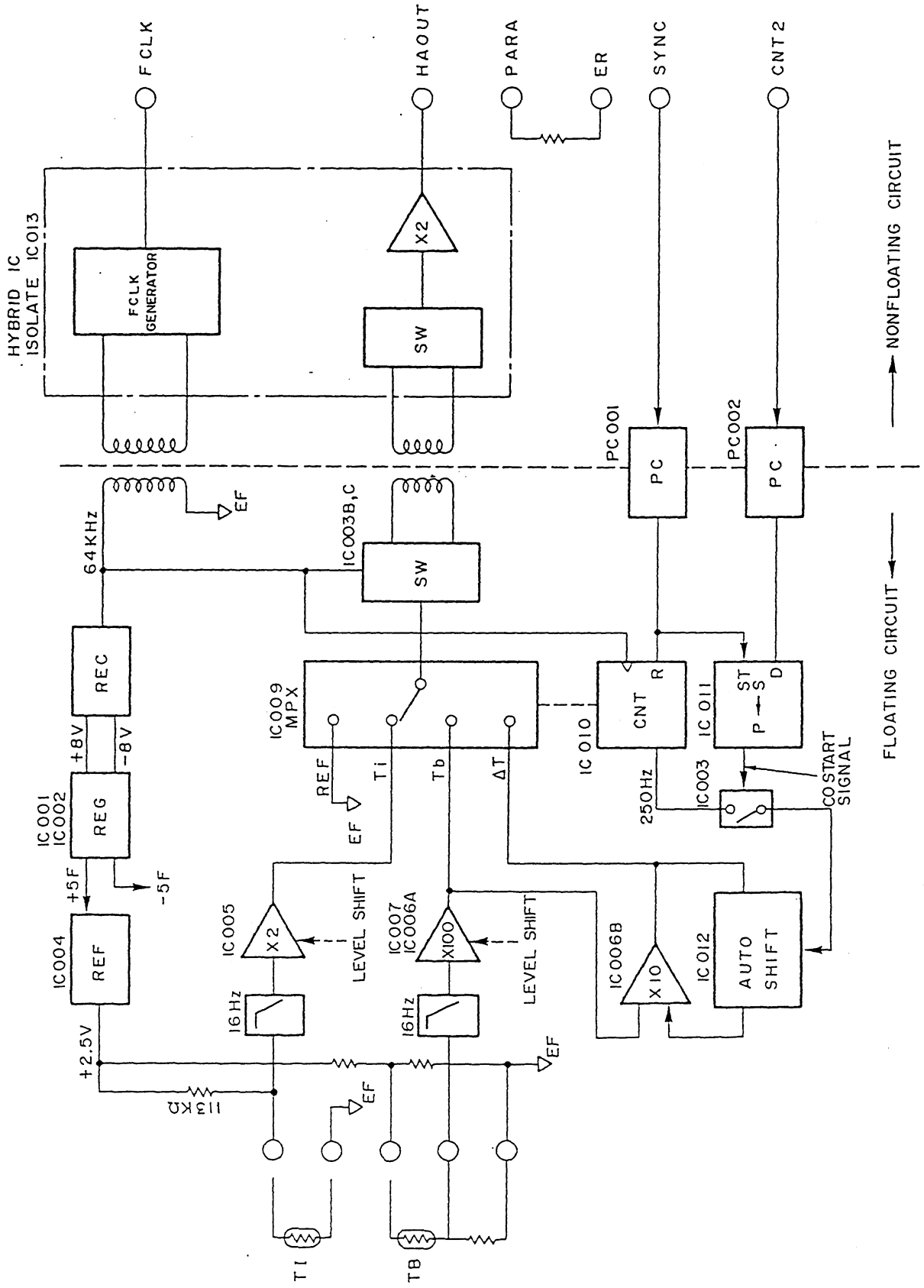


PRESS Head Amp, AP-800PA

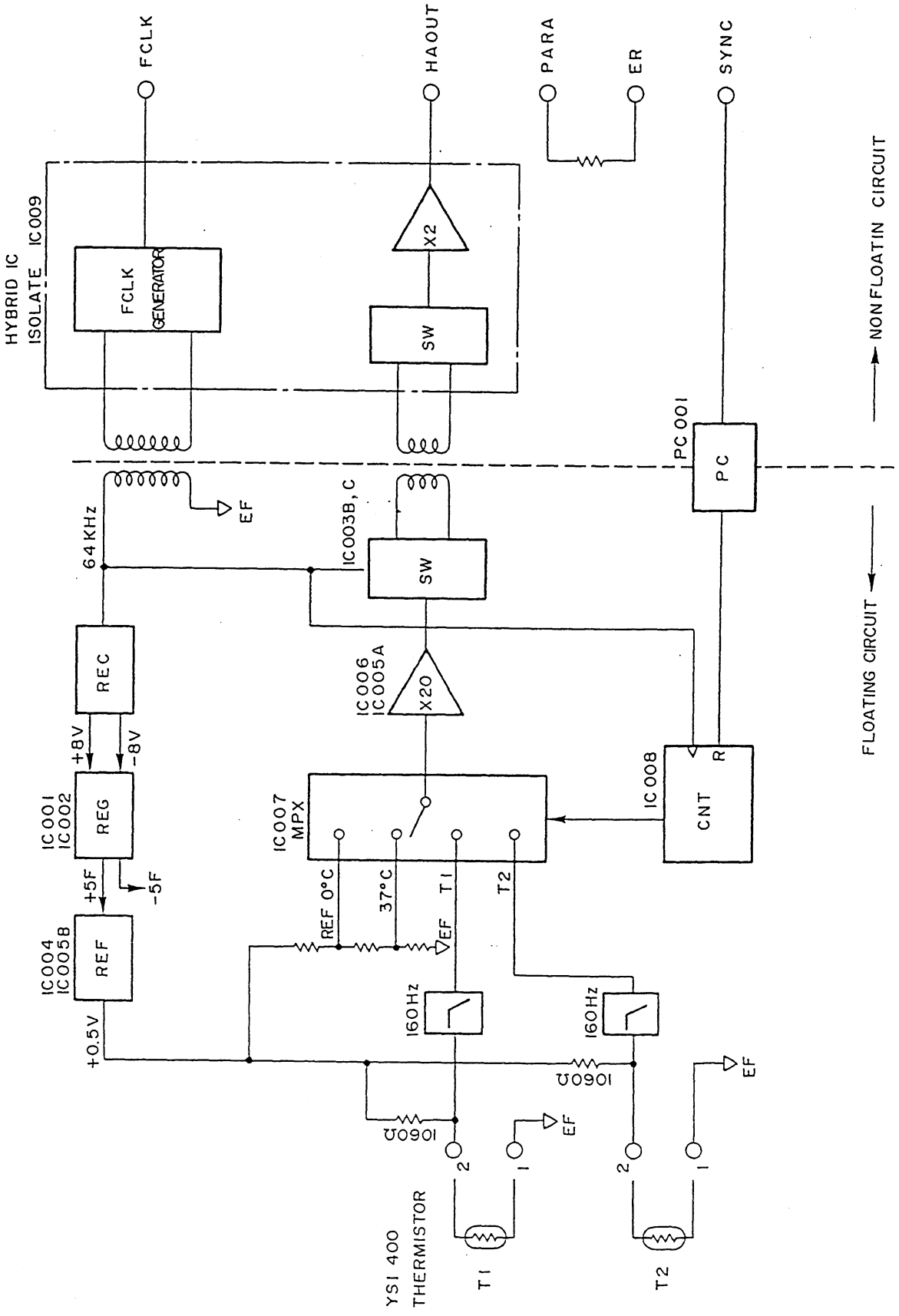


11. BLOCK DIAGRAM

CO Head Amp, AH-800PA

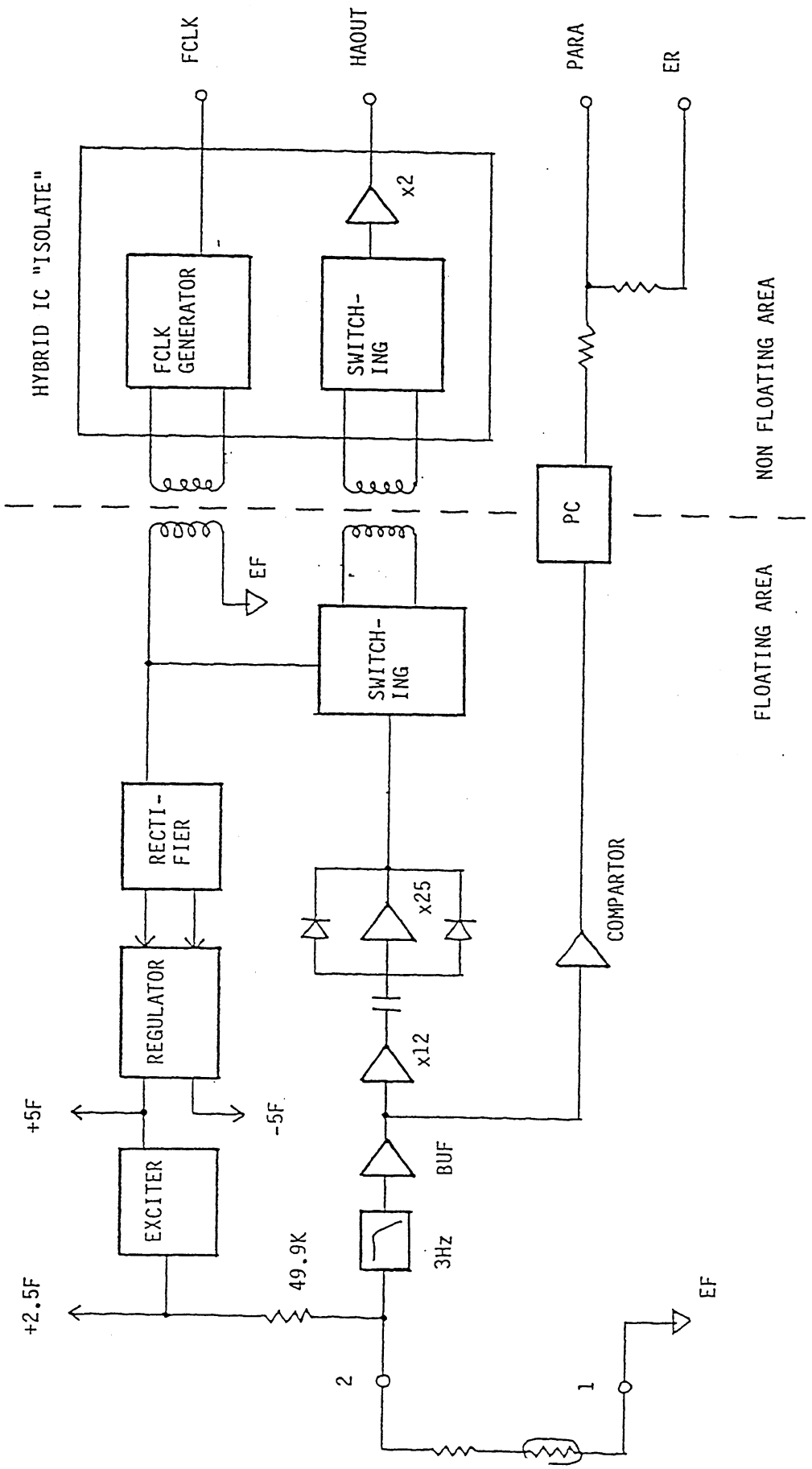


TEMP Head Amp, AW-800PA

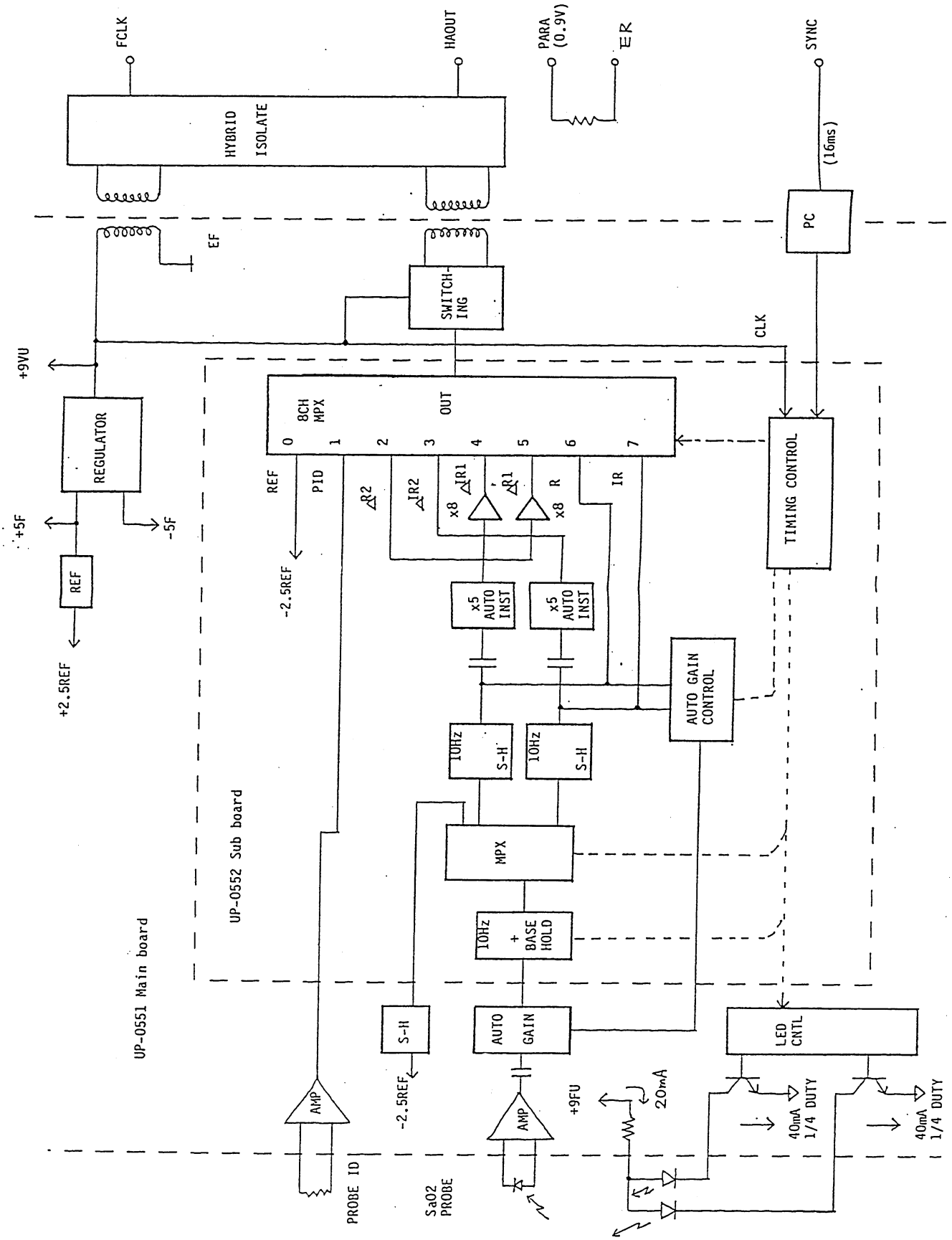


11. BLOCK DIAGRAM

RESPIRATION Head Amp, AR-800PA

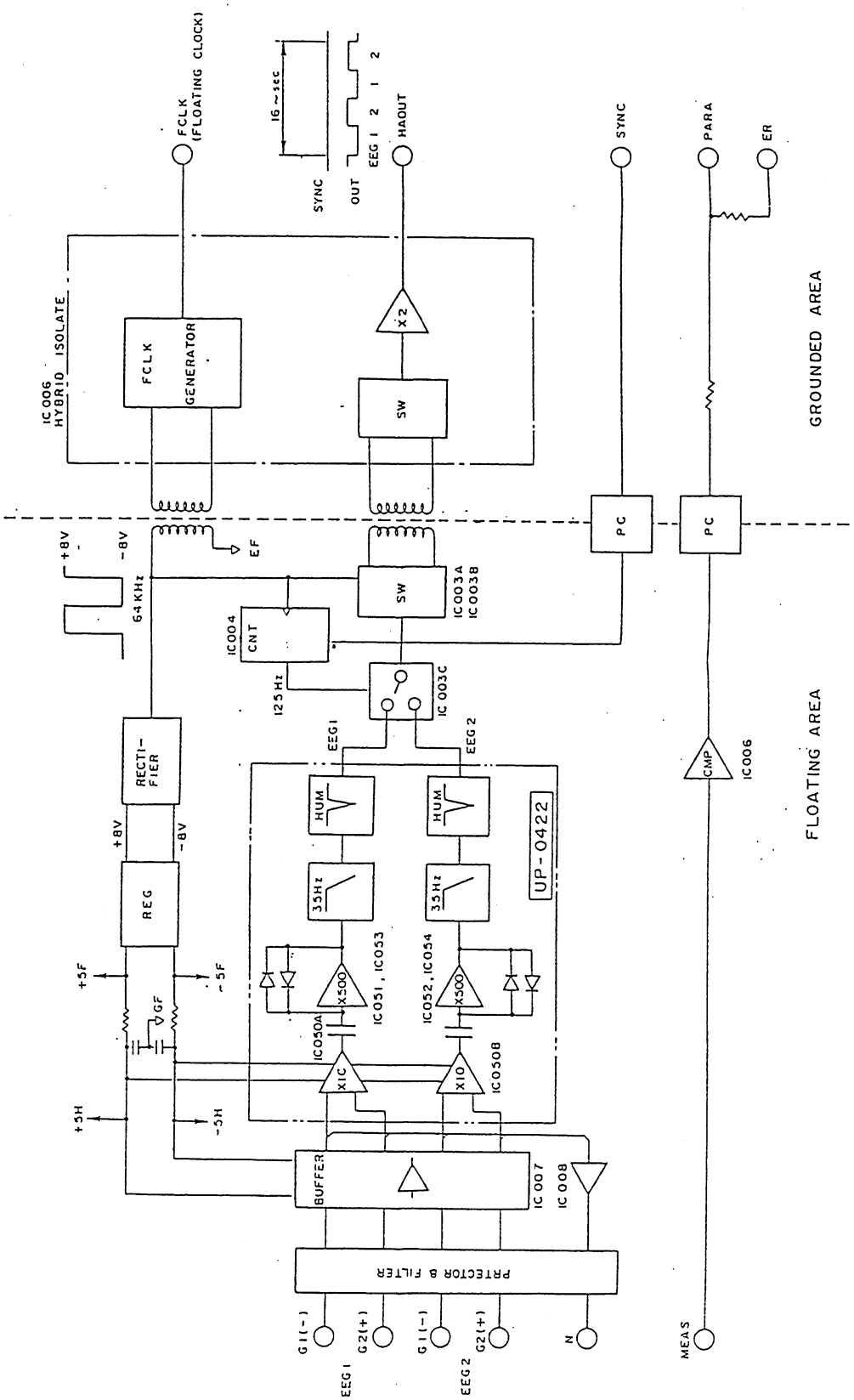


SpO_2 Head Amp, AL-800PA

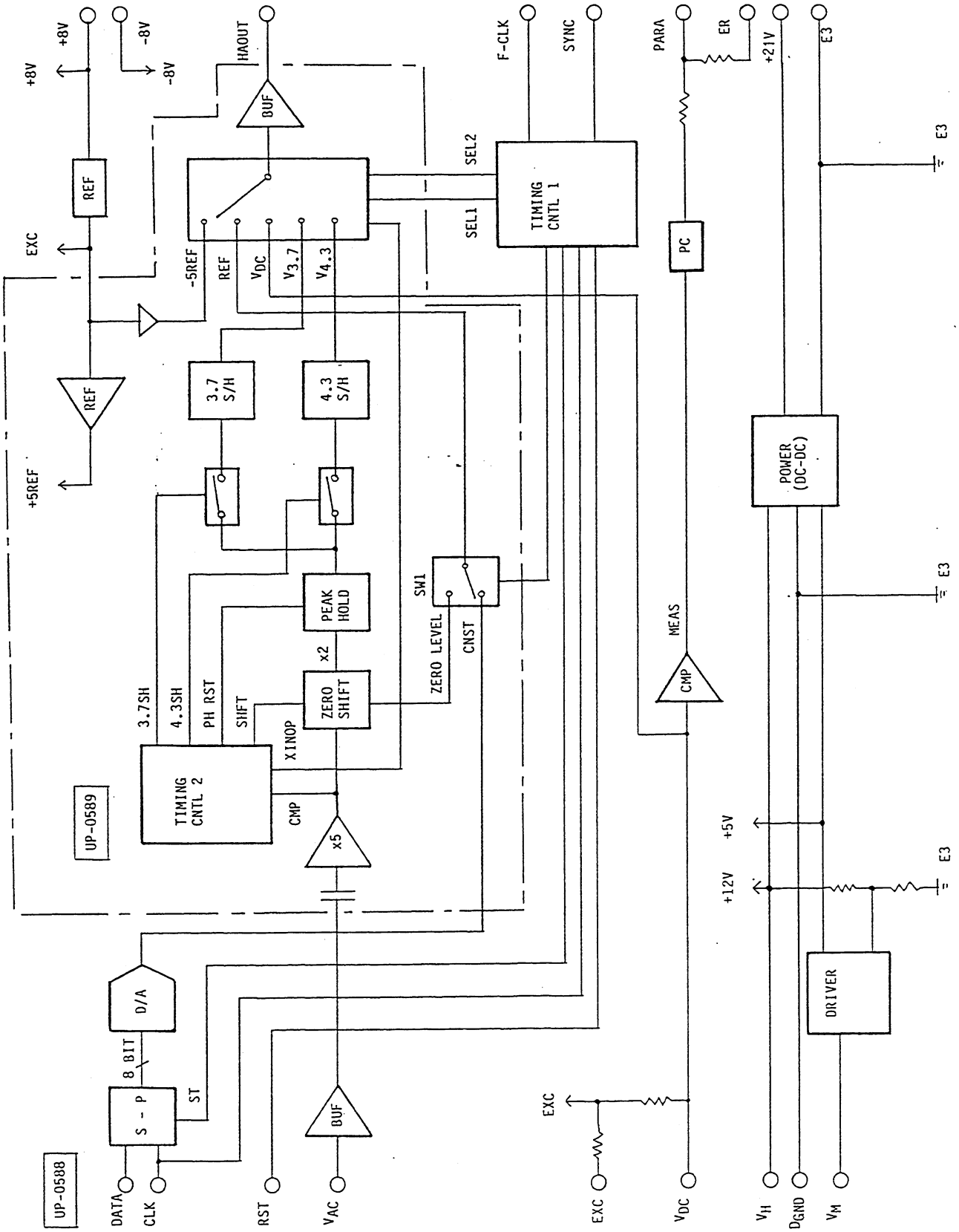


11. BLOCK DIAGRAM

EEG Head Amp, AE-800PA

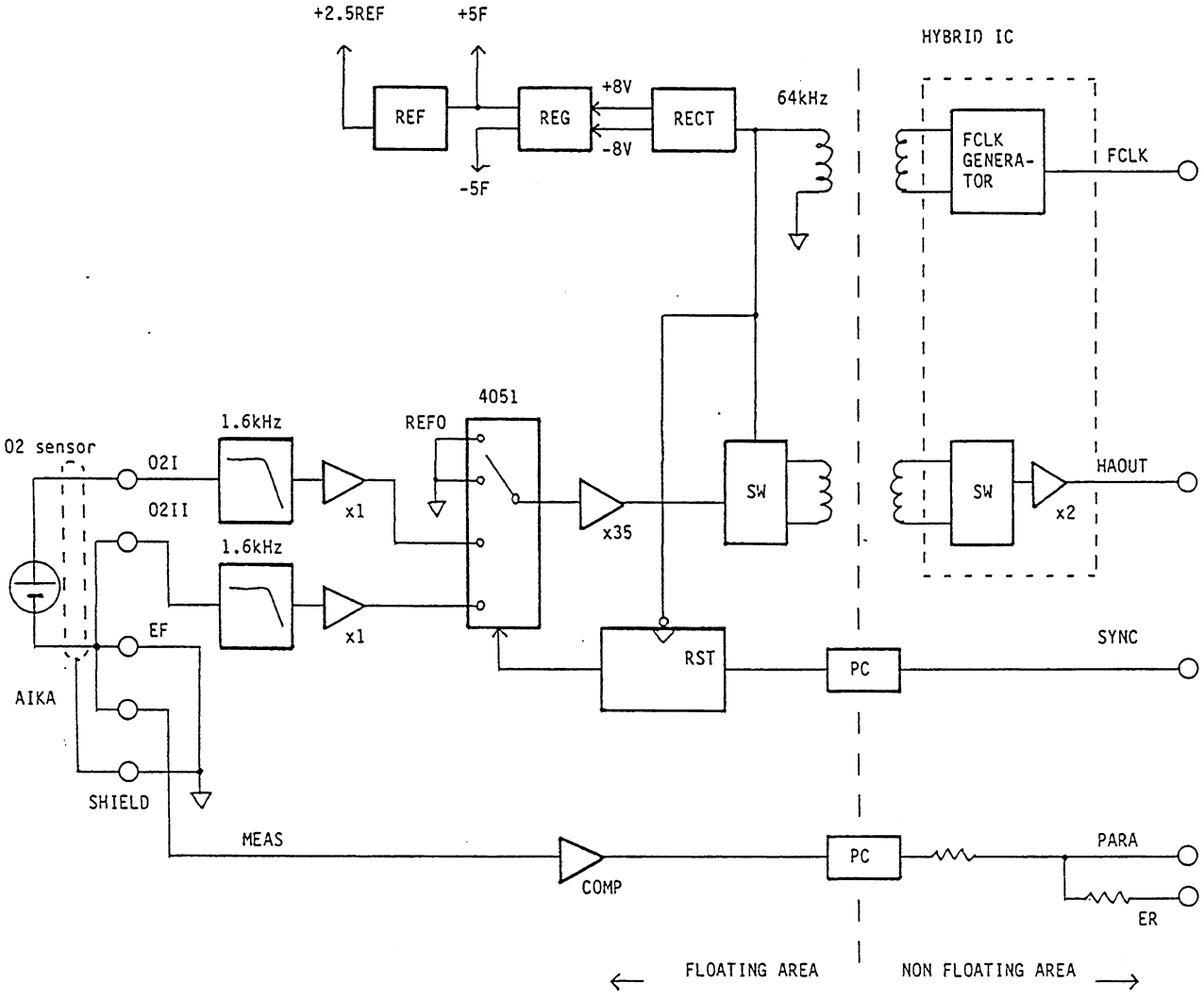


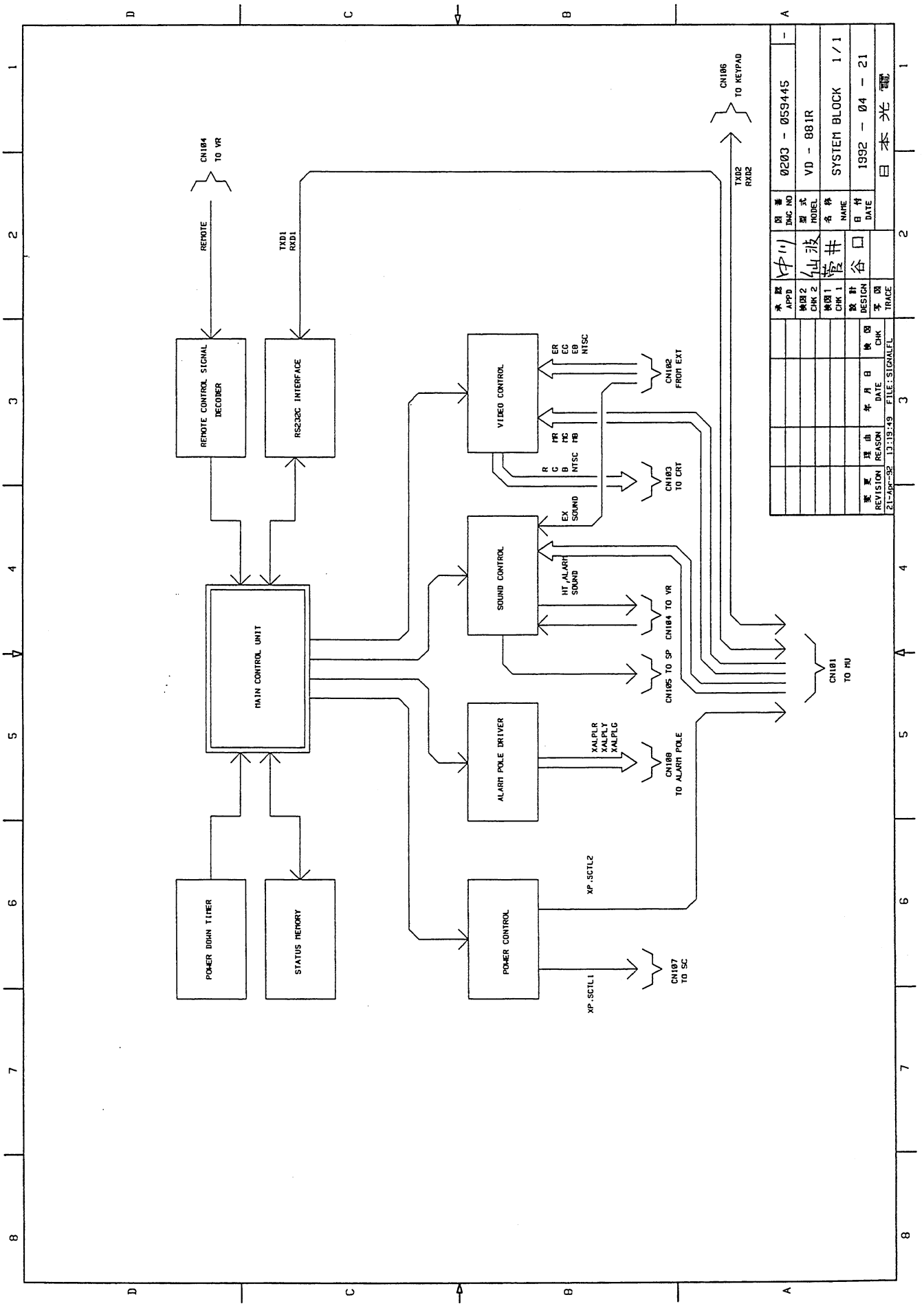
CO_2 Head Amp, AG-800PA



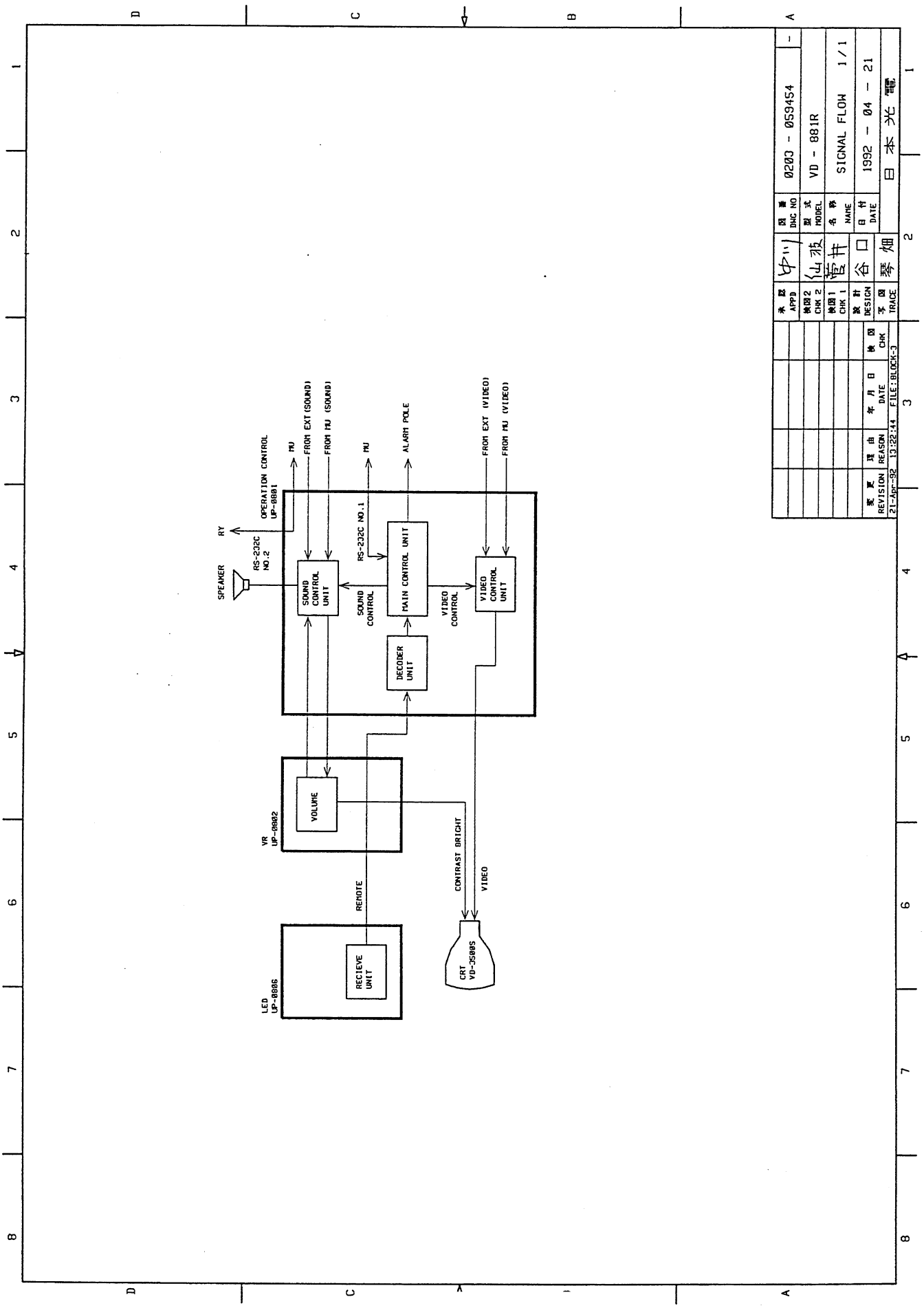
11. BLOCK DIAGRAM

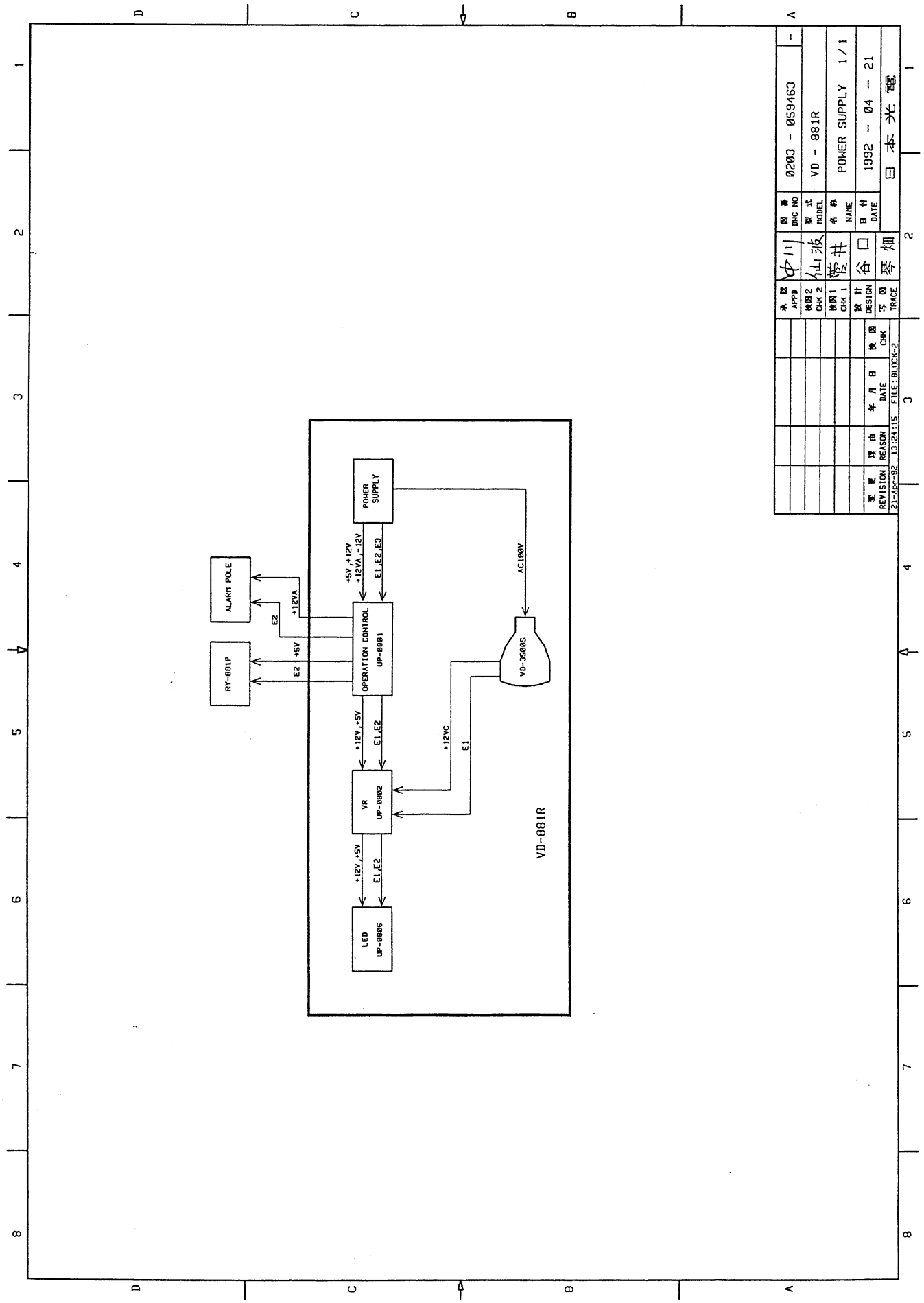
O_2 Head Amp, AG-820PA




REMOTE CONTROL SIGNAL DECODER
RS232C INTERFACE
MAIN CONTROL UNIT
POWER DOWN TIMER
STATUS MEMORY
VIDEO CONTROL
SOUND CONTROL
ALARM POLE DRIVER
POWER CONTROL
CN104 TO VR
REMOTE
TXD1 RXD1
CN106 TO KEYPAD
TXD2 RXD2
ER EG EB NTSC
CN102 FROM EXT
R G B NTSC
CN103 TO CRT
EX SOUND
HT_ALARM SOUND
CN104 TO VR
CN105 TO SP
CN101 TO MU
XALPLR XALPLY XALPLG
CN108 TO ALARM POLE
XP.SCTL2
XP.SCTL1
CN107 TO SC
0203 - 059445
VD - 881R
SYSTEM BLOCK 1/1
1992 - 04 - 21
日本光
REVISION
DESIGN
CHK 1
CHK 2
APPD
DATE
NAME
MODEL
DWG NO
TRACE
21-Apr-92 13:19:49 FILE: SIGNALFL

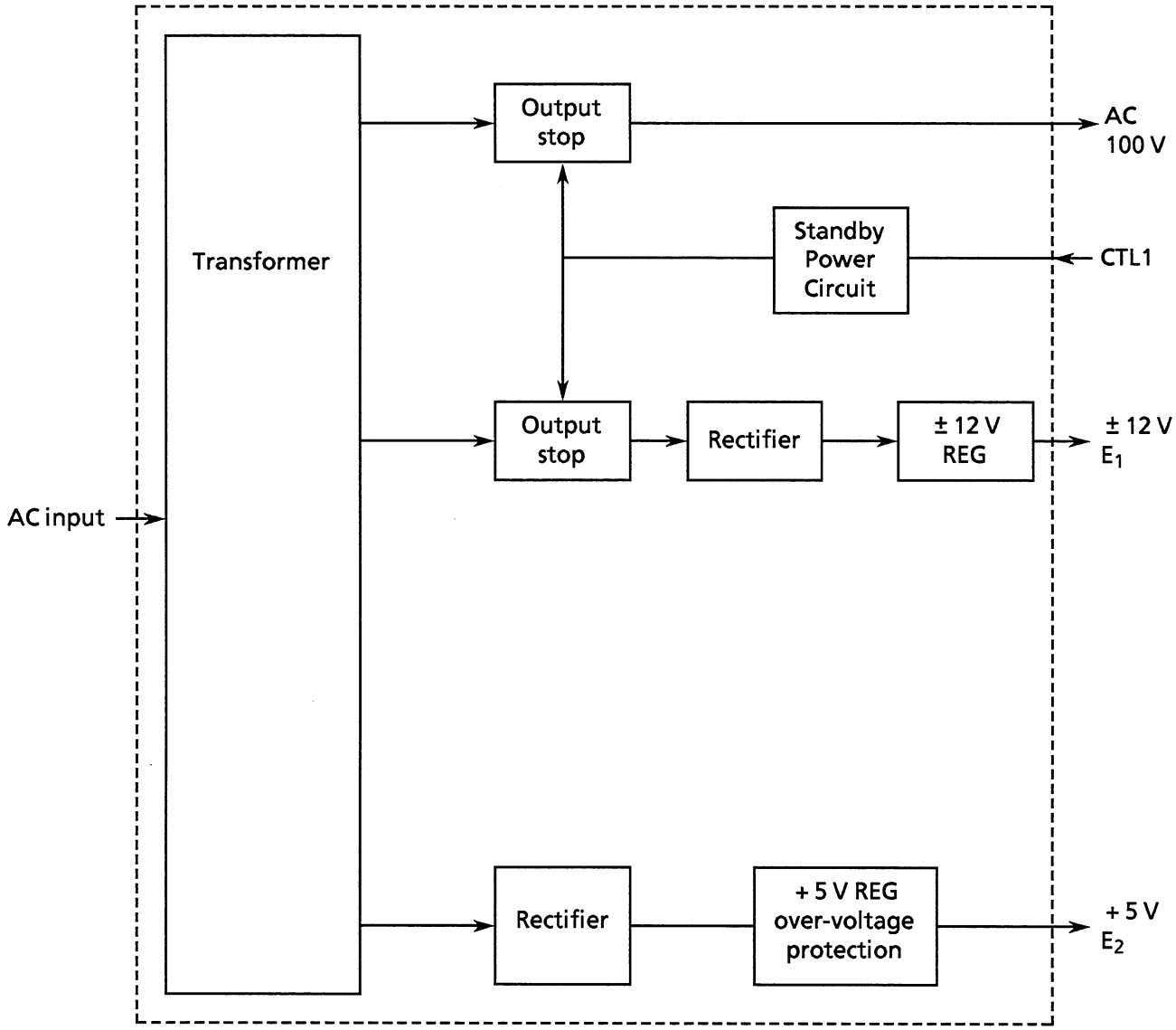
11. BLOCK DIAGRAM

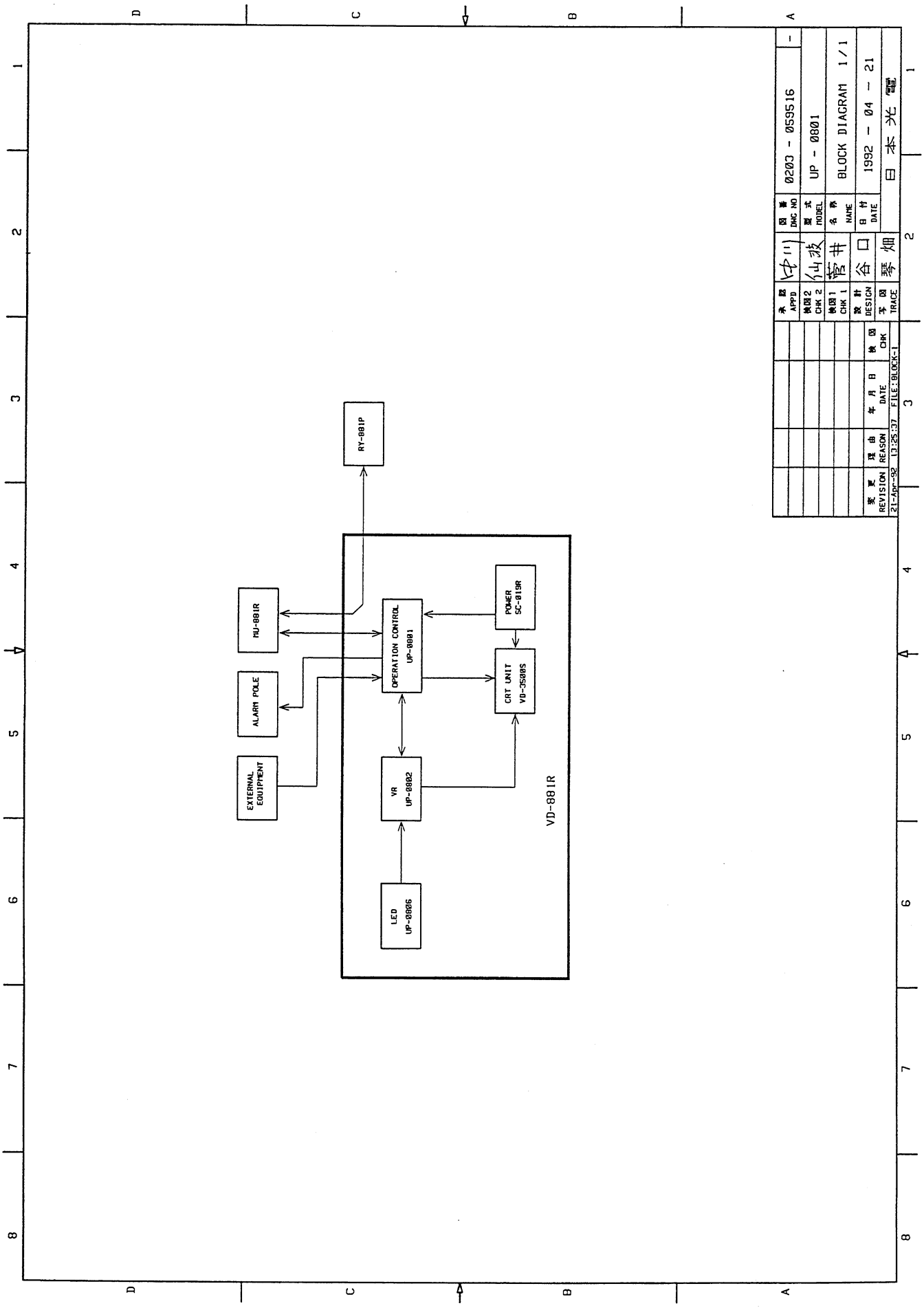



POWER SUPPLY
+5V,+12V
+12VA,-12V
E1,E2,E3
AC100V
ALARM POLE
+12VA
E2
RY-881P
+5V
E2
OPERATION CONTROL
UP-8801
VD-3508S
+12V,+5V
E1,E2
+12VC
E1
VR
UP-8802
+12V,+5V
E1,E2
LED
UP-8806
VD-881R
0203 - 059463
VD - 881R
POWER SUPPLY 1/1
1992 - 04 - 21
日本光電
REVISION
REASON
DATE
CHK
DESIGN
TRACE
APPD
CHK 2
CHK 1
MODEL
NAME
DWG NO
21-Apr-92 13:24:15 FILE:BLOCK-2

11. BLOCK DIAGRAM

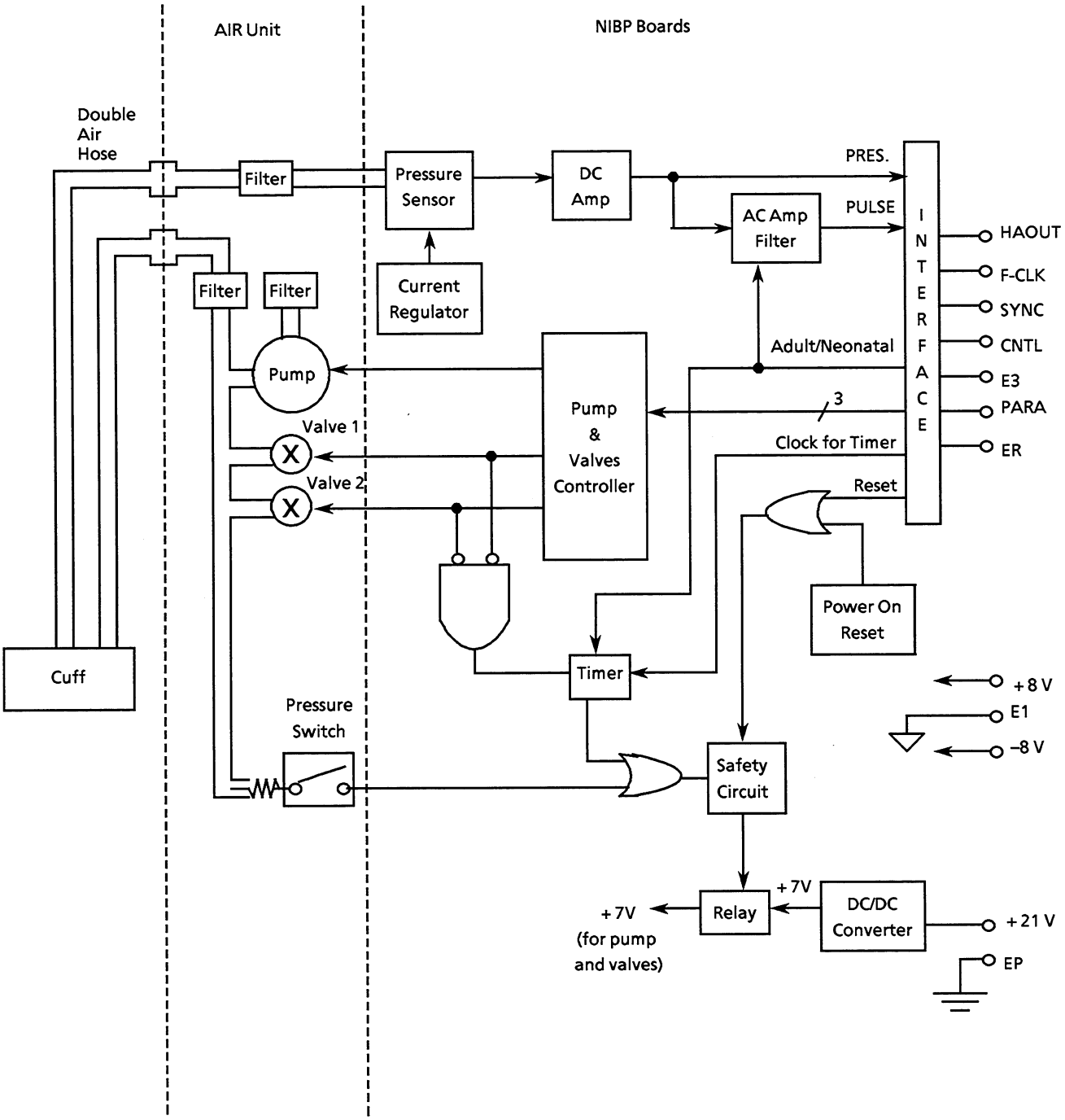
Power Supply Unit, SC-019R



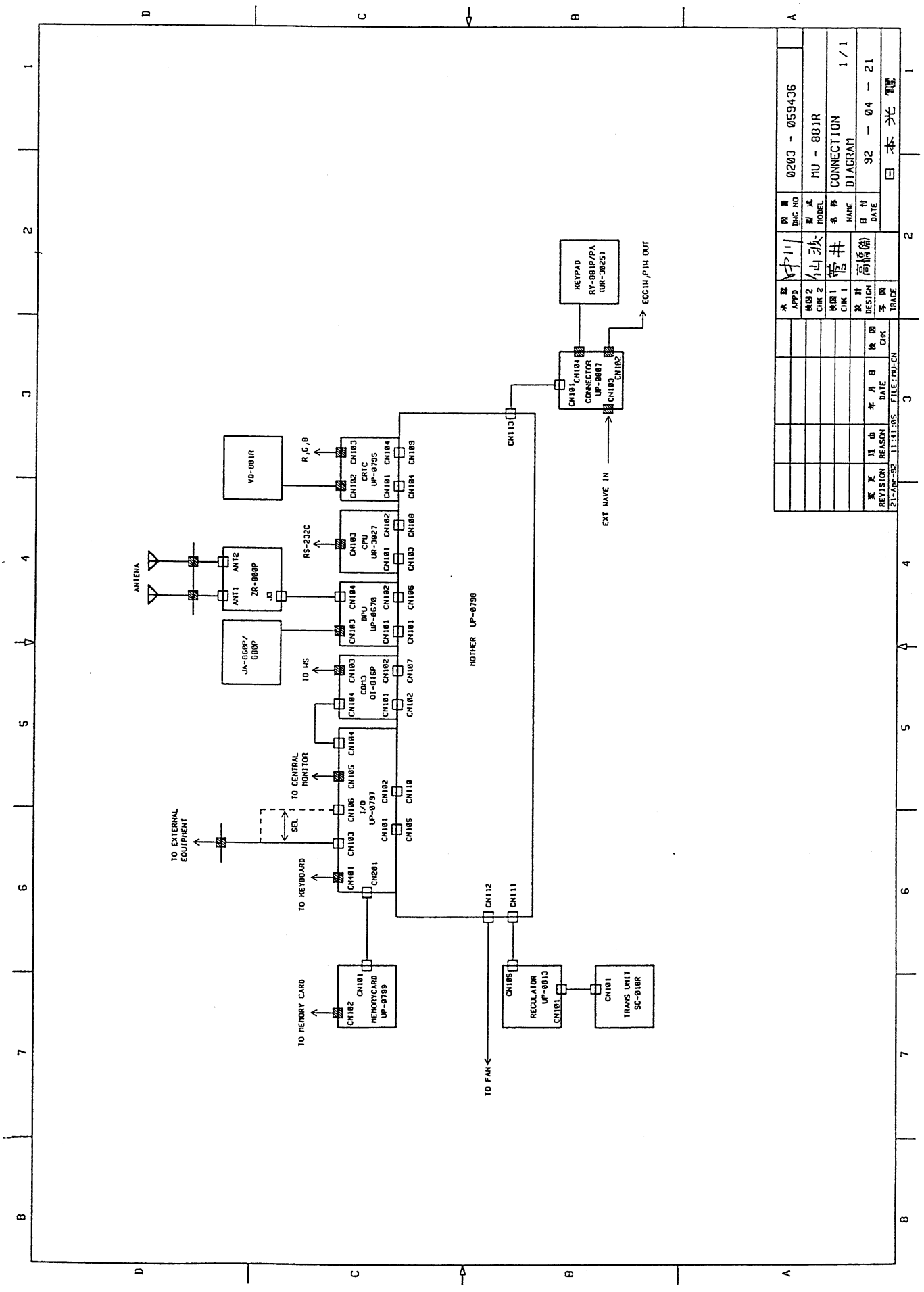

RY-881P
HU-881R
ALARM POLE
EXTERNAL EQUIPMENT
OPERATION CONTROL UP-8801
POWER SC-819R
CRT UNIT VD-3508
VR UP-8802
LED UP-8806
VD-881R
0203 - 059516
UP - 8801
BLOCK DIAGRAM 1/1
1992 - 04 - 21
日本光電
REVISION 21-Apr-92 13:25:37 FILE:BLOCK-1

11. BLOCK DIAGRAM

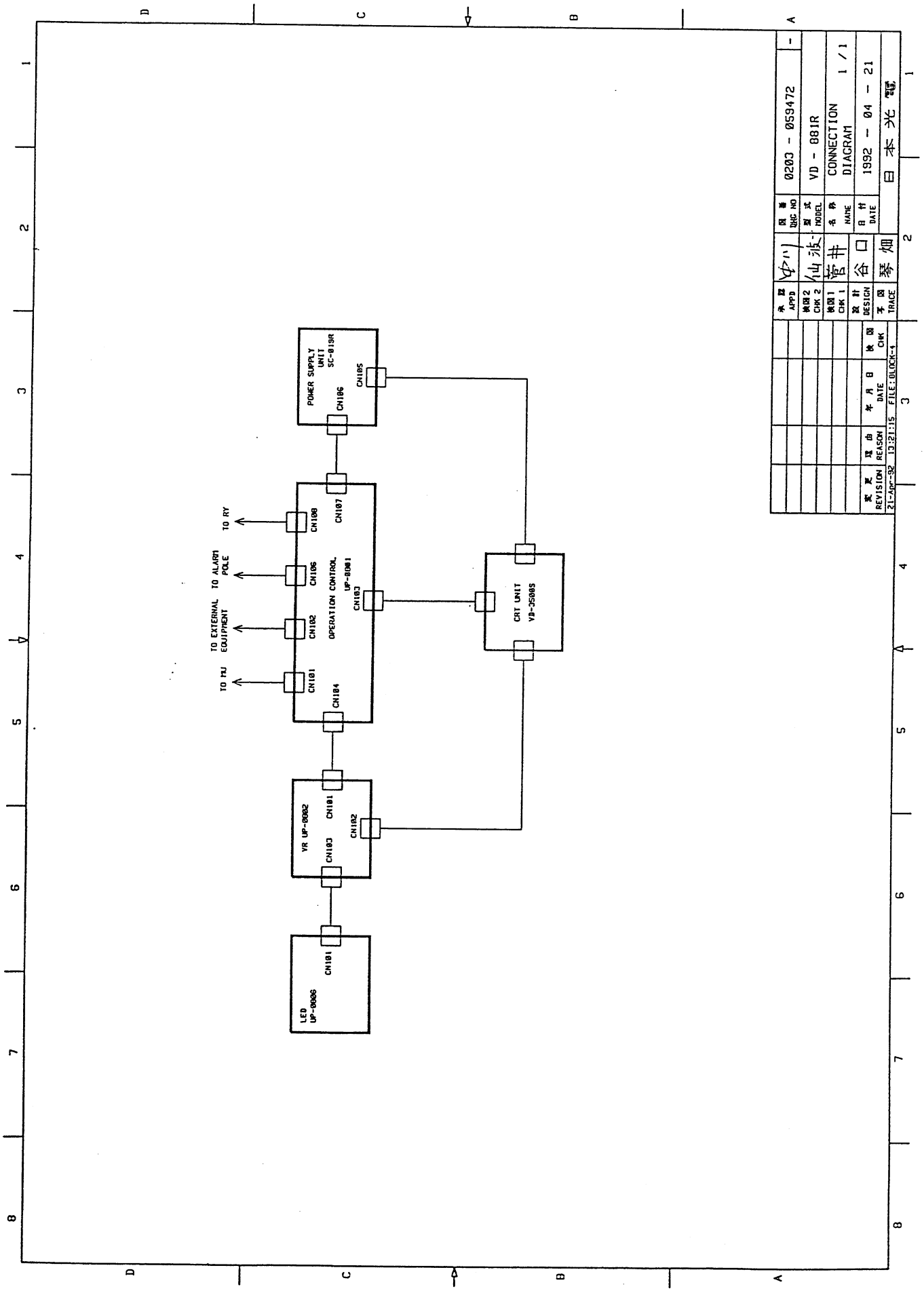
NIBP Head Amp, AP-860PA

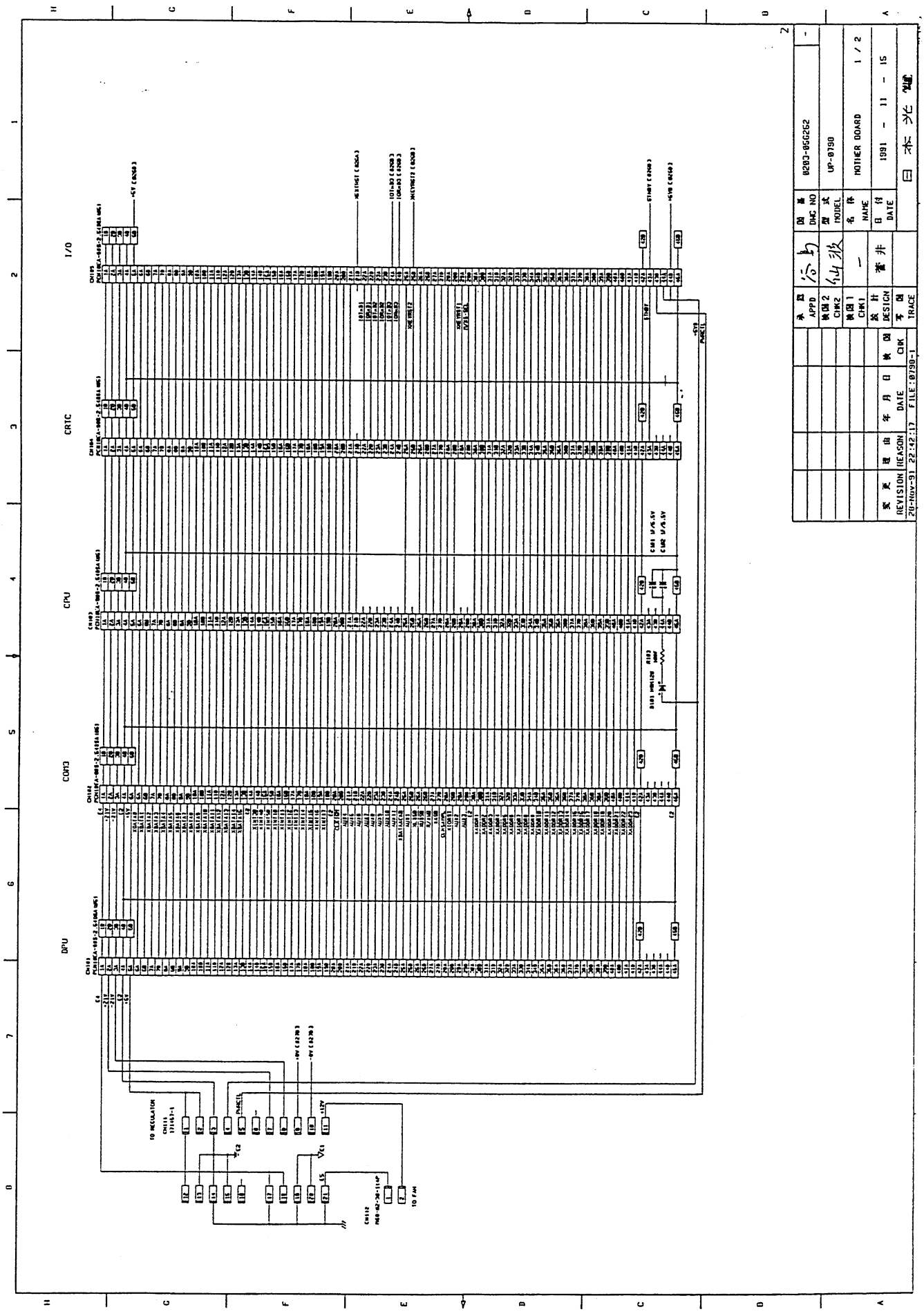


Section 12 CIRCUIT DIAGRAM

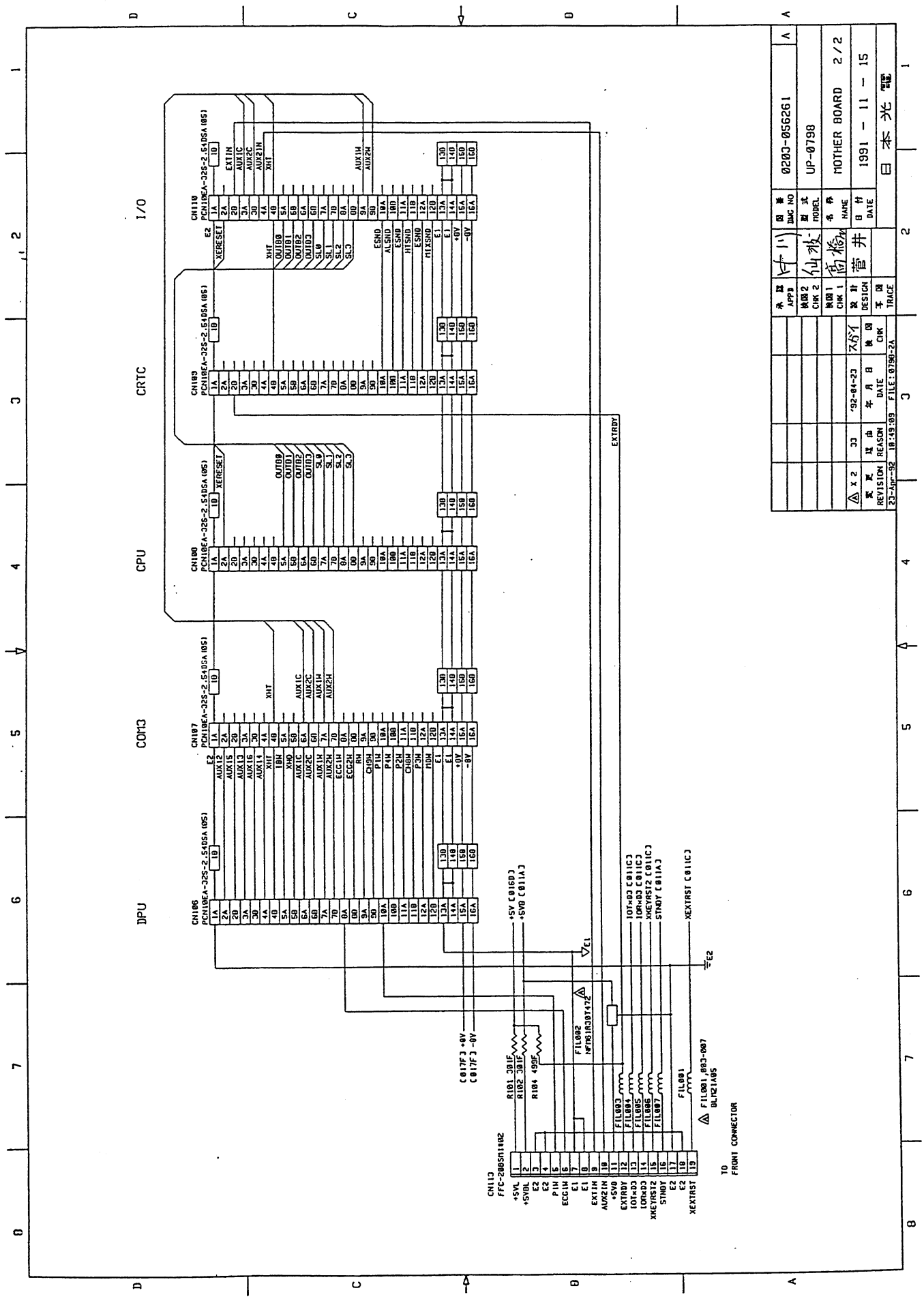

KEYPAD
RY-081P/PA
(UR-3025)
ECG1H,P1H OUT
EXT HAVE IN
CONNECTOR
UP-8087
MOTHER UP-8798
VD-081R
R,G,B
CRTC
UP-8795
RS-232C
CPU
UR-3827
ANTENA
ANT1
ANT2
ZR-088P
JD
DPU
UP-8678
JA-068P/
088P
TO HS
COM3
01-016P
TO CENTRAL
MONITOR
SEL
I/O
UP-8797
TO EXTERNAL
EQUIPMENT
TO KEYBOARD
TO MEMORY CARD
MEMORYCARD
UP-8799
REGULATOR
UP-8813
TRANS UNIT
SC-818R
TO FAN
CN113
CN112
CN111
0203 - 059436
MU - 881R
CONNECTION DIAGRAM
1 / 1
92 - 04 - 21
日本光
REVISION
DESIGN
TRACE
CHK
APPD
DATE
NAME
MODEL
DWG NO
21-Apr-92 11:41:05 FILE:MU-CN

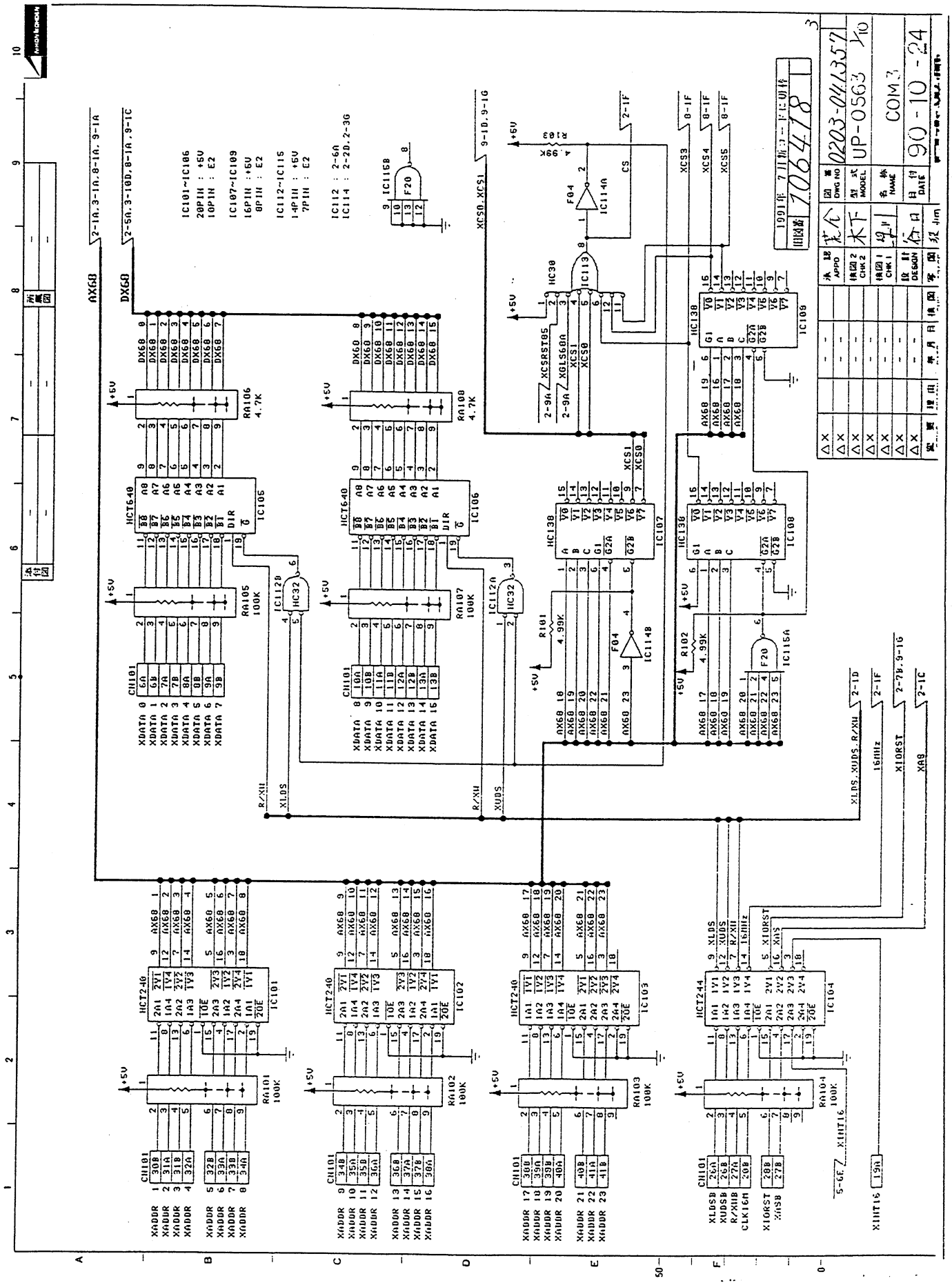
12. CIRCUIT DIAGRAM



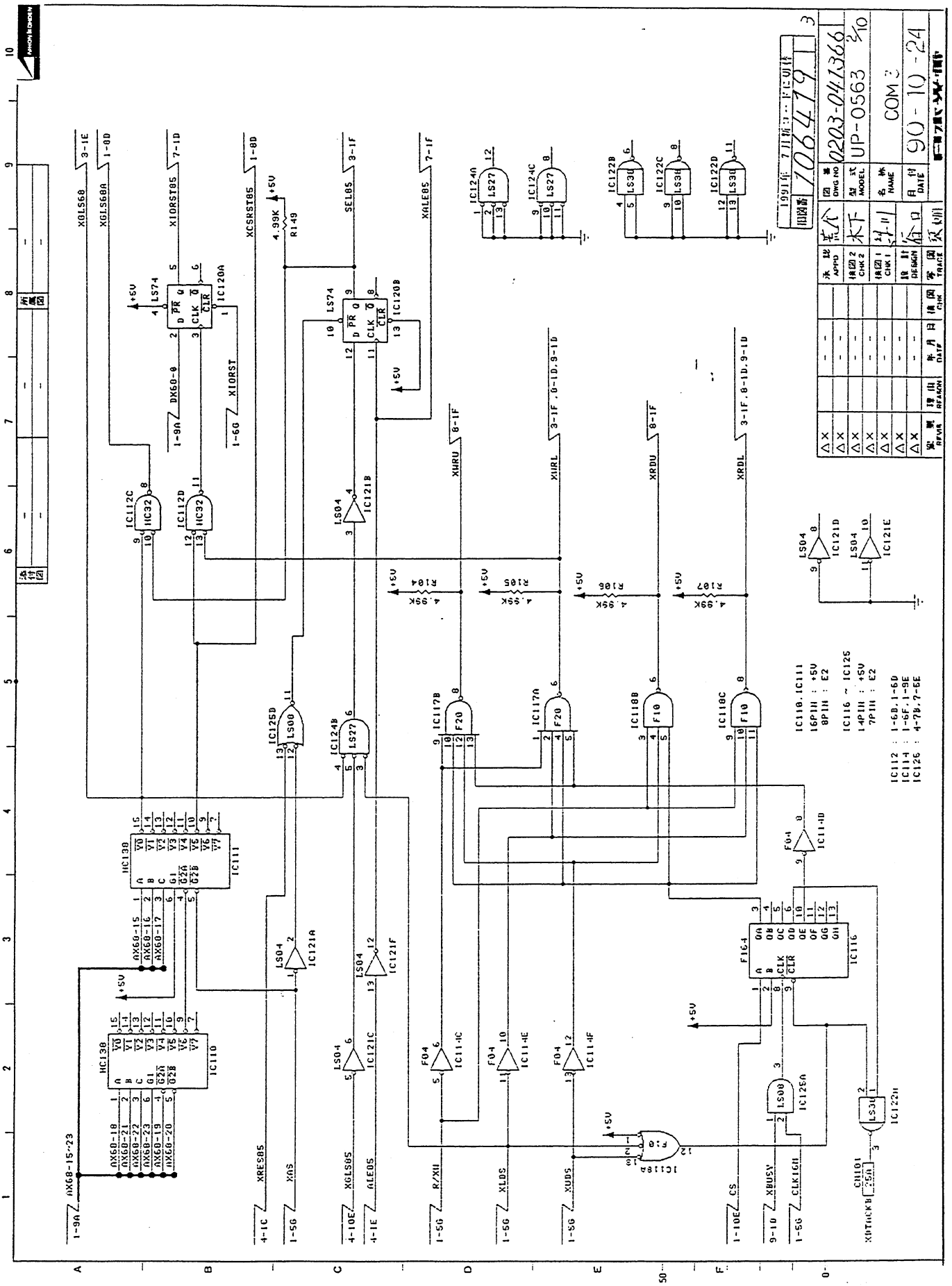

I/O
CRTC
CPU
COM3
DPU
TO REGULATOR
TO FAN
PANEL
APPD
CHK2
CHK1
DESIGN
TRACE
DMG NO
8203-8GG262
MODEL
UP-8790
NAME
MOTHER BOARD
1 / 2
DATE
1991 - 11 - 15
REVISION
REASON
DATE
CHK
29-Nov-91 22:42:17 FILE:8790-1

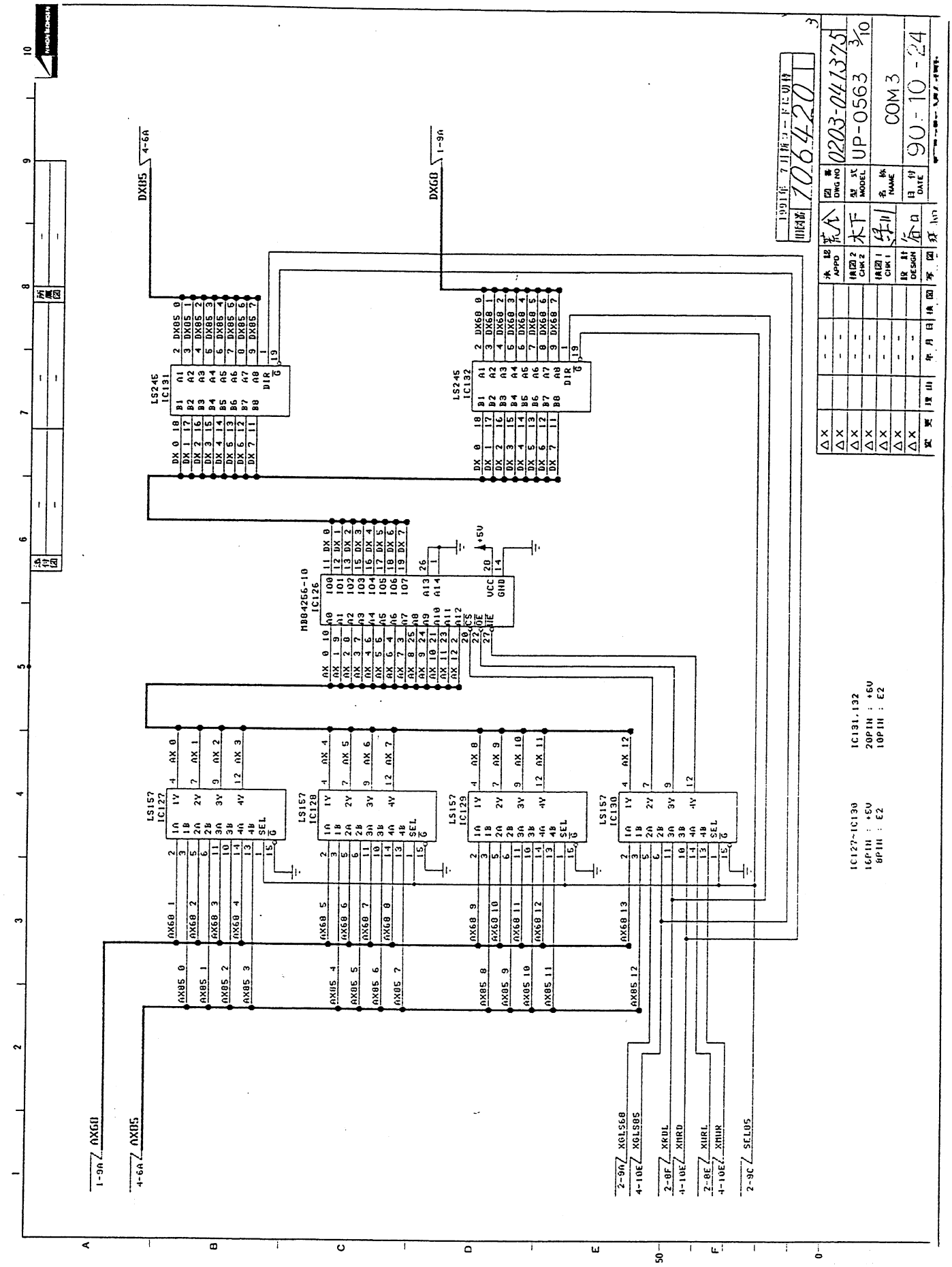
12. CIRCUIT DIAGRAM



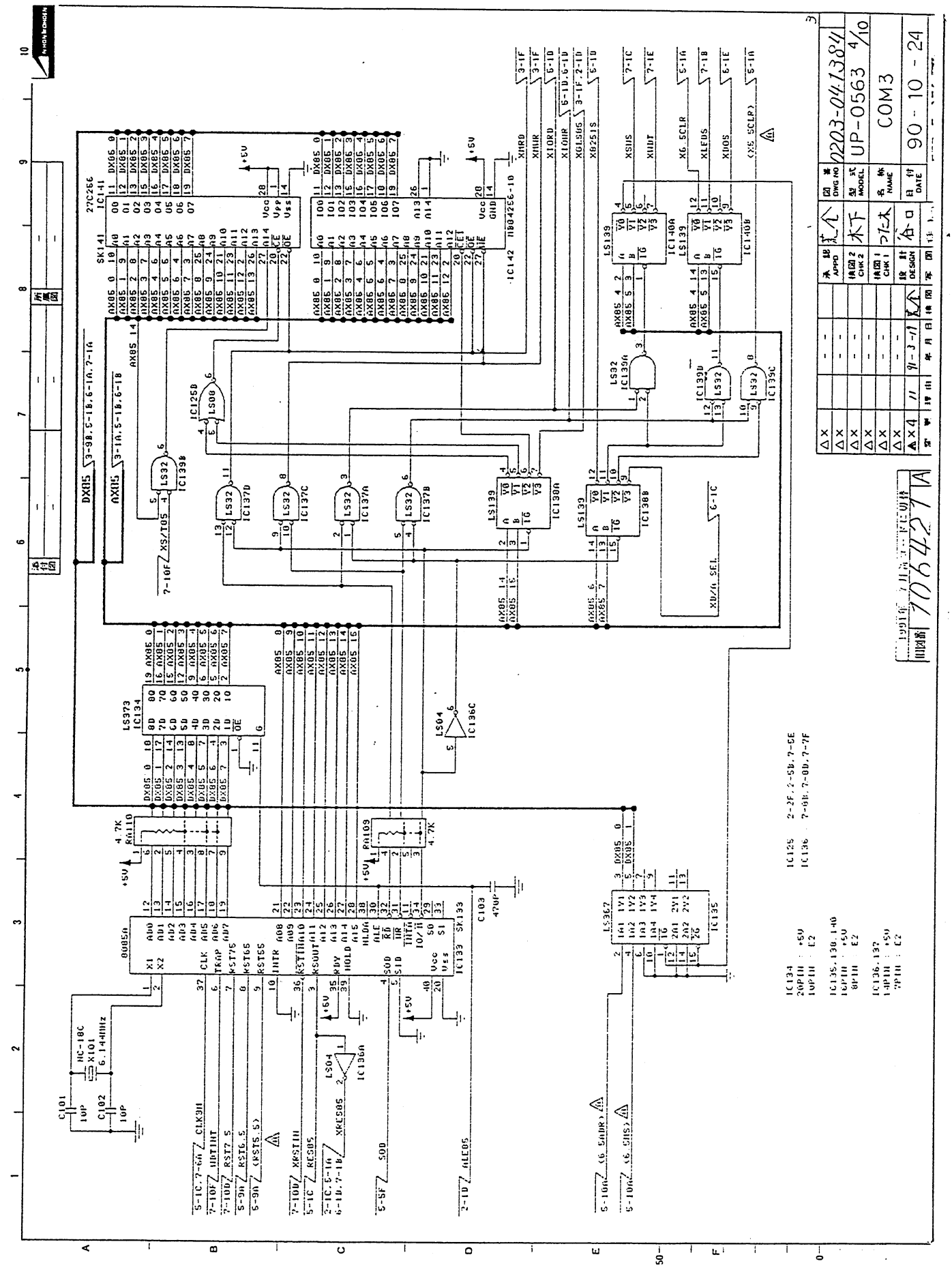


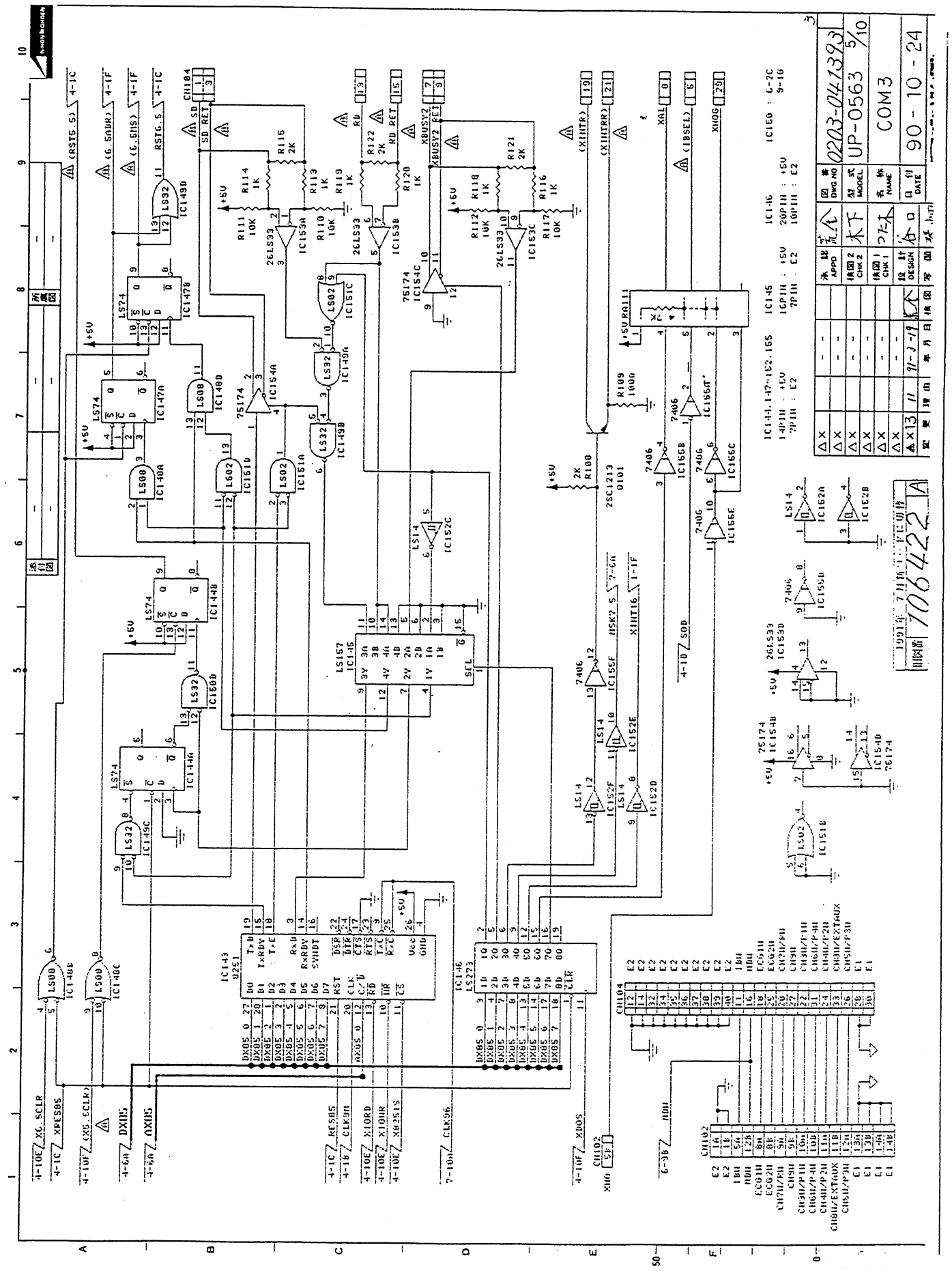
12. CIRCUIT DIAGRAM



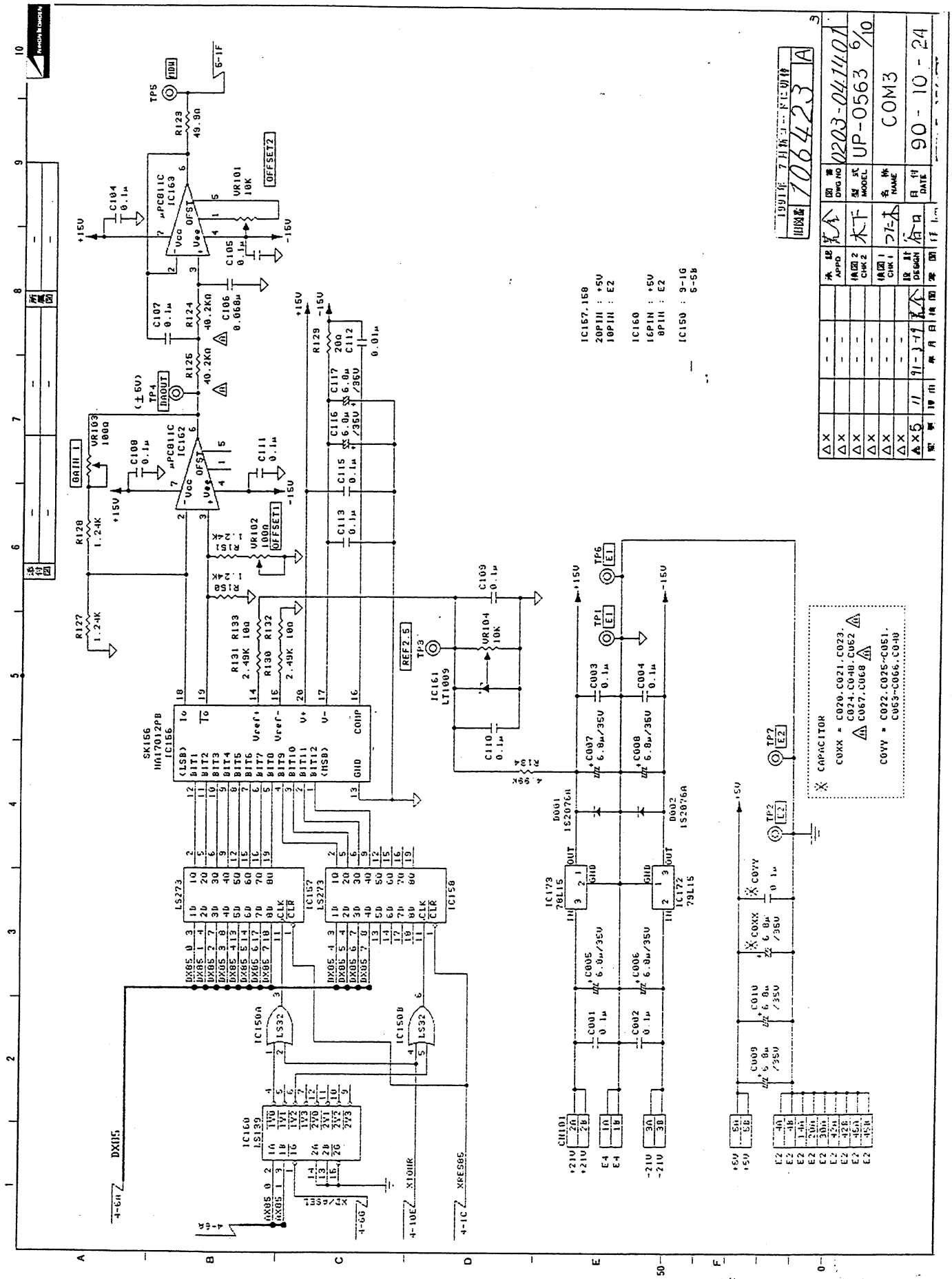

DXD5 4~6A
DXD0 1~9A
LS245 IC131
LS245 IC132
M884256-10 IC126
LS157 IC127
LS157 IC128
LS157 IC129
LS157 IC130
IC127~IC130 16PIN : +5V 8PIN : E2
IC131,132 20PIN : +5V 10PIN : E2
1-9A AXD0
4-6A AXD5
2-9A XGLSEL
4-10E XGLSDS
2-8F XKDL
4-10E XKRD
2-8E XURL
4-10E XMUR
2-9C SELD5
1991年 7月作成
1064220
0203-041375
UP-0563
COM3
90-10-24

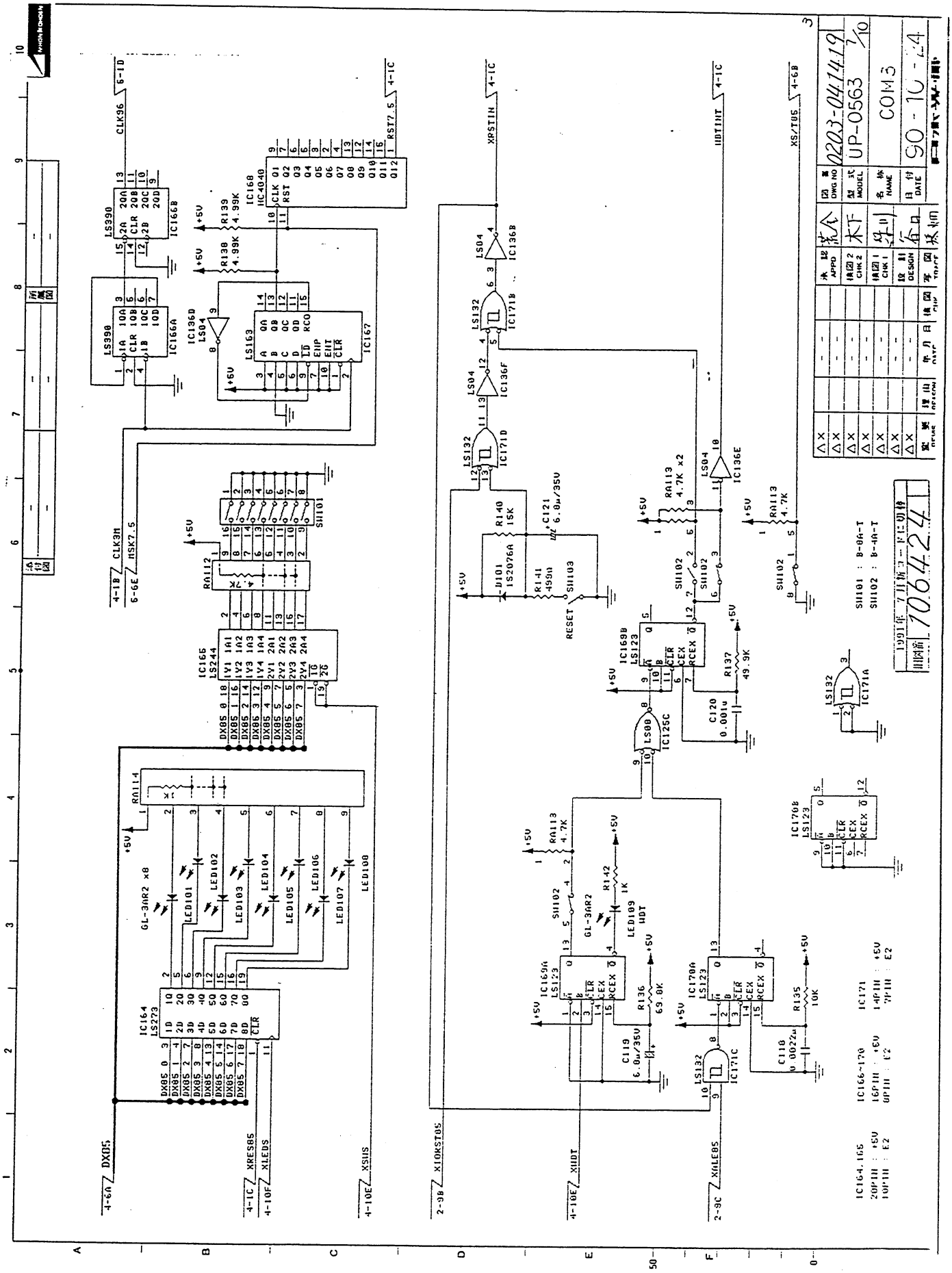
12. CIRCUIT DIAGRAM



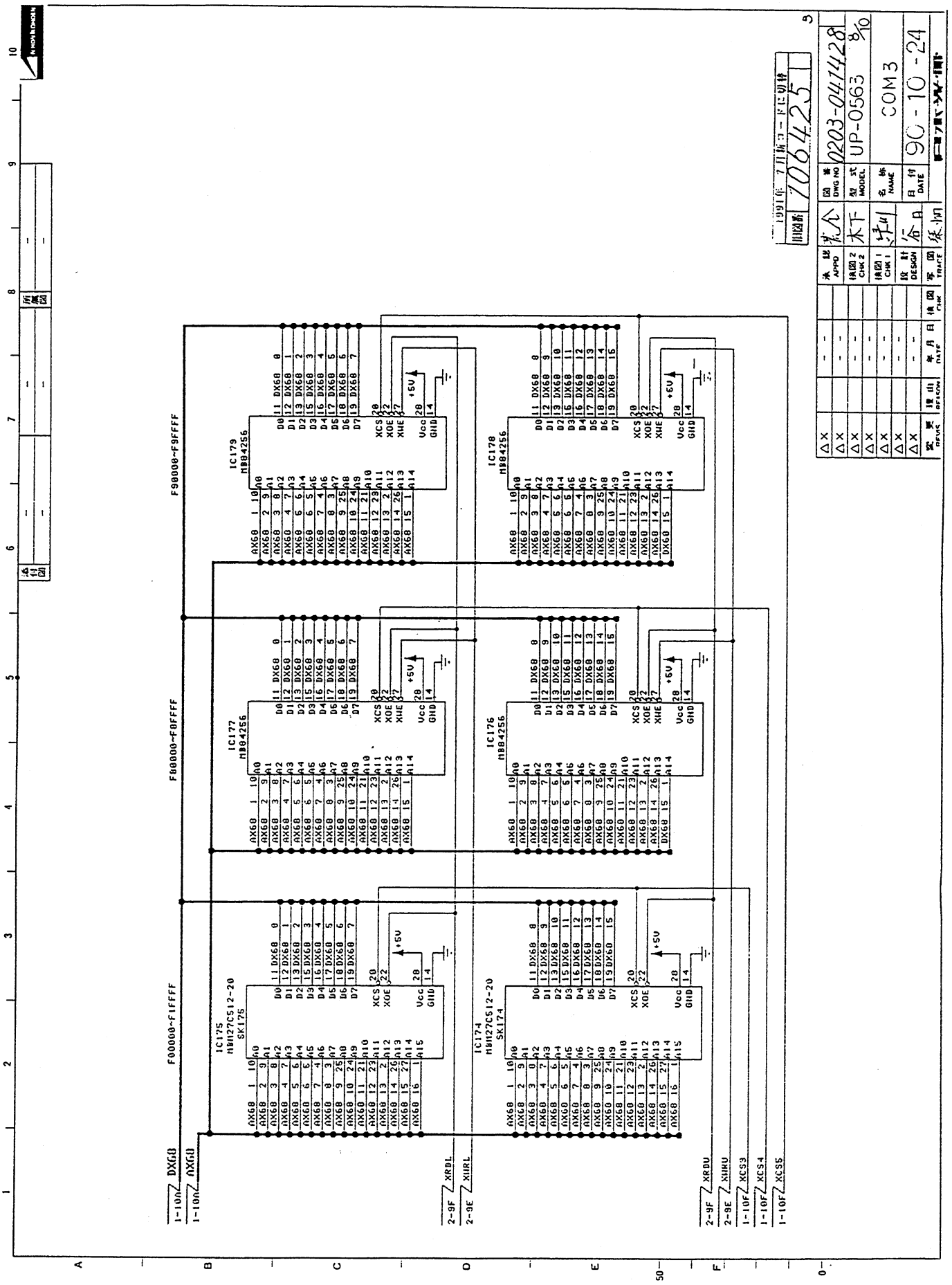


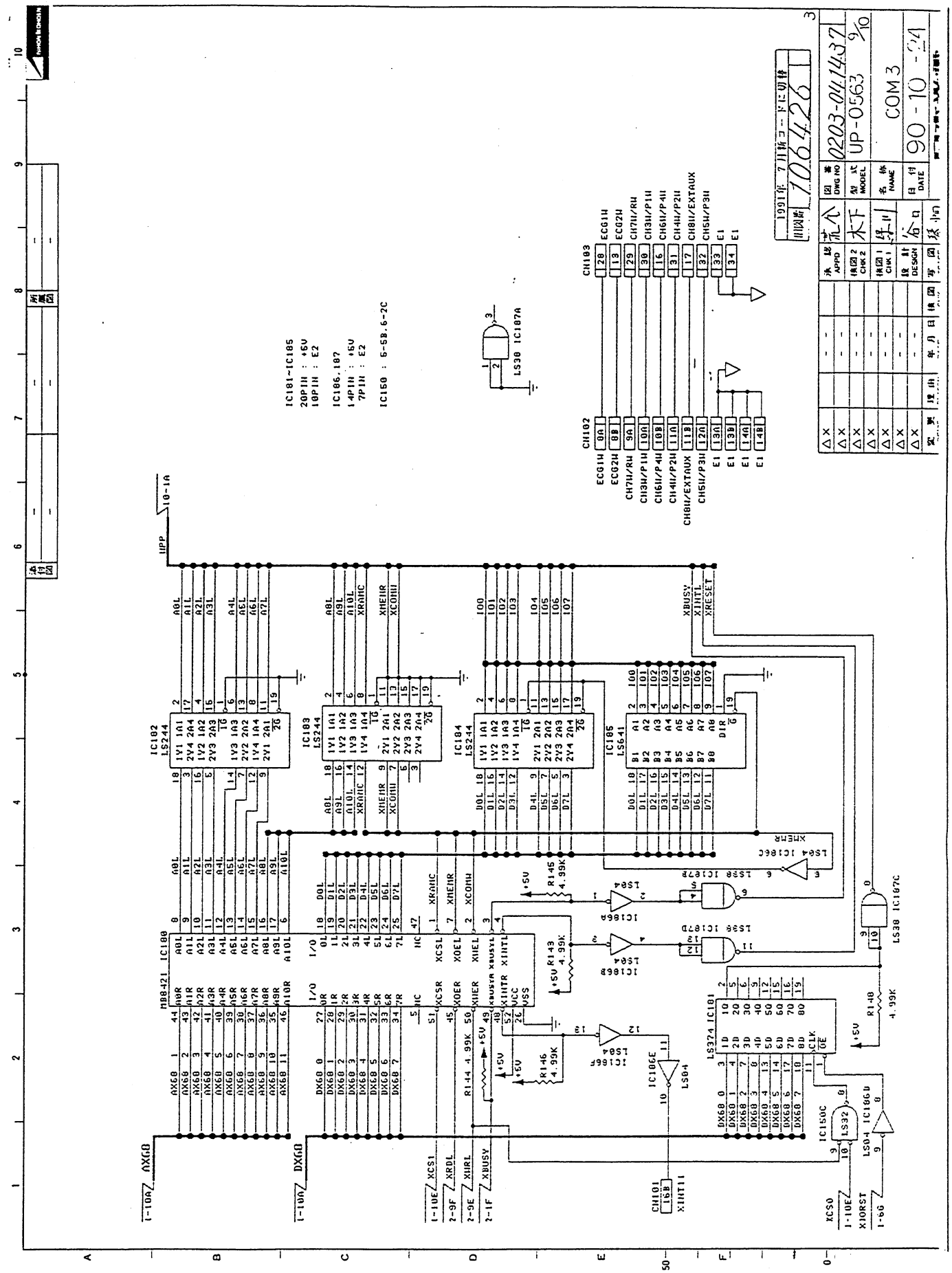
12. CIRCUIT DIAGRAM



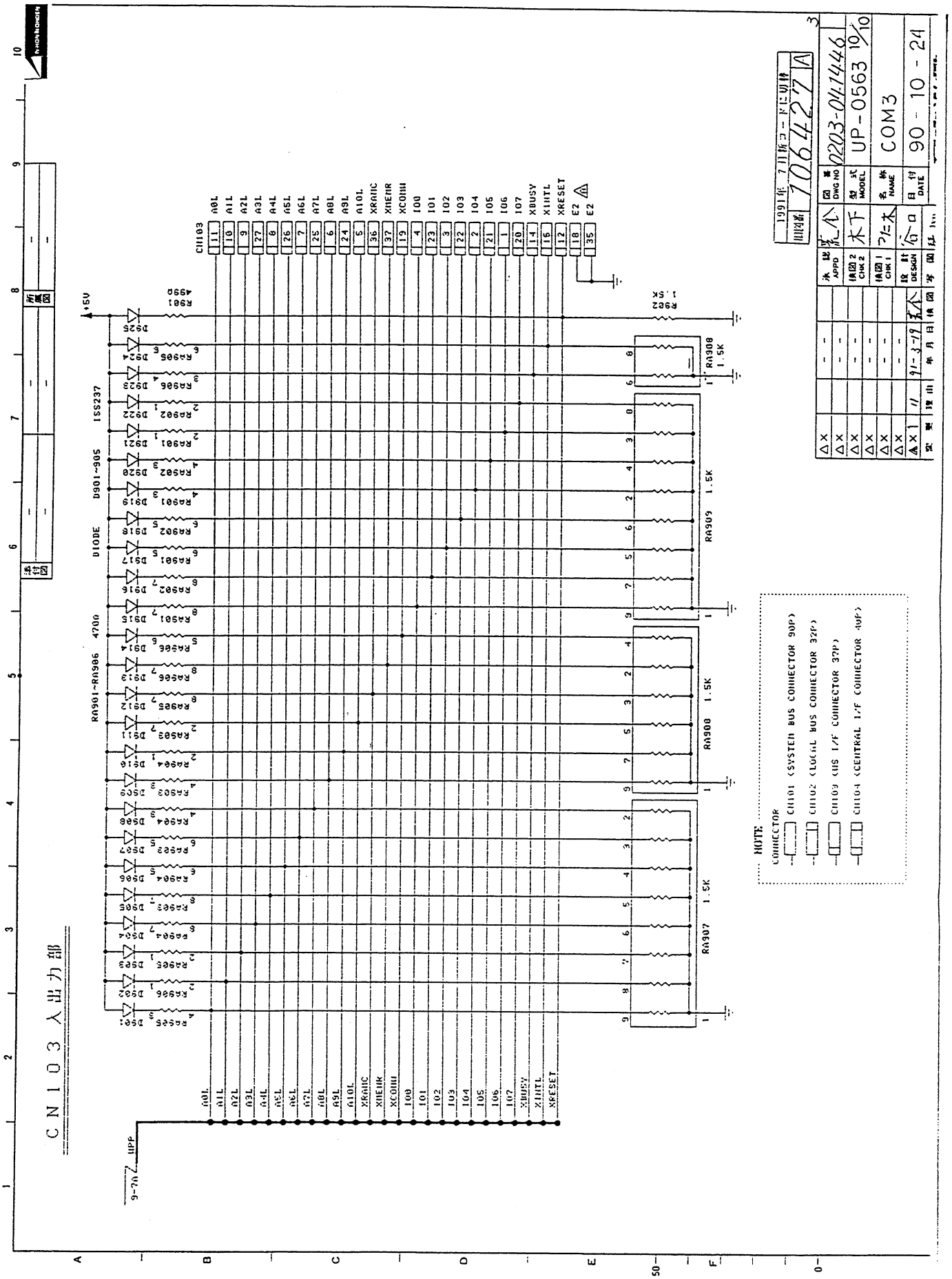


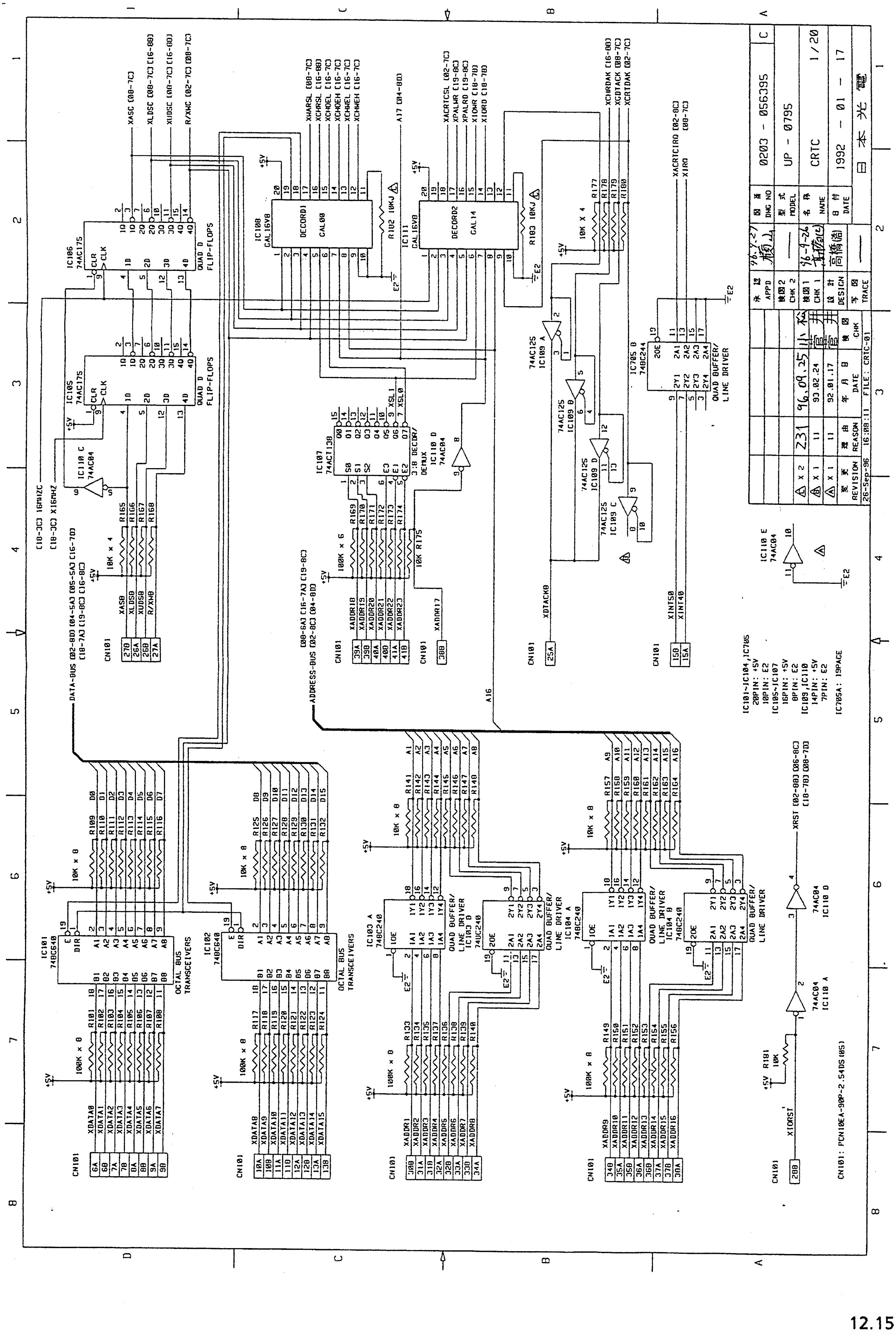
12. CIRCUIT DIAGRAM



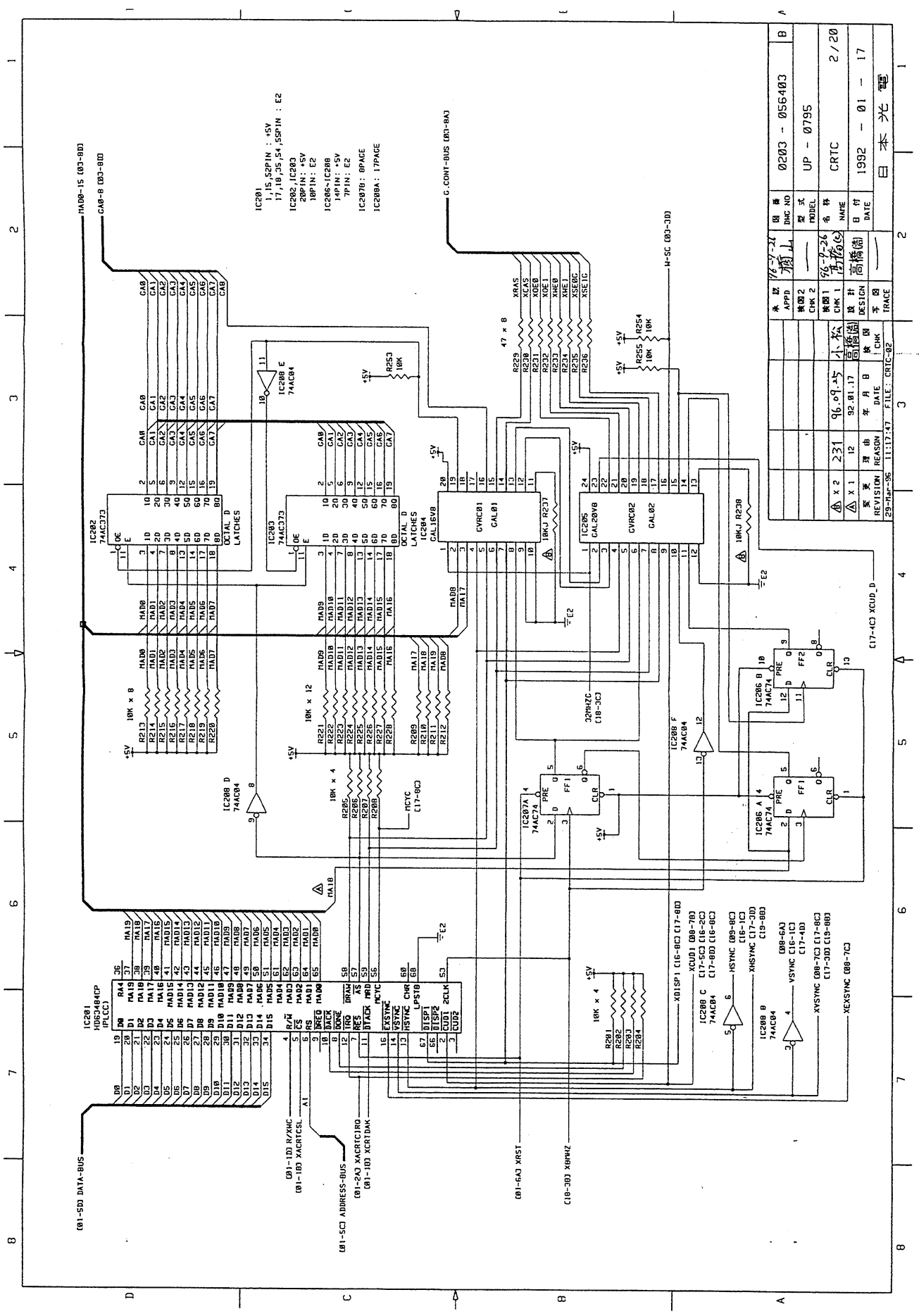

IC181~IC185
20PIN : +5V
10PIN : E2
IC186,187
14PIN : +5V
7PIN : E2
IC150 : 6-58.6-2C
LS38 IC187A
CH103
CH102
ECG1H
ECG2H
CH7U/RU
CH3U/P1U
CH6U/P4U
CH4U/P2U
CH8U/EXTAUX
CH5U/P3U
E1
IC182 LS244
IC183 LS244
IC184 LS244
IC185 LS641
IC180 MB8421
LS374 IC181
LS38 IC187C
LS32 IC186D
LS04 IC186B
LS04 IC186C
LS04 IC186E
LS04 IC186F
R145 4.99K
R146 4.99K
R143 4.99K
R144 4.99K
R148 4.99K
+5V
AX60
DX60
XCS1
XRDL
XIORL
XBUSY
XCS0
XIORST
XINT11
CH101
XMEMR
XRESET
XBUSY
XINTL
XCSL
XOEL
XMEL
XCSR
XOER
XMER
XINTR
XBUSYR
XINTL
XRANIC
XMEMR
XCOMM
1991年 7月15日 一 下午 1:06:26
0203-041437
UP-0563
COM3
90-10-24
9/10

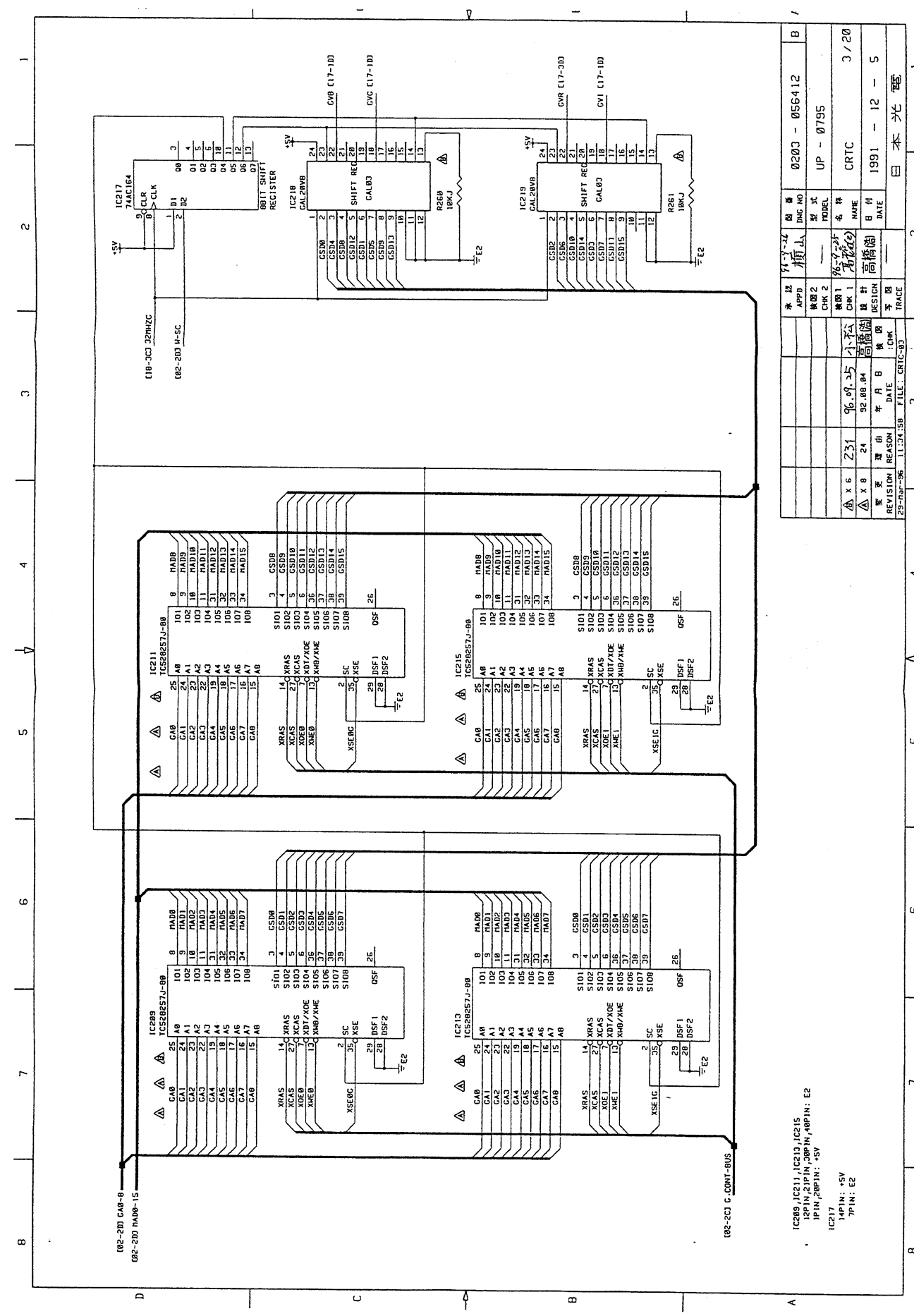
12. CIRCUIT DIAGRAM



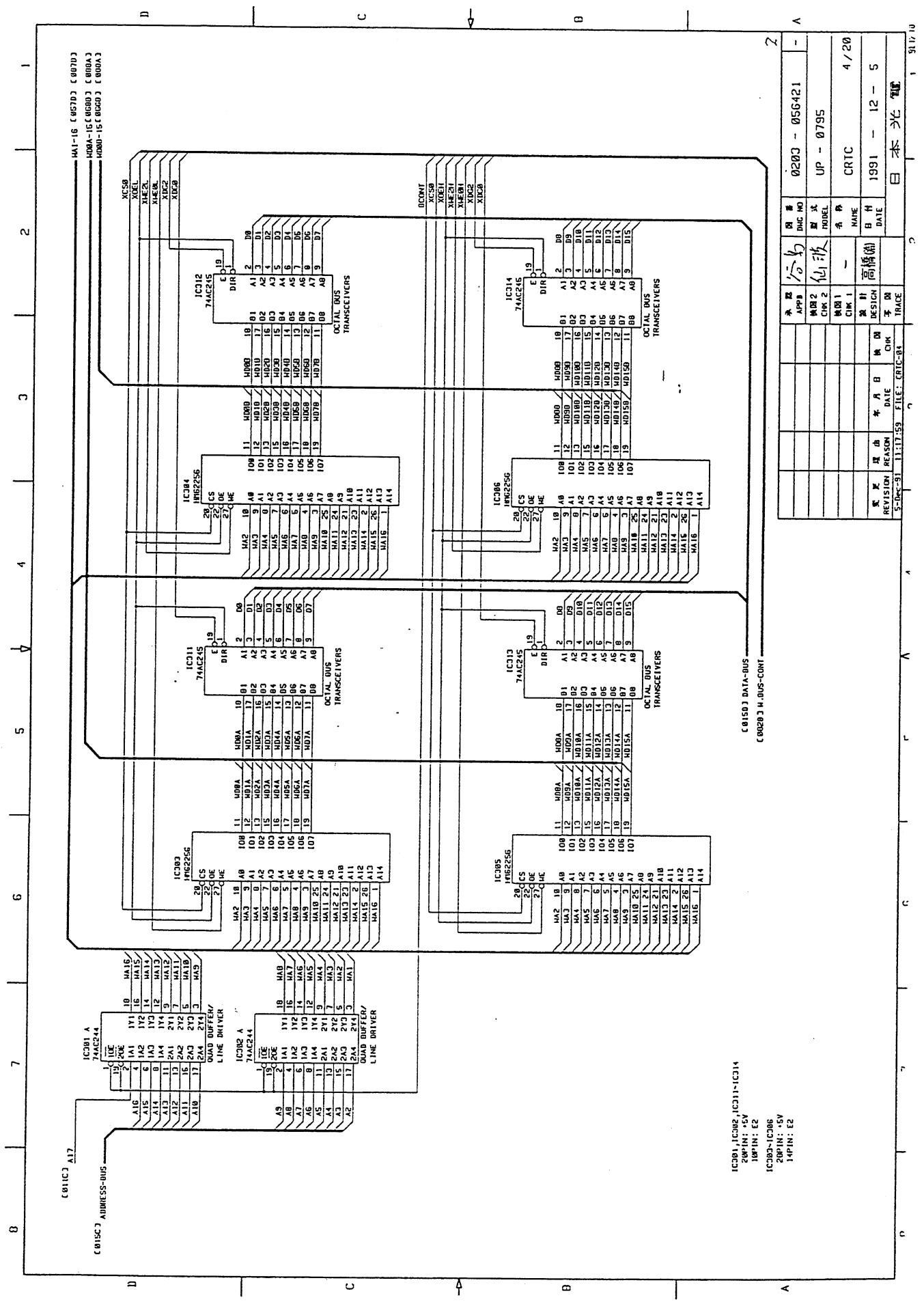

0203 - 056395
C
UP - 0795
CRTC
1/20
1992 - 01 - 17
日本光電
FILE: CRTC-01
IC106
74AC175
QUAD D FLIP-FLOPS
IC105
74AC175
IC108
CAL16V8
DECORD1
CAL08
IC111
CAL16V8
DECORD2
CAL14
R102 10KJ
R103 10KJ
IC107
74AC138
3:8 DECDR/DEMUX
IC110 D
74AC04
74AC125
IC109 A
IC109 B
IC109 C
IC109 D
IC705 B
74BC244
QUAD BUFFER/LINE DRIVER
IC101
74BC640
OCTAL BUS TRANSCEIVERS
IC102
74BC640
IC103 A
74BC240
IC103 B
IC104 A
IC104 B
DATA-BUS
ADDRESS-BUS
XASC
XLDSC
XUDSC
R/XWC
XHARSL
XCHRSL
XCHOEL
XCHOEH
XCHWEL
XCHWEH
A17
XACRTCSL
XPALWR
XPALRD
XIOWR
XIORD
XCHRDAK
XGDTACK
XCRTDAK
XACRTCIRQ
XIRQ
XDTACK0
XINT50
XINT40
XRST
XIORST
16MHZC
X16MHZ
IC101~IC104,IC705
20PIN: +5V
10PIN: E2
IC105~IC107
16PIN: +5V
8PIN: E2
IC109,IC110
14PIN: +5V
7PIN: E2
IC705A: 19PAGE
CN101: PCN10EA-90P-2.54DS(05)

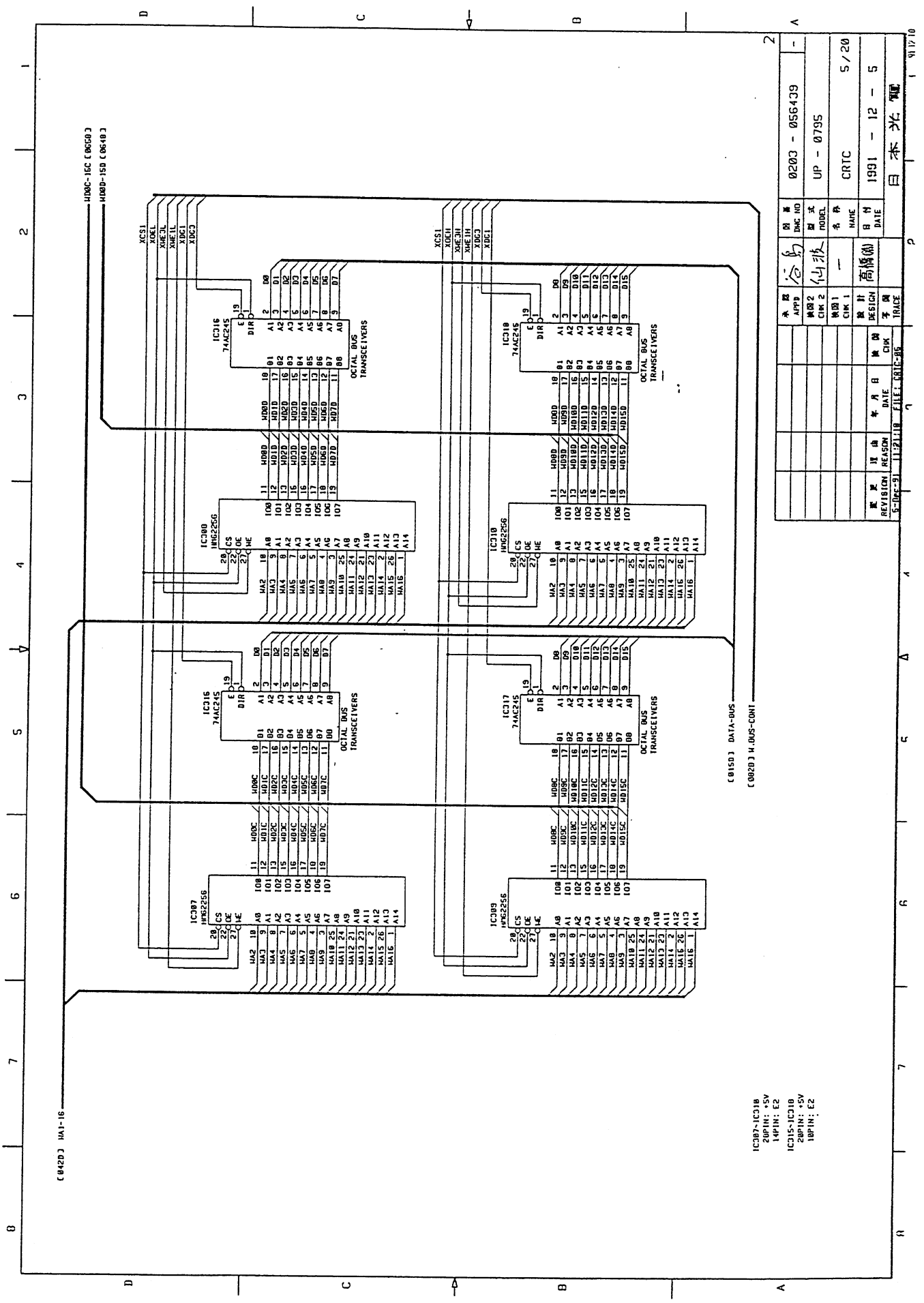
12. CIRCUIT DIAGRAM



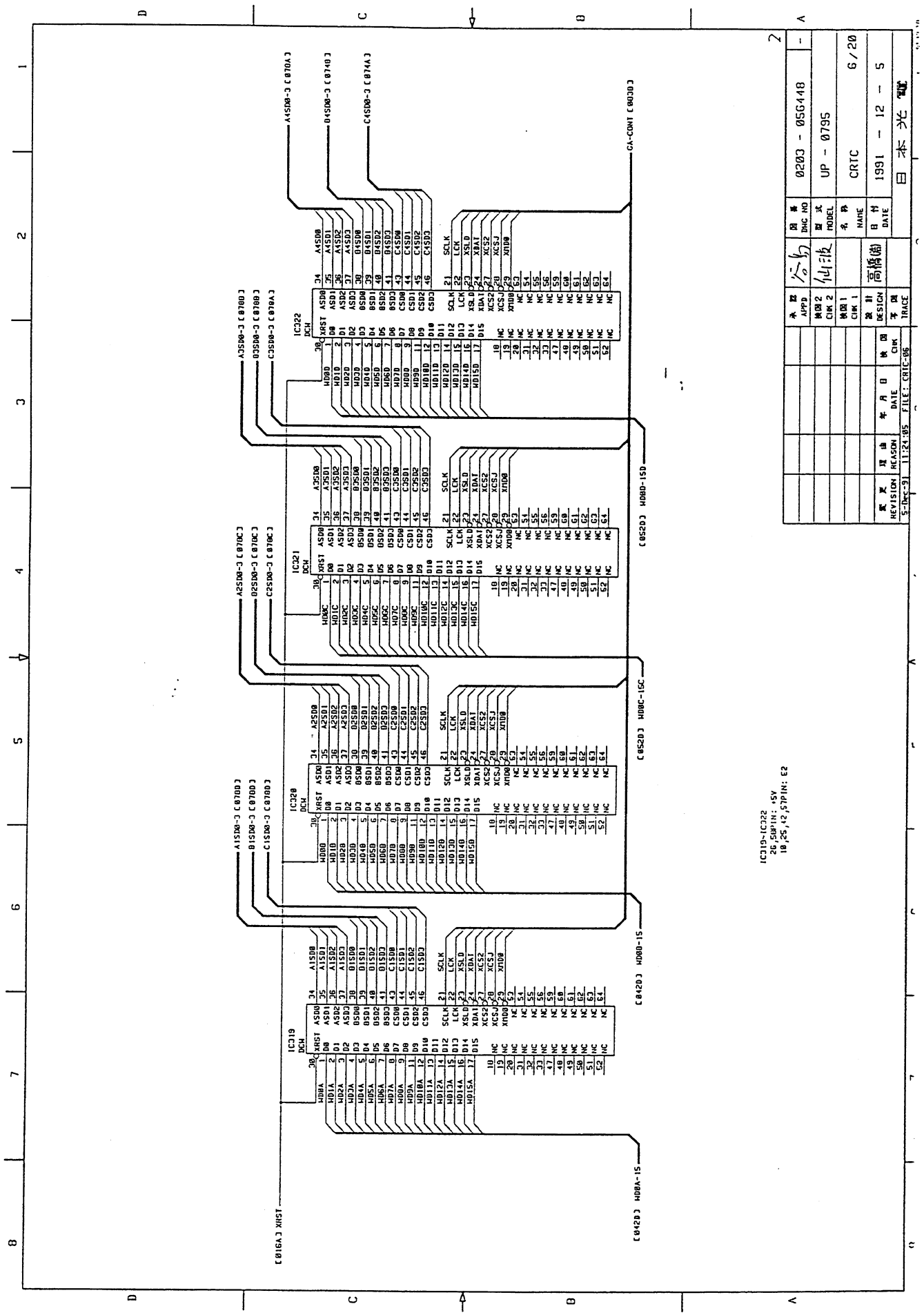

IC217 74AC164
8BIT SHIFT REGISTER
IC218 CAL20V8
IC219 CAL20V8
SHIFT REG CAL03
R260 10KJ
R261 10KJ
IC211 TC528257J-00
IC215 TC528257J-00
IC209 TC528257J-00
IC213 TC528257J-00
[10-3C] 32MHZC
[02-2D] H-SC
[02-2D] MAD0-15
[02-2C] G_CONT-BUS
IC209,IC211,IC213,IC215
12PIN,21PIN,30PIN,40PIN: E2
1PIN,20PIN: +5V
IC217
14PIN: +5V
7PIN: E2
0203 - 0564 12
UP - 0795
CRTC
1991 - 12 - 5
日本光電
3/20

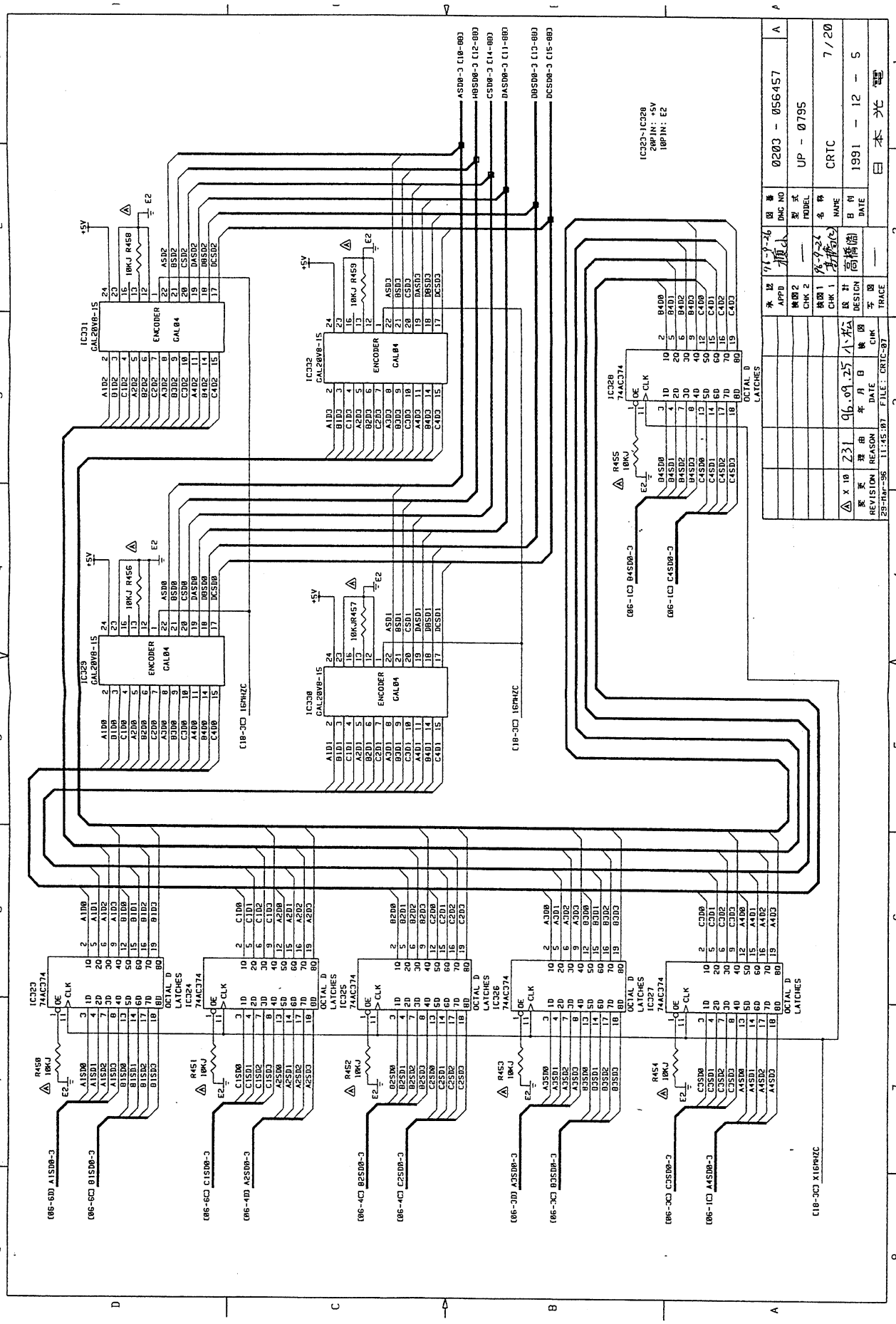
12. CIRCUIT DIAGRAM



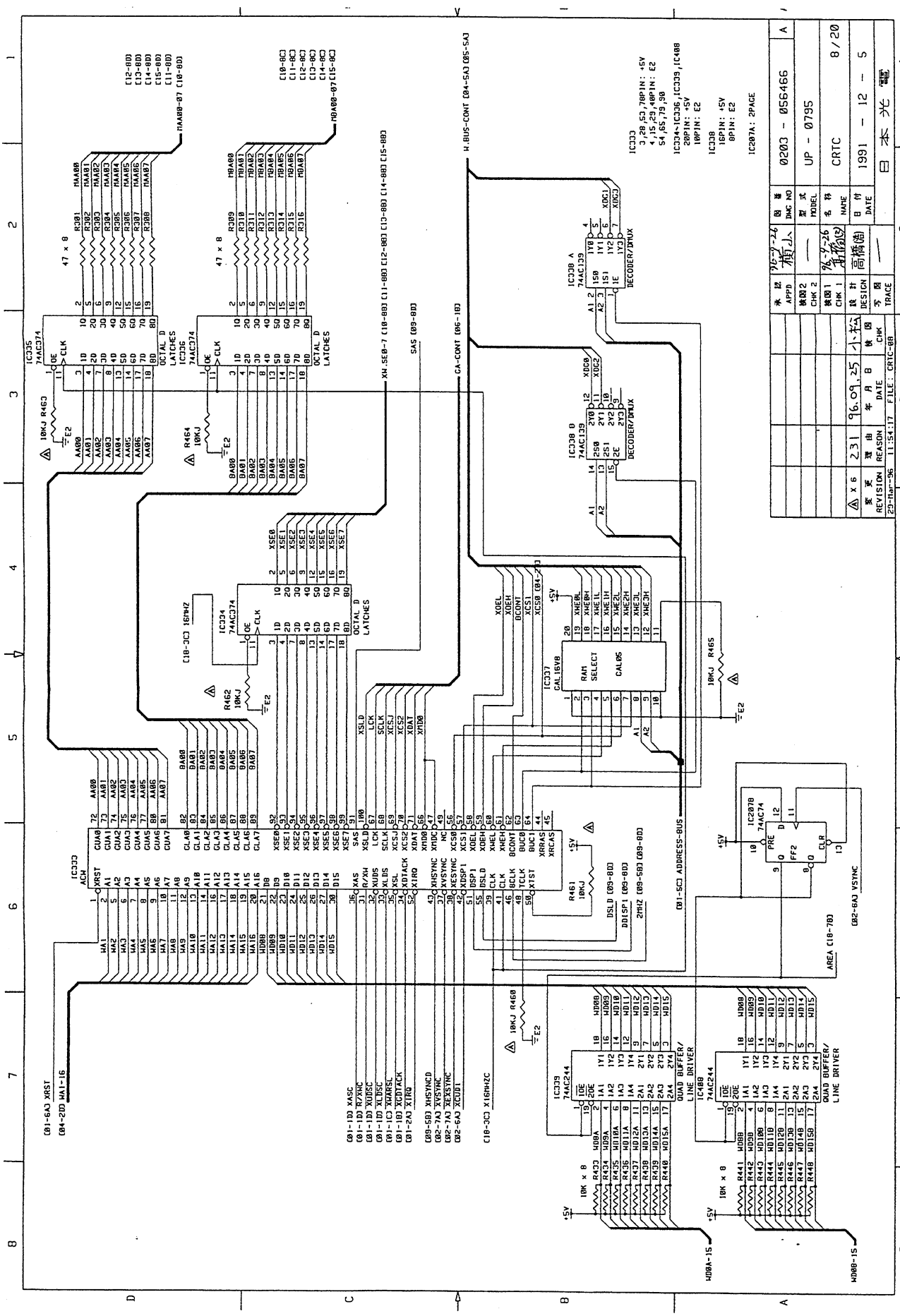

REVISION
REASON
DATE
FILE: CRTC-05
APPD
CHK 2
DRWN 1
CHK 1
DESIGN
TRACE
DWG NO
0203 - 056439
MODEL
UP - 0795
NAME
CRTC
5/20
DATE
1991 - 12 - 5
日本光電
OCTAL BUS TRANSCEIVERS
74AC245
HM62256
DATA-BUS
M.BUS-CONT
HA1-16
IC307~IC310
20PIN: +5V
14PIN: E2
IC315~IC318
20PIN: +5V
18PIN: E2

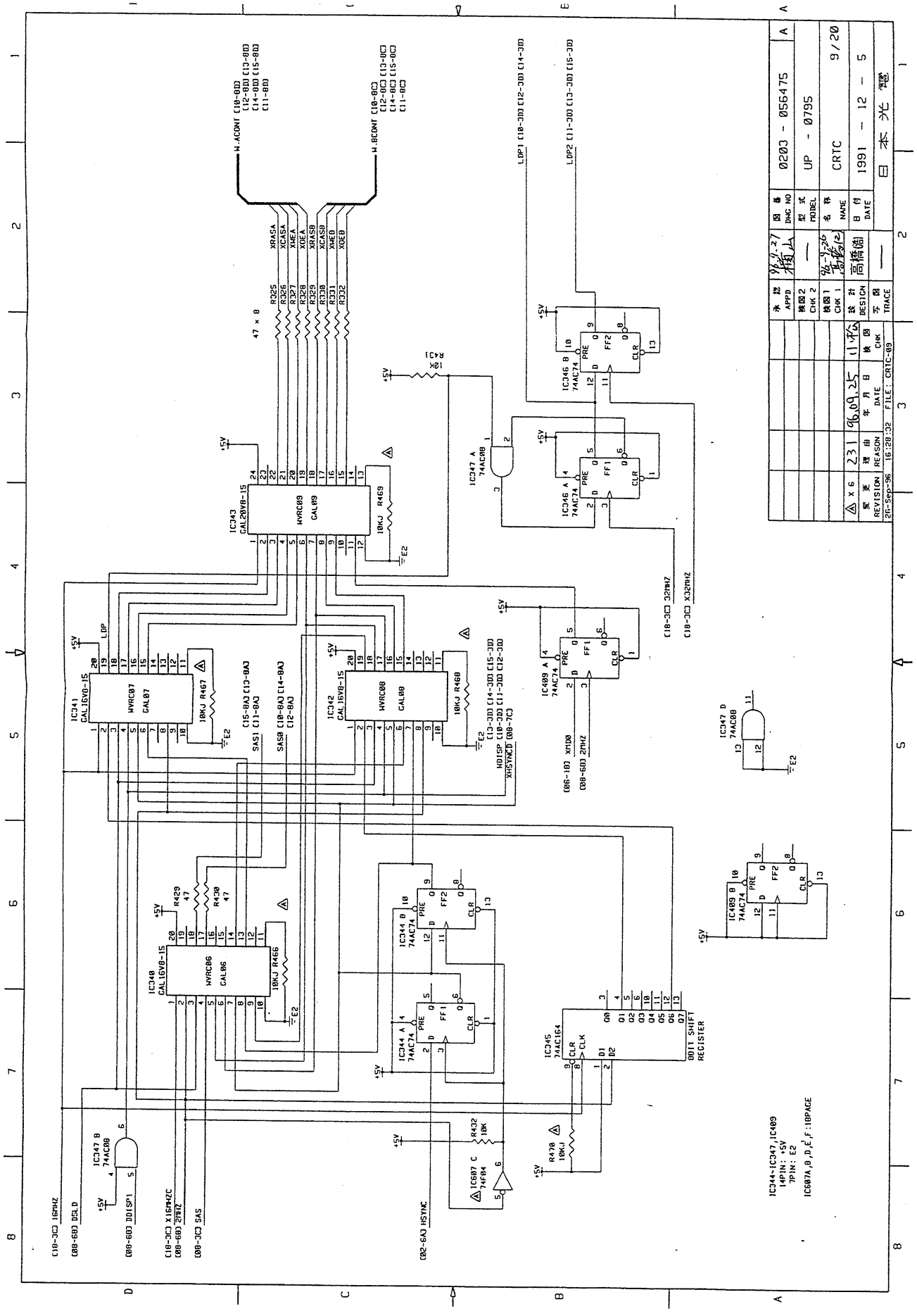
12. CIRCUIT DIAGRAM



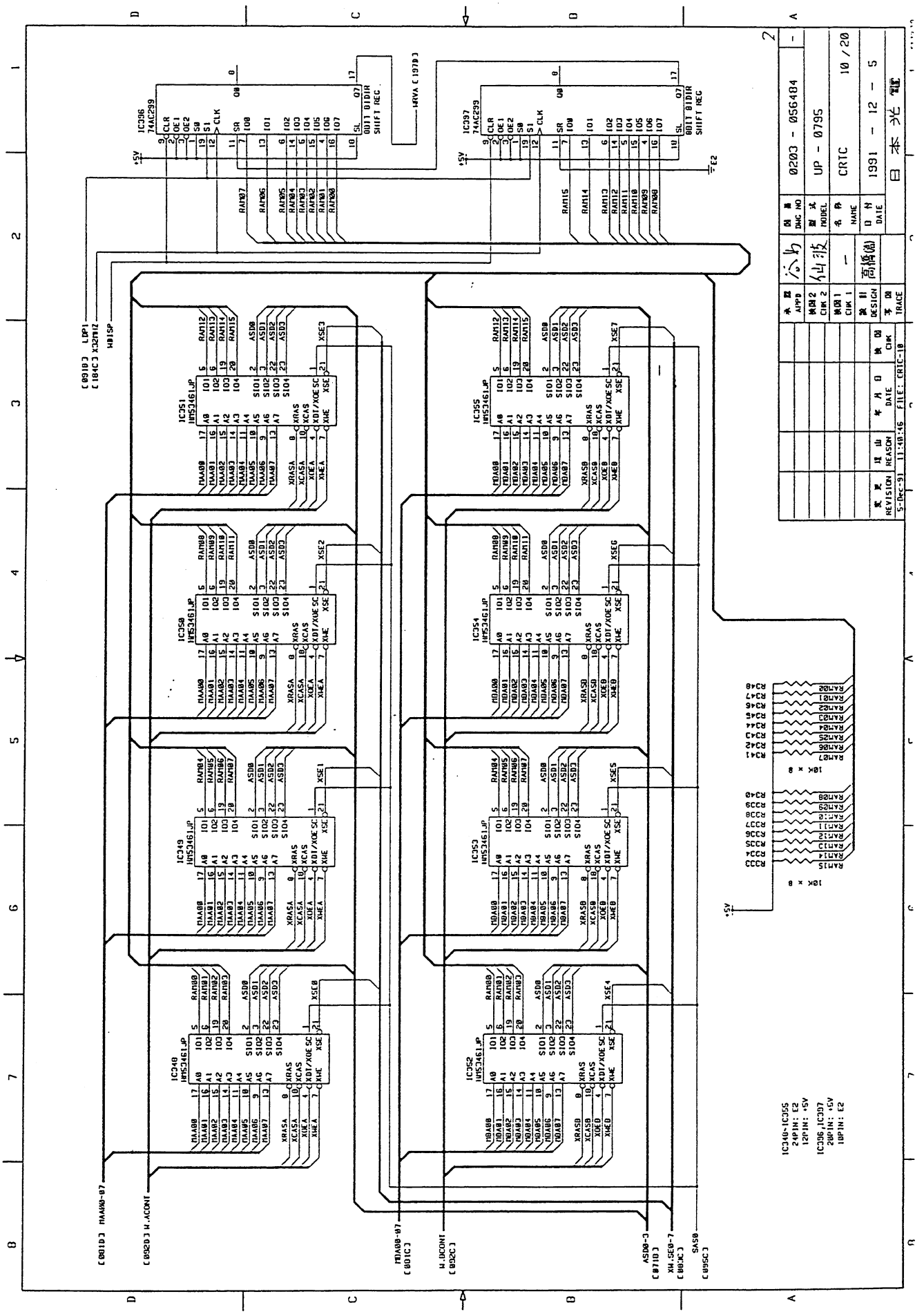

IC329 GAL20V8-15
IC330 GAL20V8-15
IC331 GAL20V8-15
IC332 GAL20V8-15
ENCODER
GAL04
IC323 74AC374
IC324 74AC374
IC325 74AC374
IC326 74AC374
IC327 74AC374
IC328 74AC374
OCTAL D LATCHES
R458 10KJ
R456 10KJ
R457 10KJ
R459 10KJ
R455 10KJ
R451 10KJ
R452 10KJ
R453 10KJ
R454 10KJ
+5V
E2
ASD0-3 [10-00J
BSD0-3 [12-00J
CSD0-3 [14-00J
DASD0-3 [11-00J
DBSD0-3 [13-00J
DCSD0-3 [15-00J
IC323-IC328
20PIN: +5V
10PIN: E2
C18-3C] 16MHZC
C18-3C] X16MHZC
REVISION 29-Mar-96
REASON 変更
DATE 年月日
FILE: CRTC-07
DESIGN 設計
TRACE 手図
CHK 1 検図1
CHK 2 検図2
APPD 承認
DWG NO 図番
MODEL 型式
NAME 名称
DATE 日付
0203 - 056457
UP - 0795
CRTC
7/20
1991 - 12 - 5
日本光電

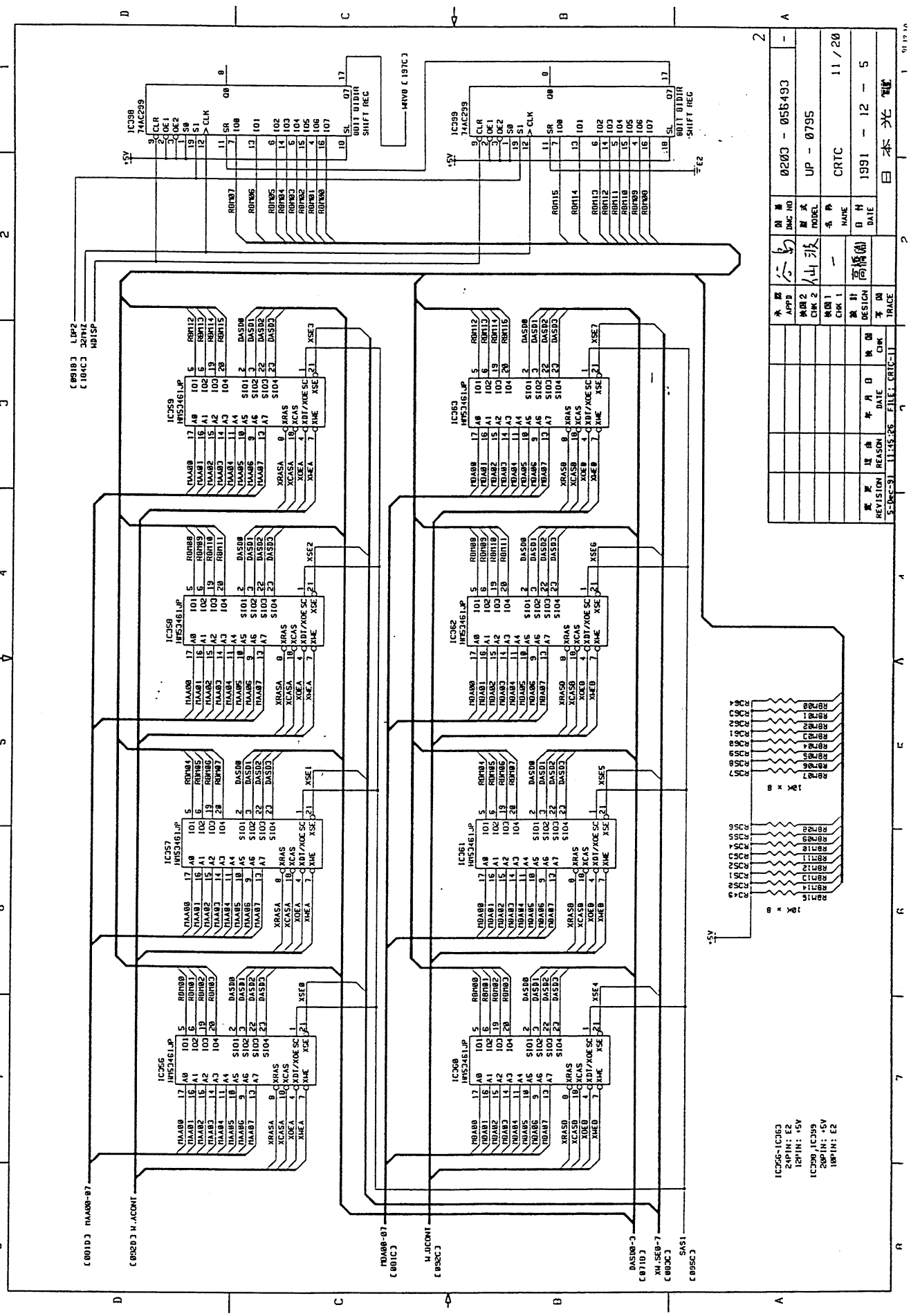
12. CIRCUIT DIAGRAM



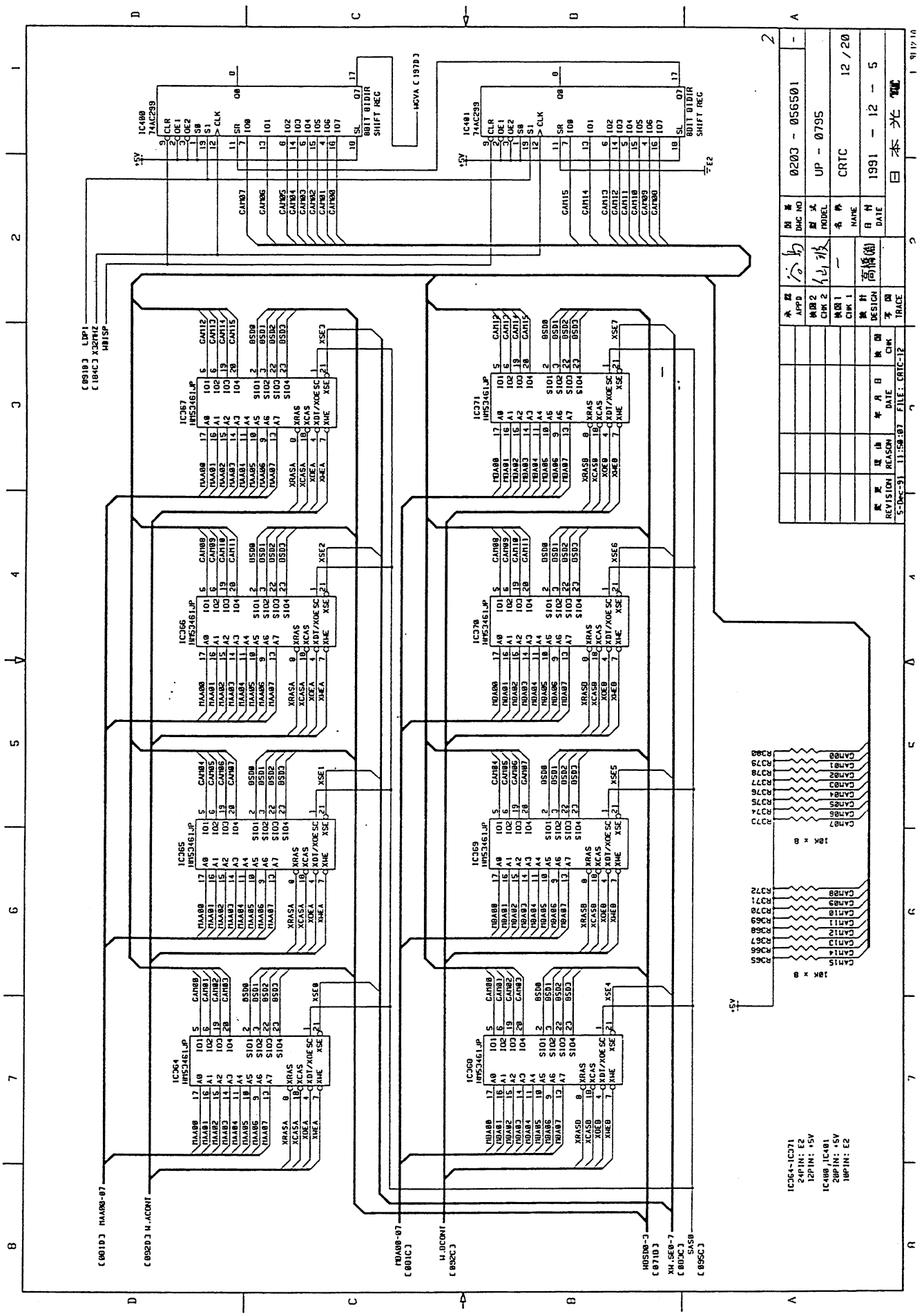

W.ACONT C10-0D3 C12-0D3 C13-0D3 C14-0D3 C15-0D3 C11-0D3
W.BCONT C10-0C3 C12-0C3 C13-0C3 C14-0C3 C15-0C3 C11-0C3
LDP1 C10-3D3 C12-3D3 C13-3D3 C14-3D3 C15-3D3
LDP2 C11-3D3 C12-3D3 C13-3D3 C14-3D3 C15-3D3
47 × 8
R325 R326 R327 R328 R329 R330 R331 R332
XRASA XCASA XWEA XOEA XRASB XCASB XWEB XOEB
R431 10K
IC343 CAL20V8-15 HVRC09 CAL09
IC341 CAL16V8-15 HVRC07 CAL07
IC342 CAL16V8-15 HVRC08 CAL08
IC340 CAL16V8-15 HVRC06 CAL06
R469 10KJ
R467 10KJ
R468 10KJ
R466 10KJ
R429 47
R430 47
R432 10K
R470 10KJ
IC346 A 74AC74
IC346 B 74AC74
IC347 A 74AC08
IC347 B 74AC08
IC347 D 74AC08
IC409 A 74AC74
IC409 B 74AC74
IC344 A 74AC74
IC344 B 74AC74
IC345 74AC164
8BIT SHIFT REGISTER
IC687 C 74F04
PRE CLR FF1 FF2
C10-3C3 32MHZ
C10-3C3 X32MHZ
C08-6D3 XH30
C08-6D3 2MHZ
C13-3D3 C14-3D3 C15-3D3
C10-3D3 C11-3D3 C12-3D3
HDISP C10-3D3
C08-7C3 XHSYNCD
C15-8A3 C13-8A3
C11-8A3
SAS1
SAS0 C10-8A3 C14-8A3
C12-8A3
C10-3C3 16MHZ
C08-6D3 DSLD
C08-6D3 DDISP1
C10-3C3 X16MHZC
C08-6D3 2MHZ
C08-3C3 SAS
C02-6A3 HSYNC
IC344-IC347,IC409
14PIN: +5V
7PIN: E2
IC687A,B,D,E,F:10PACE
REVISION 21-Sep-96 REASON 16:28:32 DATE 96.09.25 FILE: CRTC-09
承認 APPD 96.9.27
検図2 CHK 2
検図1 CHK 1 96.9.26
設計 DESIGN 高橋(伯)
手図 TRACE
検図 CHK
図番 DWG NO 0203 - 056475 A
型式 MODEL UP - 0795
名称 NAME CRTC 9/20
日付 DATE 1991 - 12 - 5
日本光電

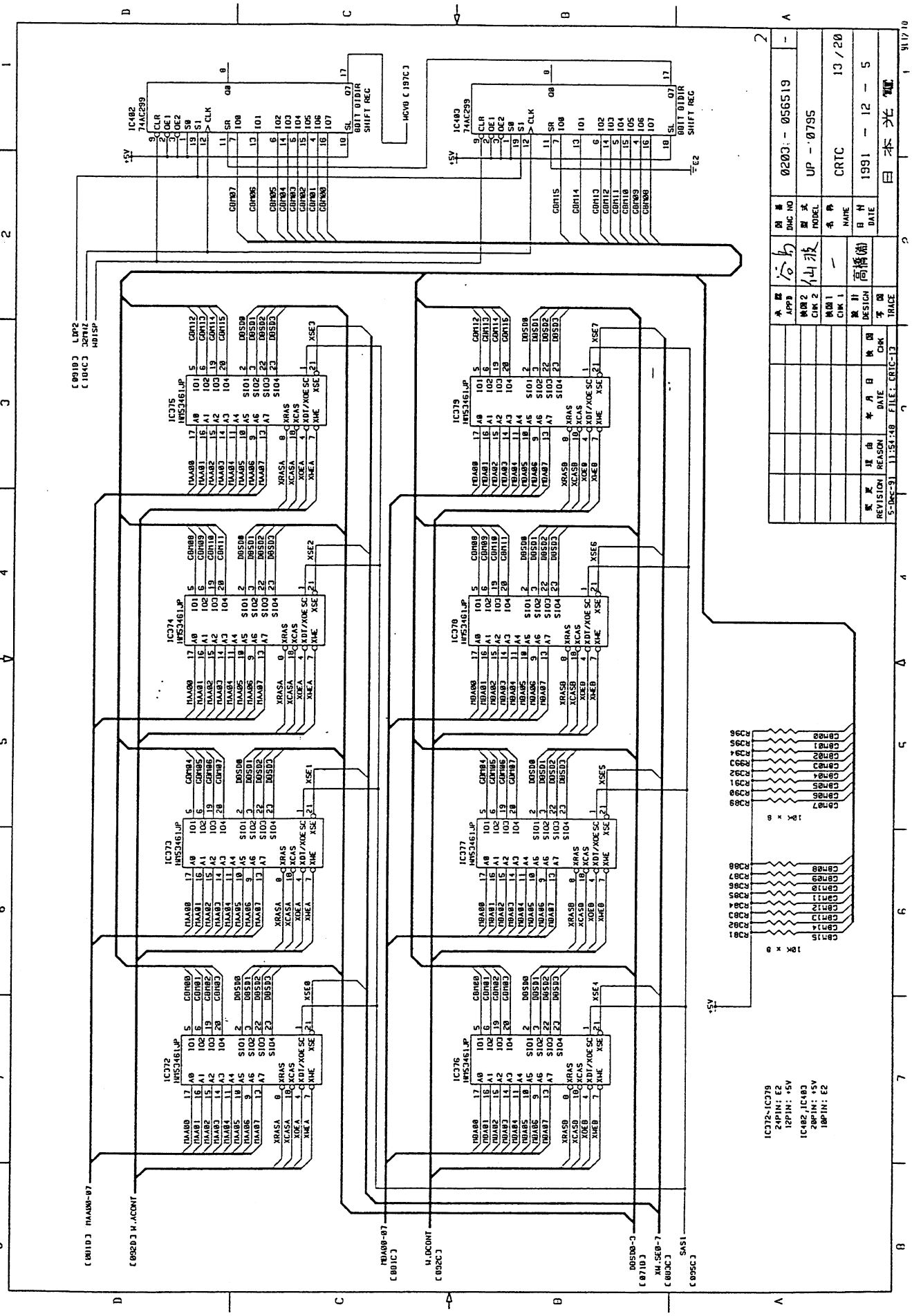
12. CIRCUIT DIAGRAM



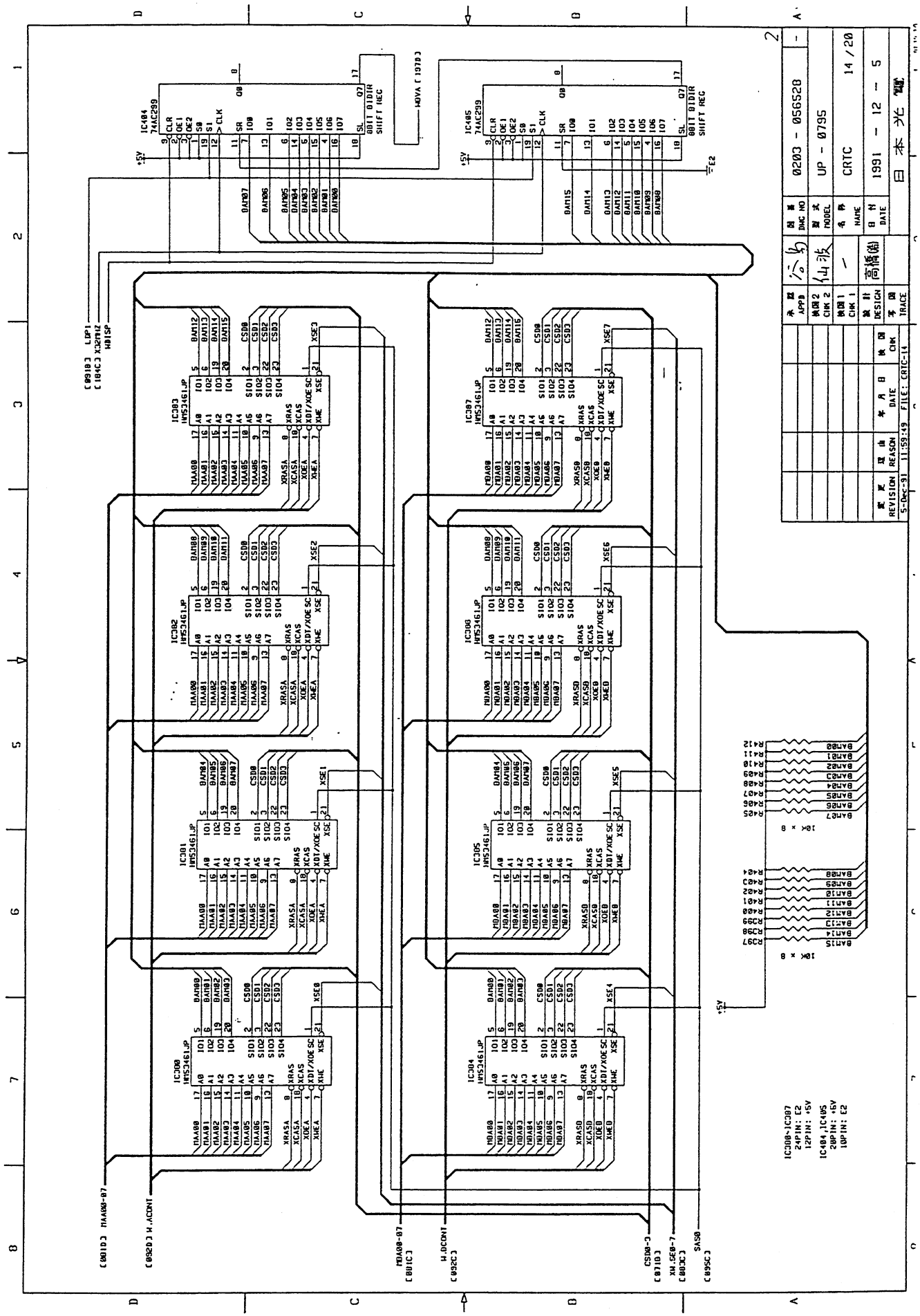


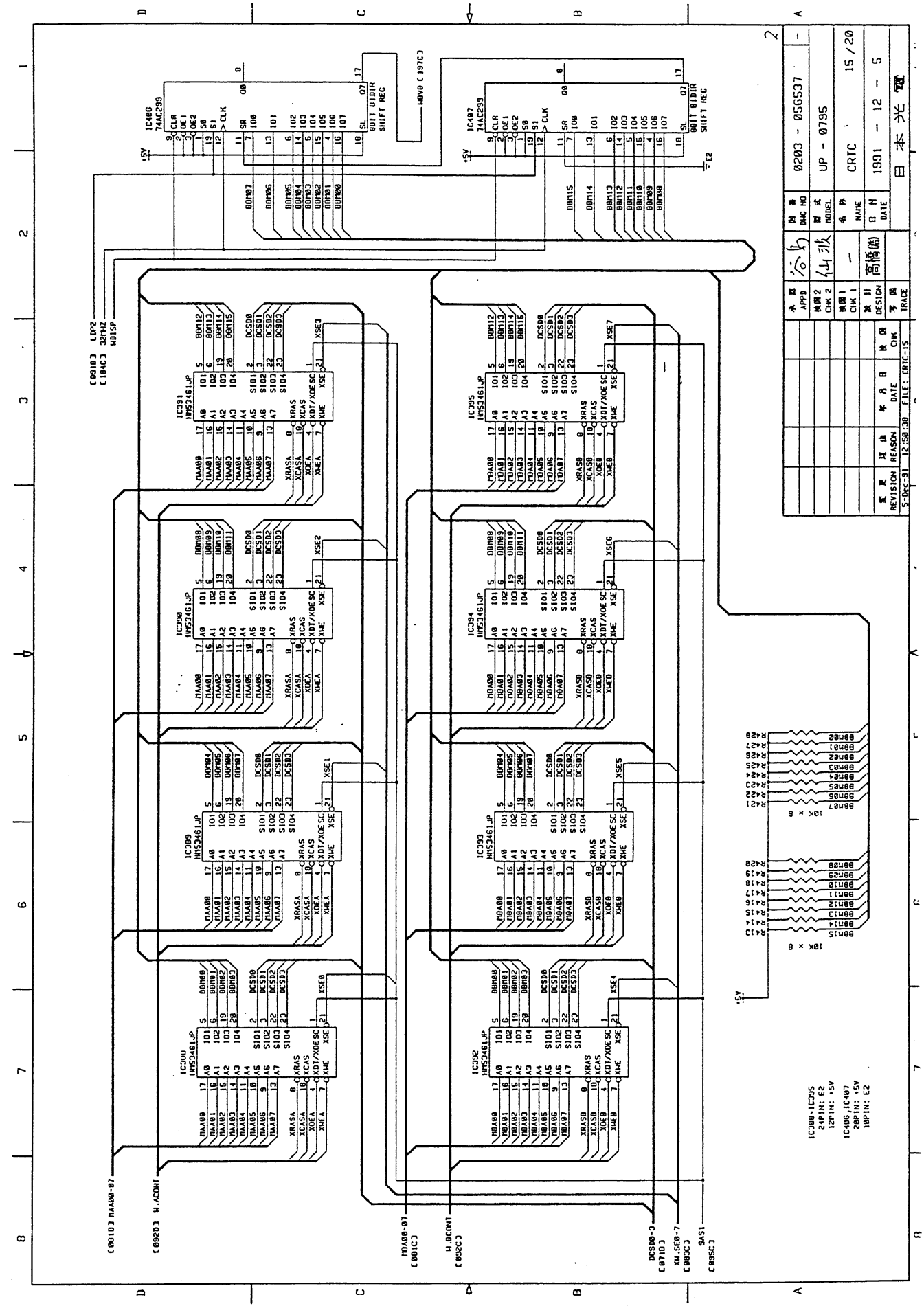
12. CIRCUIT DIAGRAM



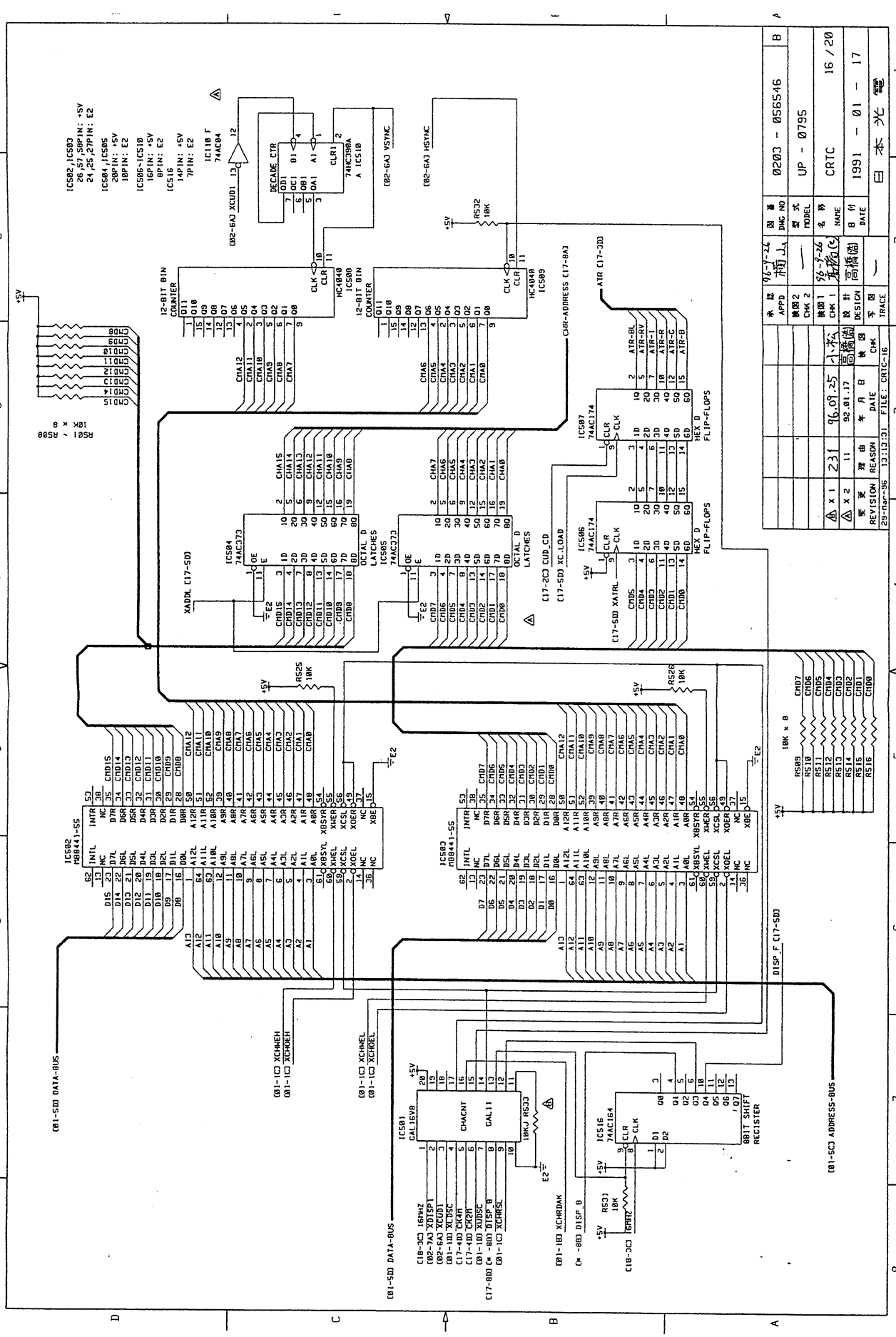

IC372-IC379
24PIN: E2
12PIN: +5V
IC402,IC403
20PIN: +5V
18PIN: E2
REVISION 5-Dec-91
REASON
DATE 11:54:48
FILE: CRTC-13
DWG NO 0203-056519
MODEL UP-0795
NAME CRTC
DATE 1991-12-5
SHEET 13/20

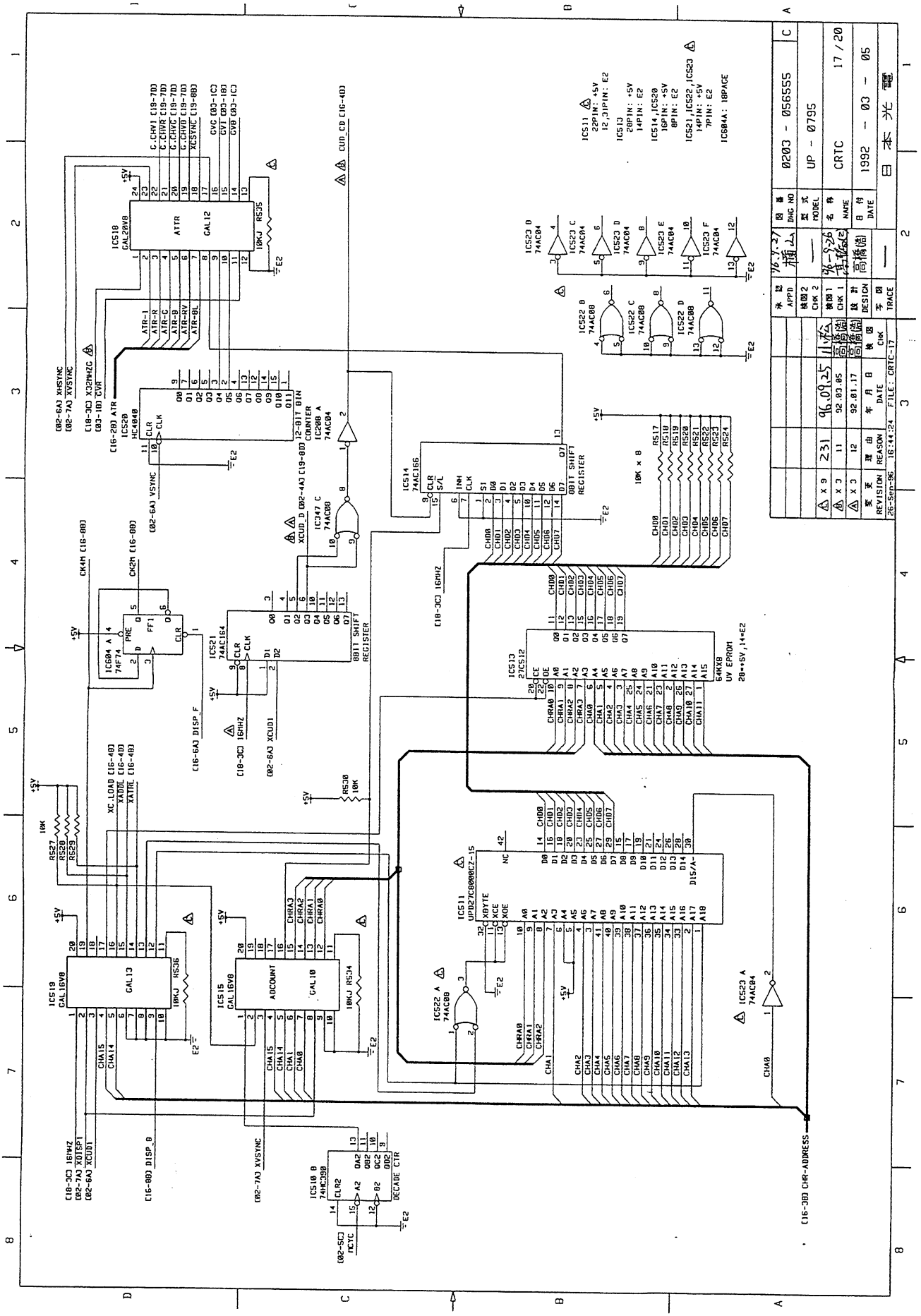
12. CIRCUIT DIAGRAM



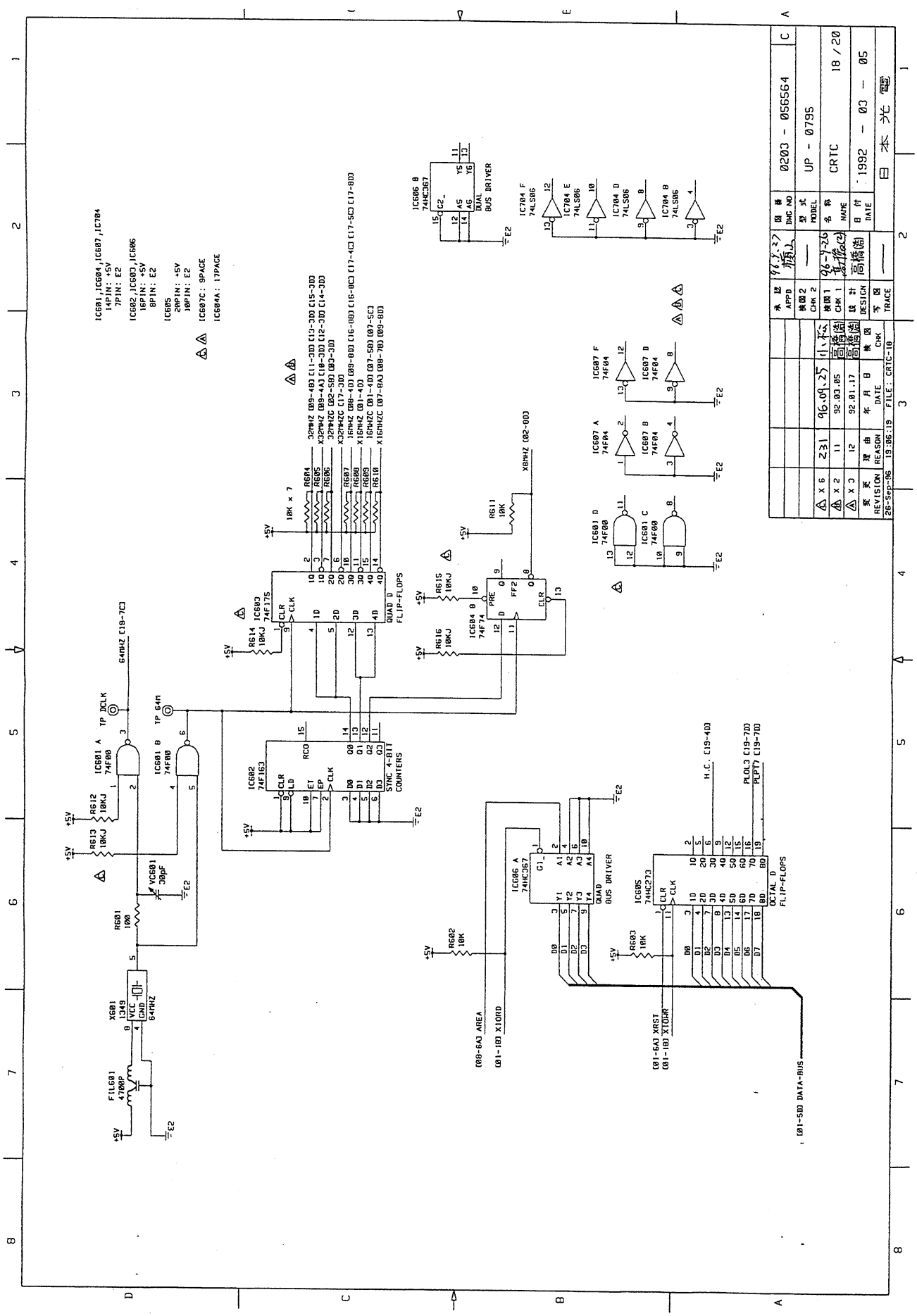


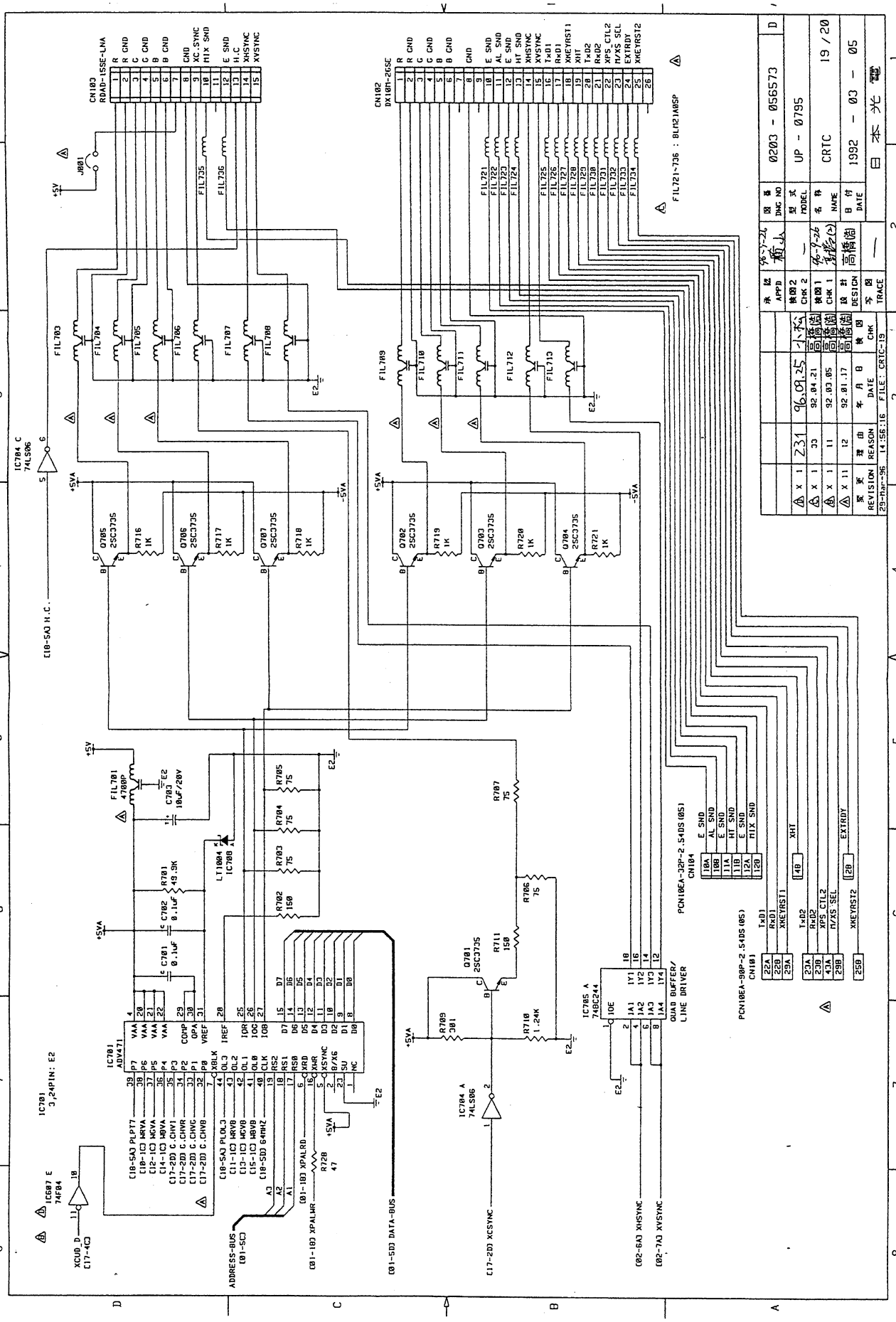
12. CIRCUIT DIAGRAM



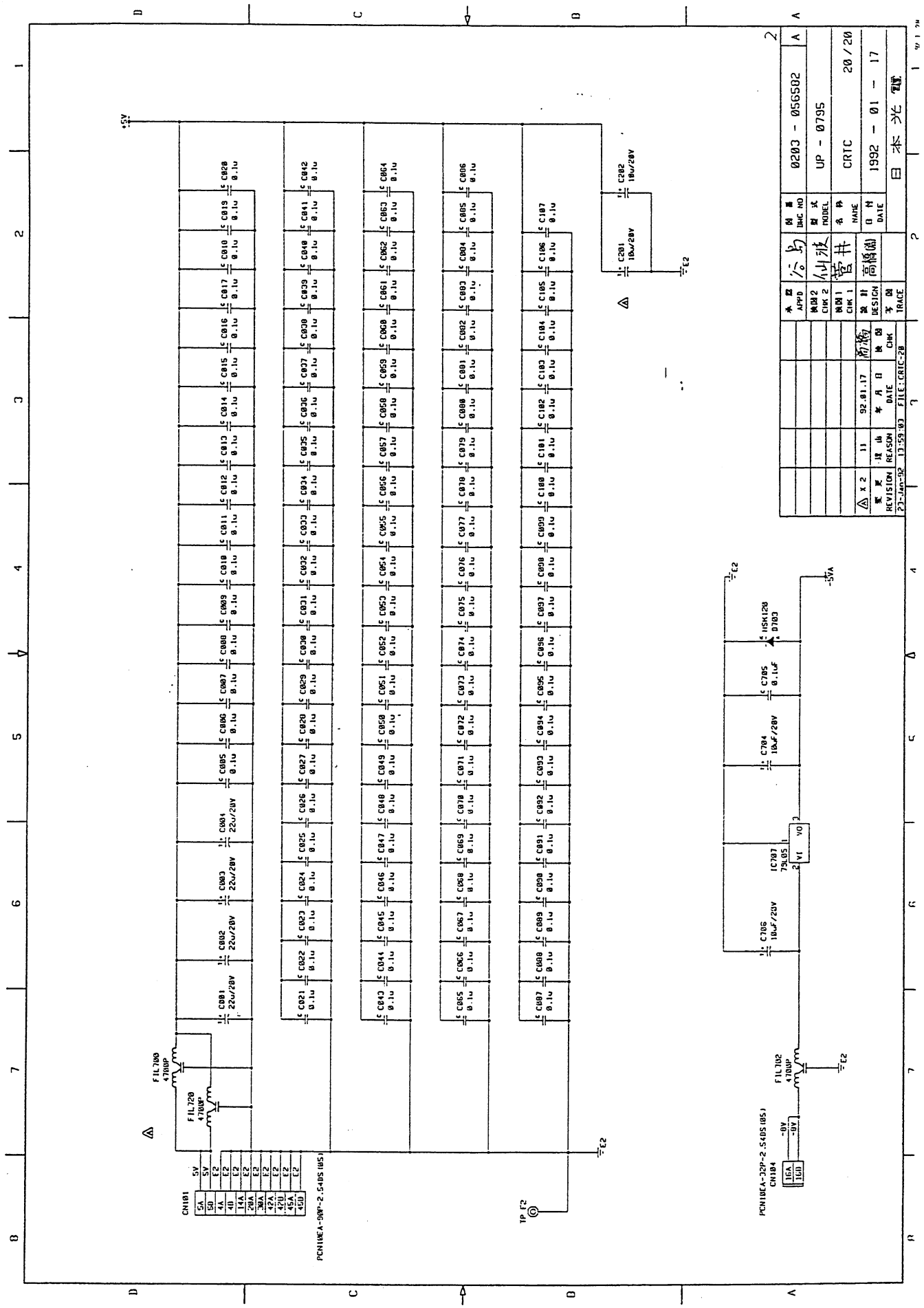


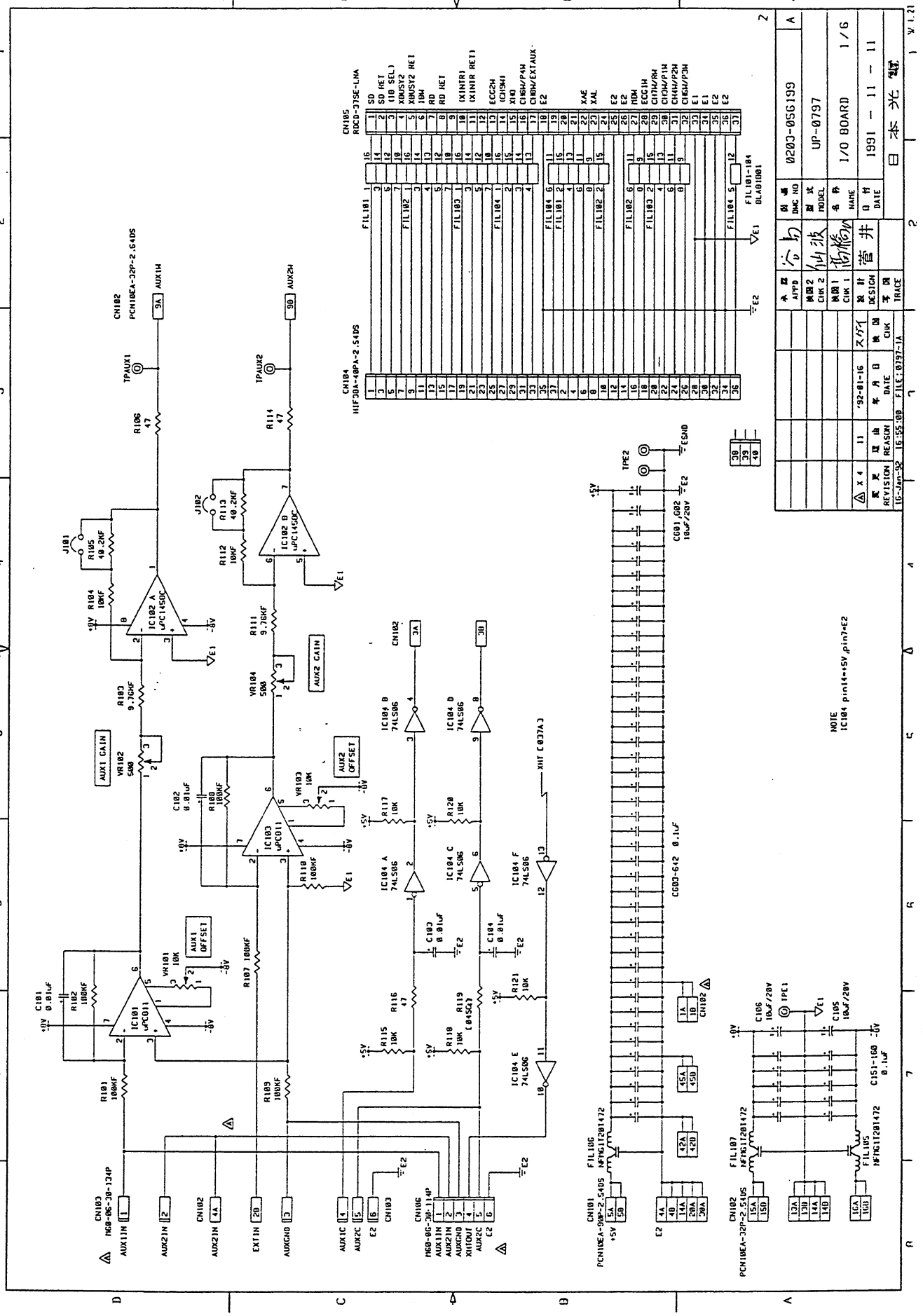
12. CIRCUIT DIAGRAM



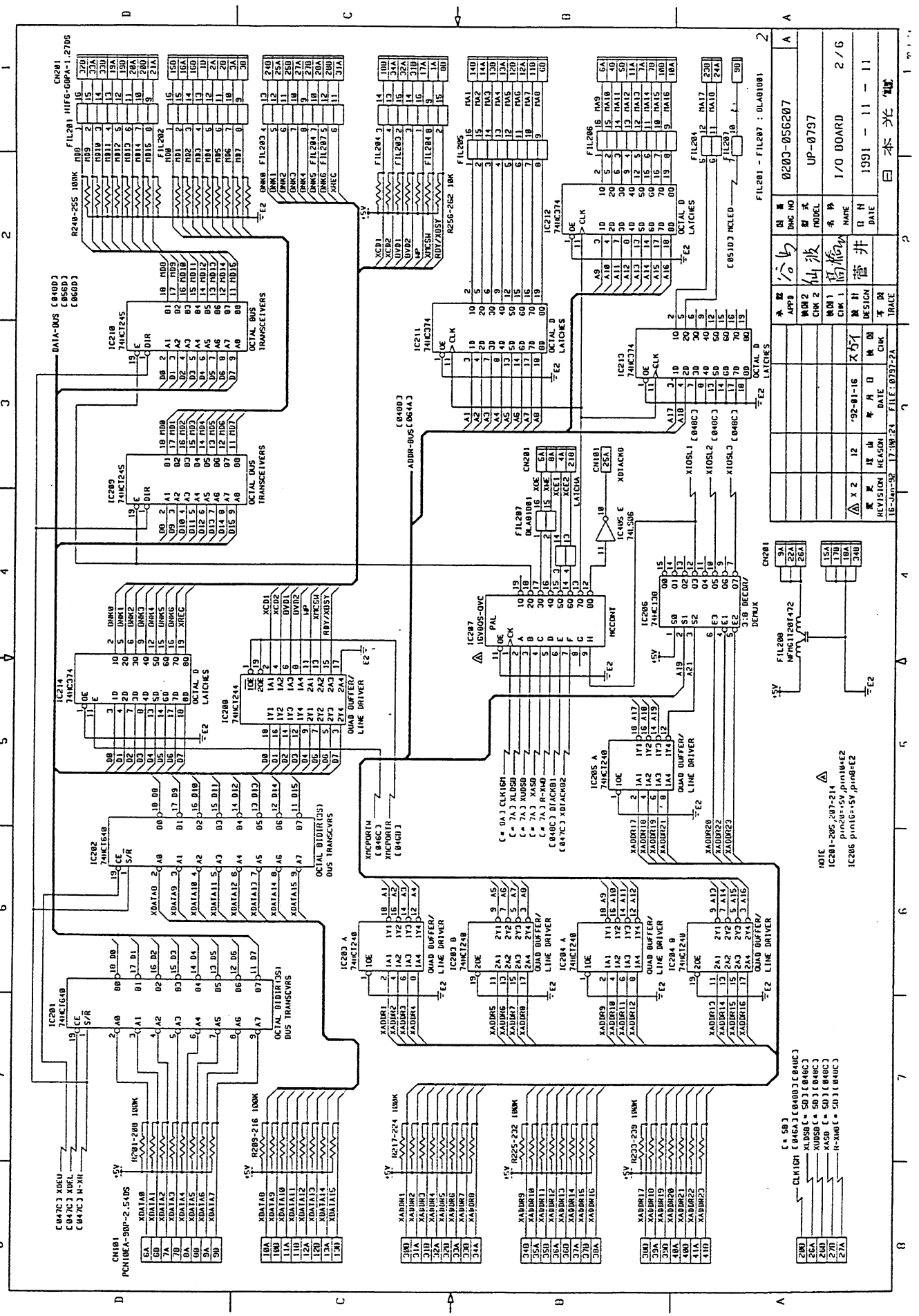


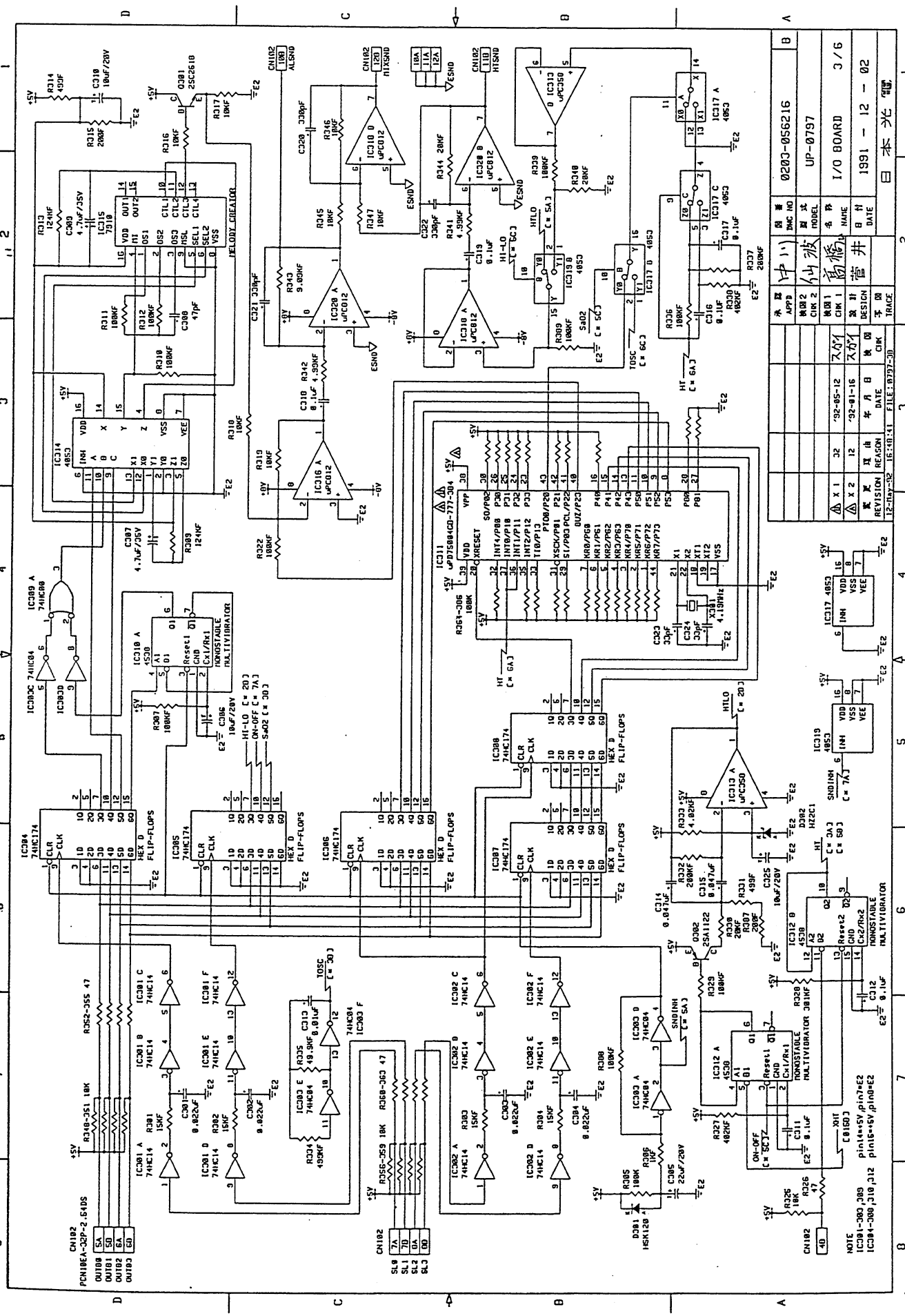
12. CIRCUIT DIAGRAM



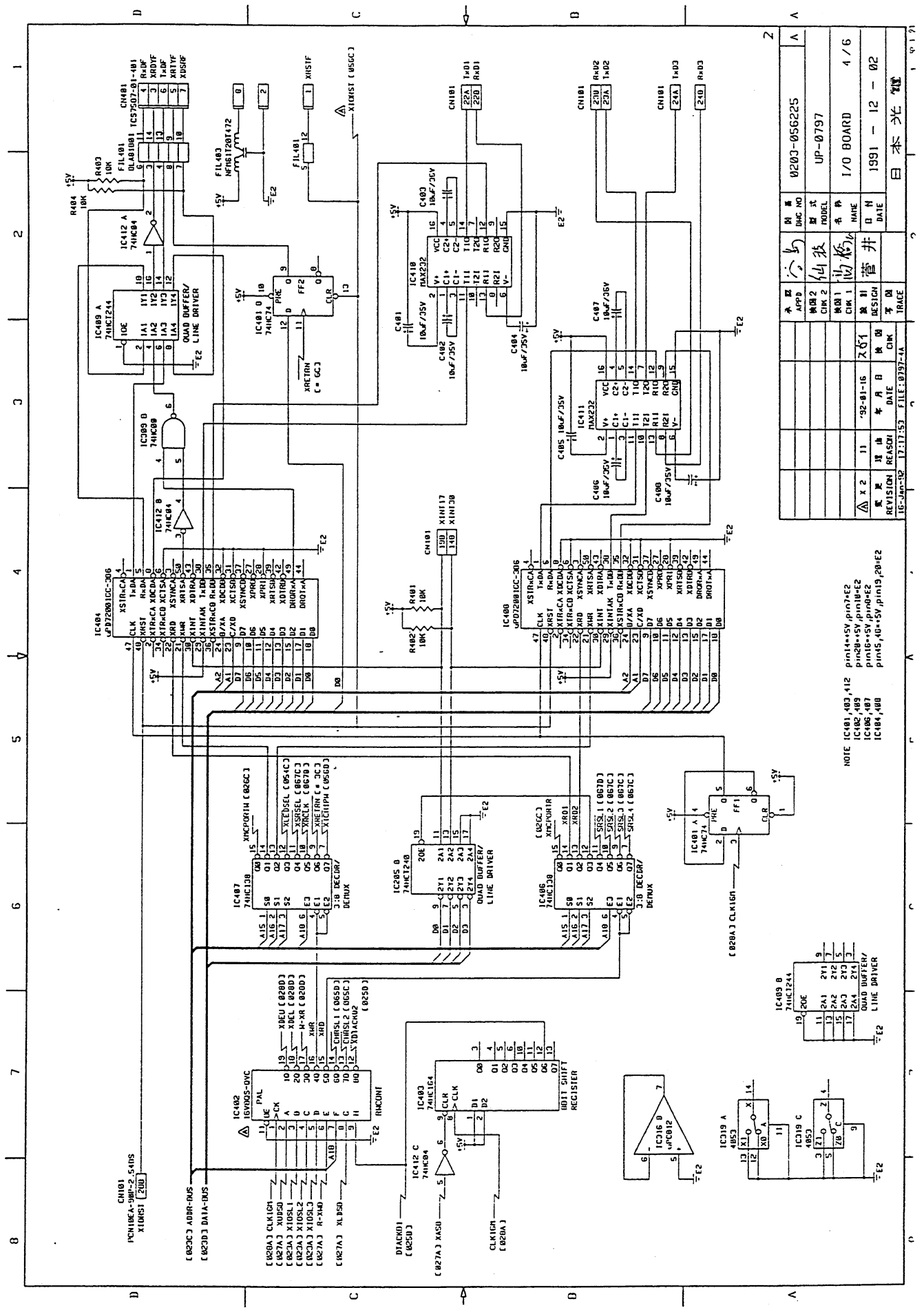


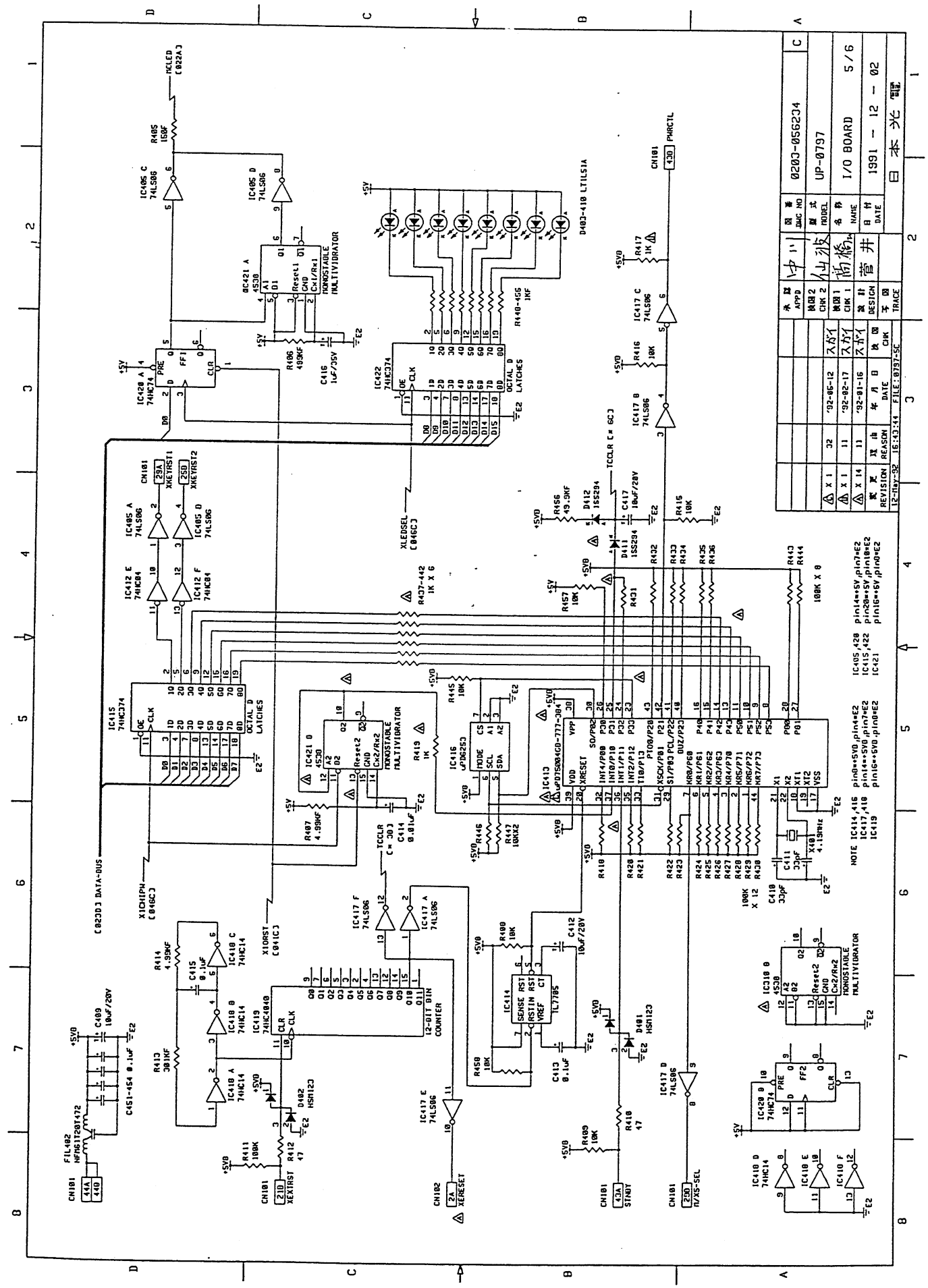
12. CIRCUIT DIAGRAM



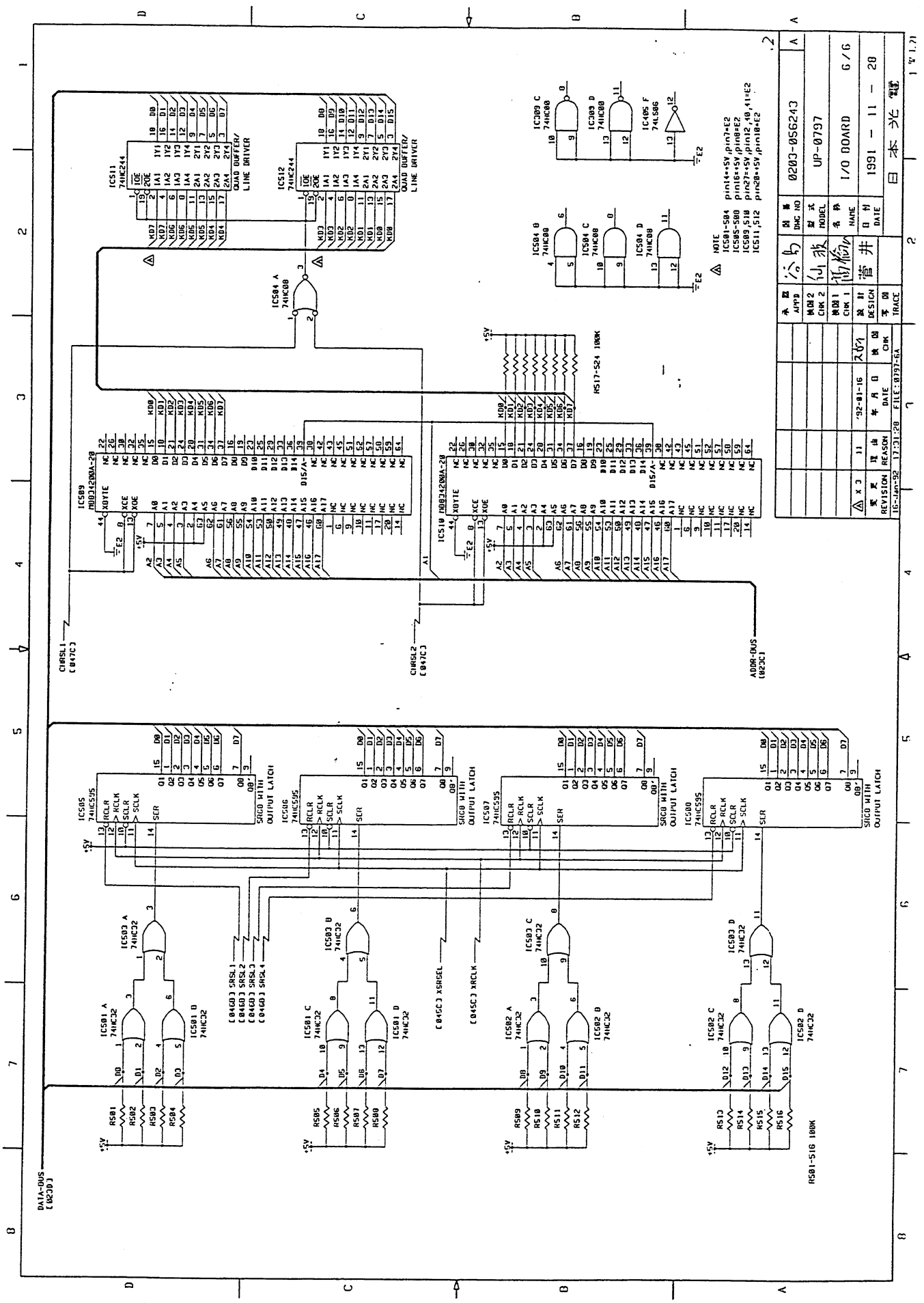


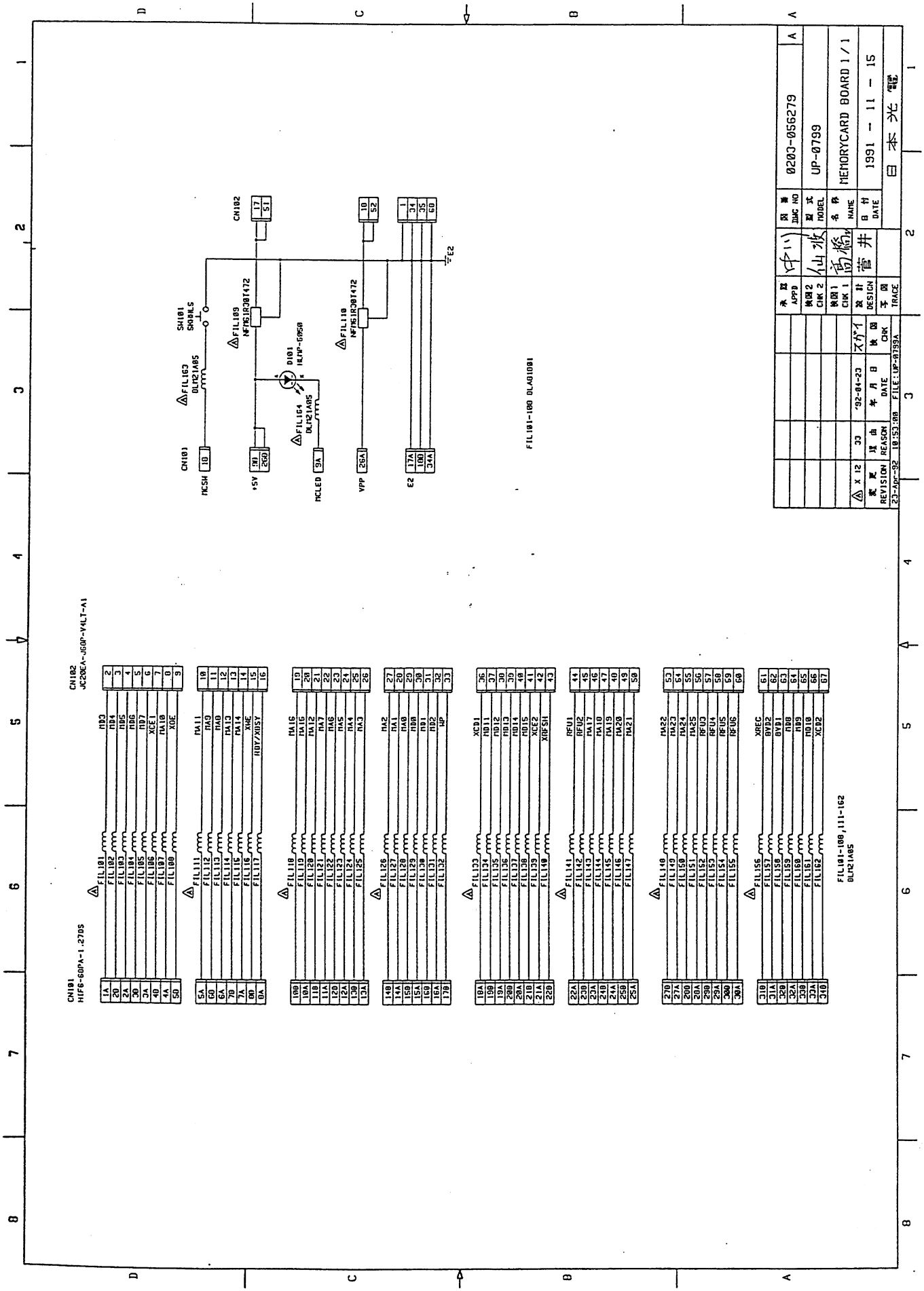
12. CIRCUIT DIAGRAM



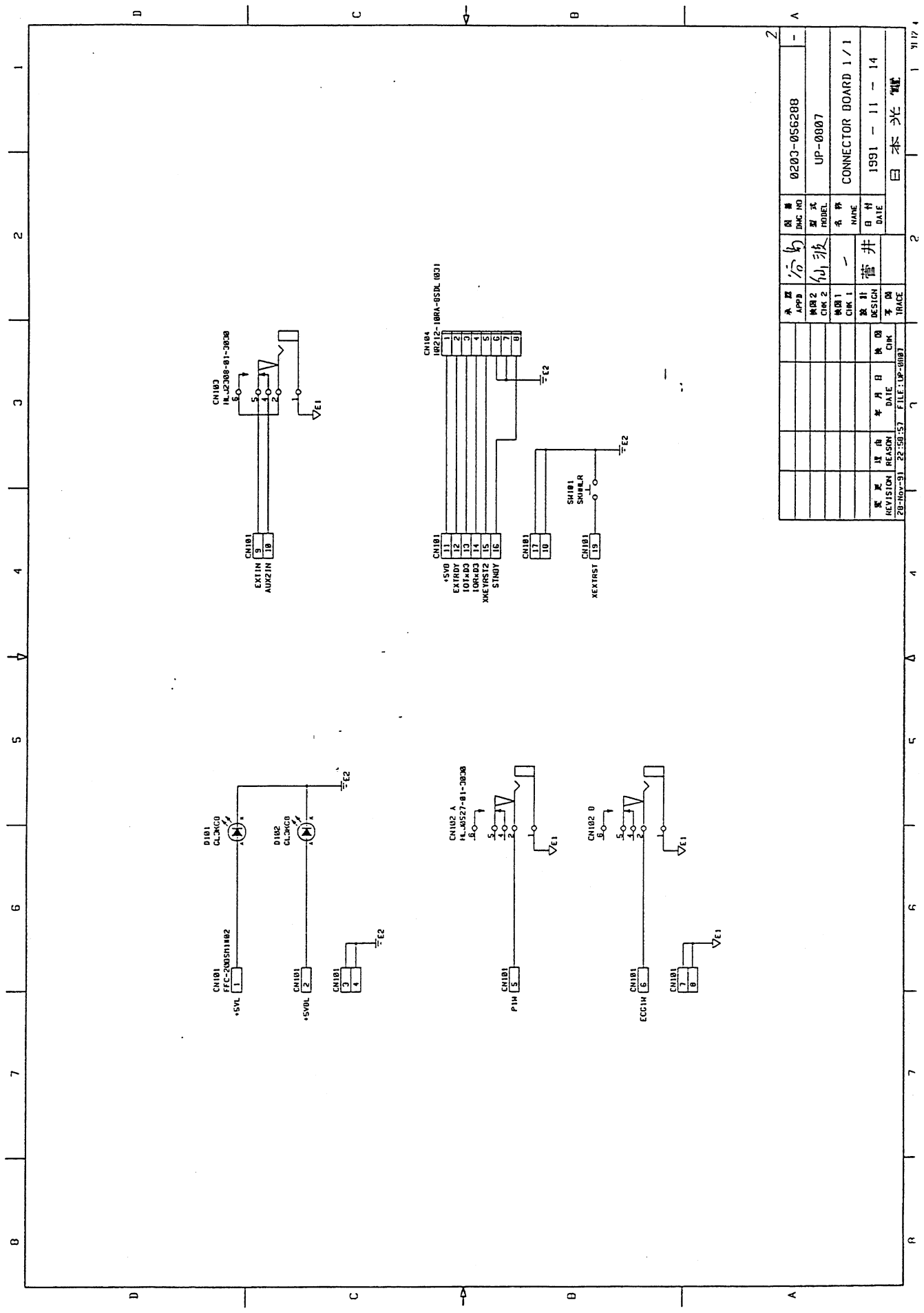

0203-056234
UP-0797
I/O BOARD 5/6
1991 - 12 - 02
日本光電
IC405 C 74LS06
IC405 D 74LS06
IC421 A 4538
IC422 74HC374
OCTAL D LATCHES
IC420 A 74HC74
IC405 A 74LS06
IC405 D 74LS06
IC412 E 74HC04
IC412 F 74HC04
IC415 74HC374
IC421 B 4538
IC416 μPD9625
IC413 μPD75004CD-777-3B4
IC417 B 74LS06
IC417 C 74LS06
IC417 F 74LS06
IC417 A 74LS06
IC414 TL7705
IC417 D 74LS06
IC417 E 74LS06
IC419 74HC4040
12-BIT BIN COUNTER
IC418 A 74HC14
IC418 B 74HC14
IC418 C 74HC14
IC420 B 74HC74
IC418 D 74HC14
IC418 E 74HC14
IC418 F 74HC14
IC410 B 4538
D403-410 LTL1S1A
D411 1SS294
D412 1SS294
D401 HSM123
D402 HSM123
FIL402 NFM61T20T472
X410 4.19MHz
CN101 PWRCTL
CN101 XKEYRST1
CN101 XKEYRST2
CN101 XEXTRST
CN101 START
CN101 AVSS-SEL
CN102 XERESET
XLEDSEL [846CJ]
XCHIPN [846CJ]
X10RST [841CJ]
[802DJ DATA-BUS
TCCLR [* 6CJ]
TCCLR [* 30J]
MONOSTABLE MULTIVIBRATOR
OCTAL D LATCHES
R437-442 1K X 6
100K X 8
100K X 12
NOTE IC414,416 IC417,418 IC419
IC405,420 IC415,422 IC421
pin8=5V0,pin4=E2
pin14=5V0,pin7=E2
pin16=5V0,pin8=E2
pin20=5V,pin10=E2
pin16=6V,pin0=E2
REVISION 12-Nov-92 16:43:44 FILE:0797-SC
DESIGN TRACE CHK APPD DATE

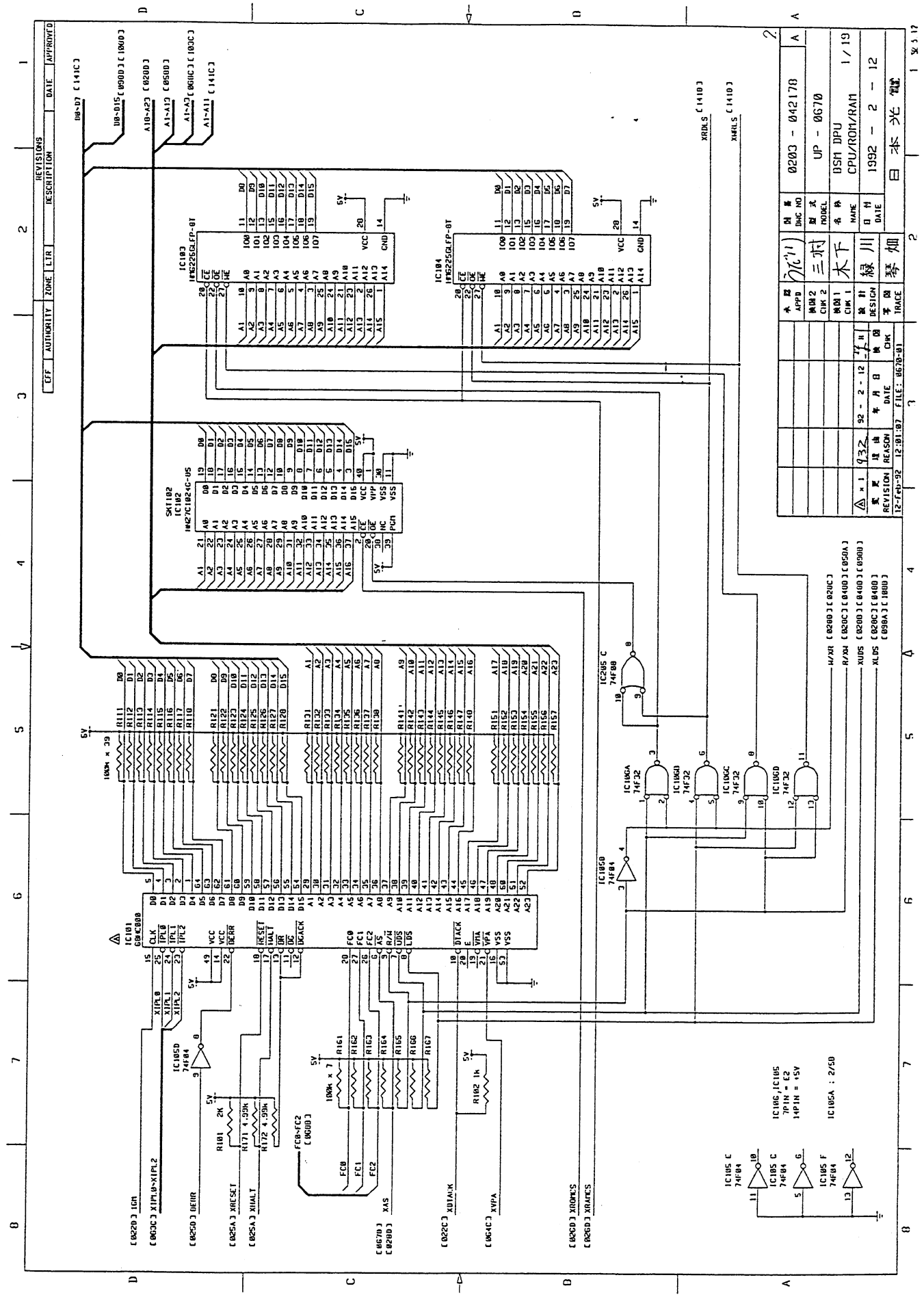
12. CIRCUIT DIAGRAM



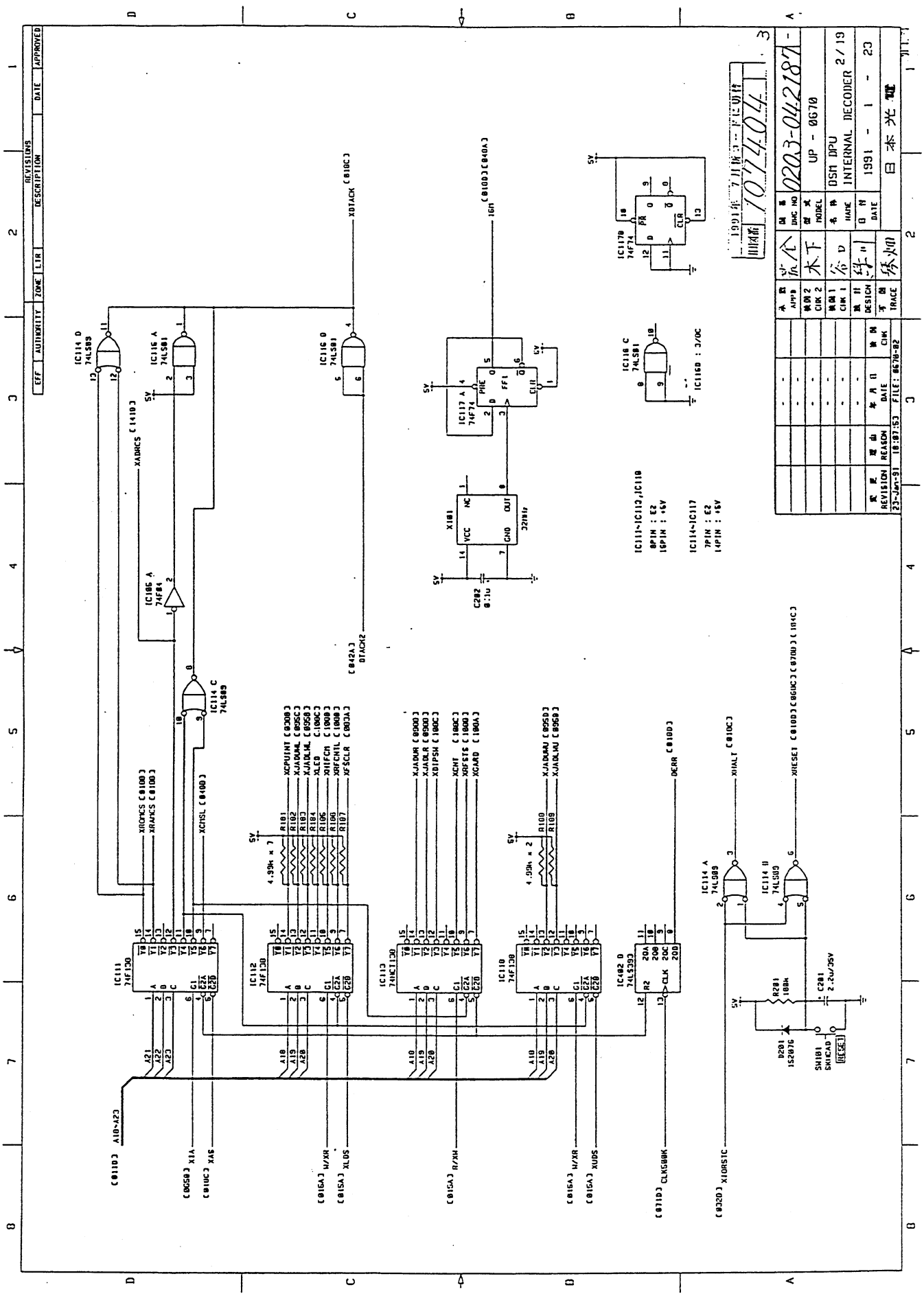

CN101
HIF6-60PA-1.27DS
CN102
JC20EA-J60P-V4LT-A1
FIL101-180 DLA01081
FIL101-180,111-162
DLR21A05
CN101
MCSW
FIL163
DLR21A05
SH101
SG08LS
FIL164
DLR21A05
D101
MLNP-G050
MCLED
FIL109
NFM61R30T472
FIL110
NFM61R30T472
CN102
+5V
VPP
E2
REVISION
REASON
DATE
CHK
DESIGN
TRACE
APPD
CHK 2
CHK 1
DWG NO
MODEL
NAME
DATE
0203-056279
UP-0799
MEMORYCARD BOARD 1 / 1
1991 - 11 - 15
日本光電
23-Apr-92 10:53:00
FILE : UP-0799A

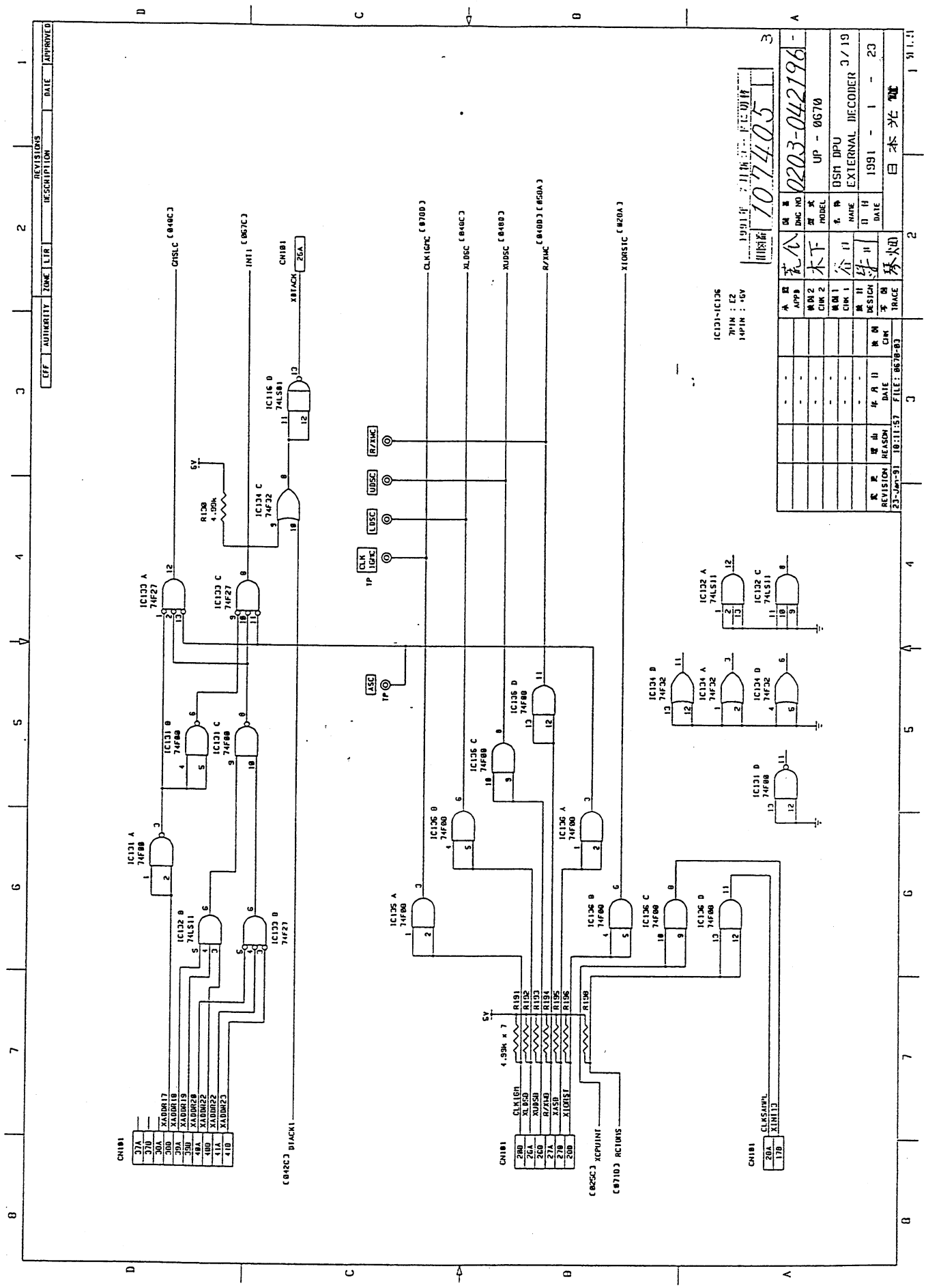
12. CIRCUIT DIAGRAM



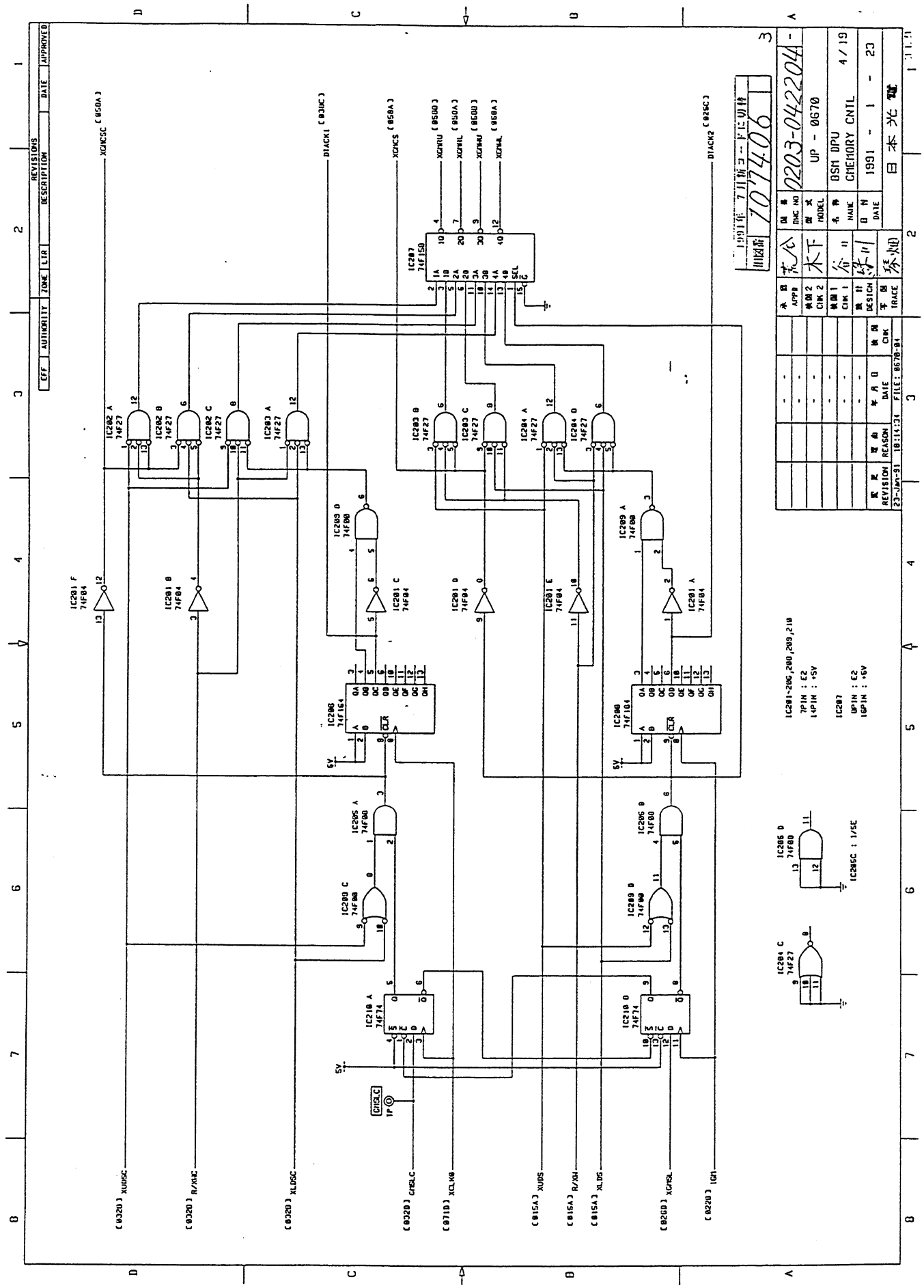


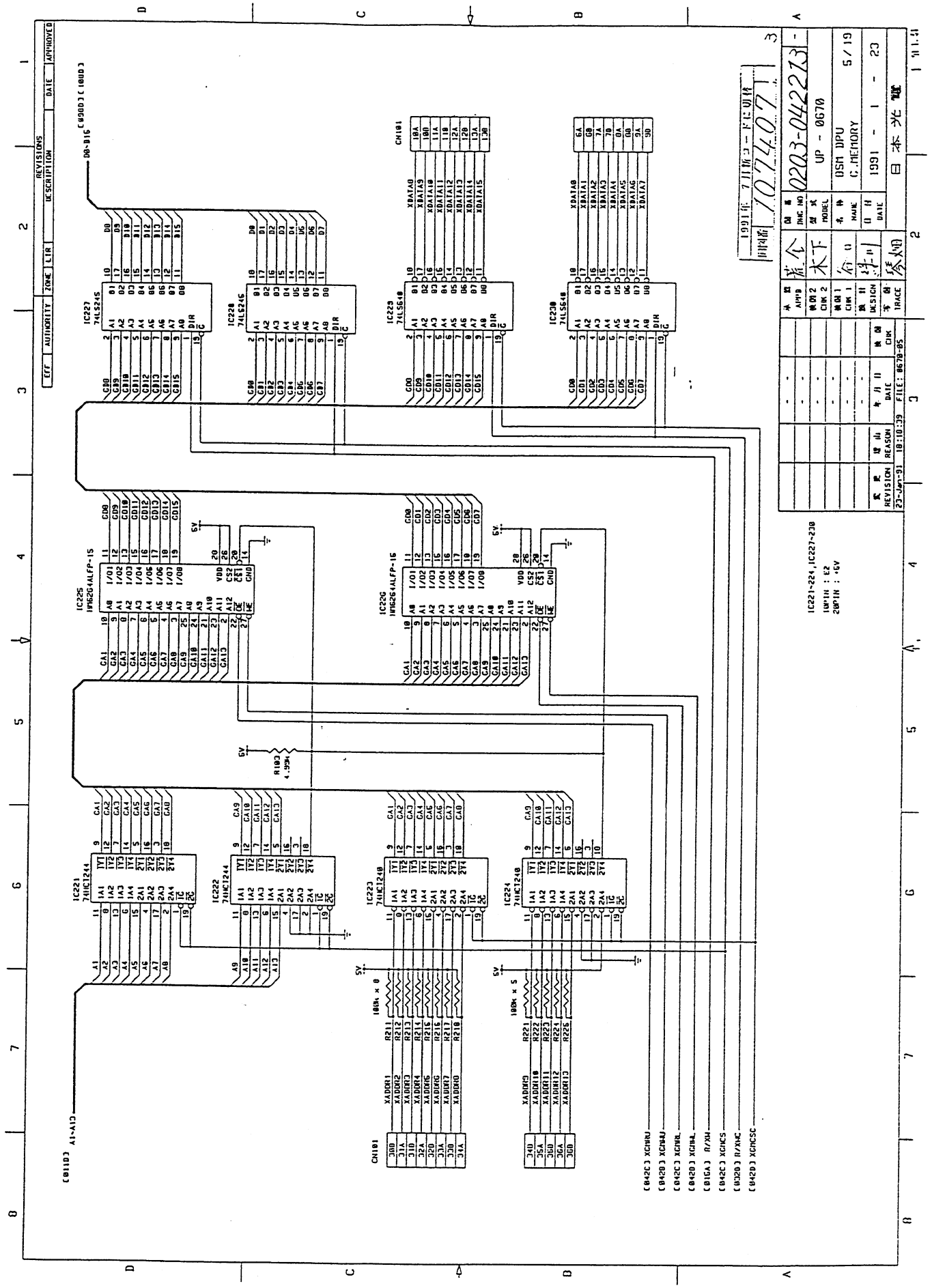
12. CIRCUIT DIAGRAM



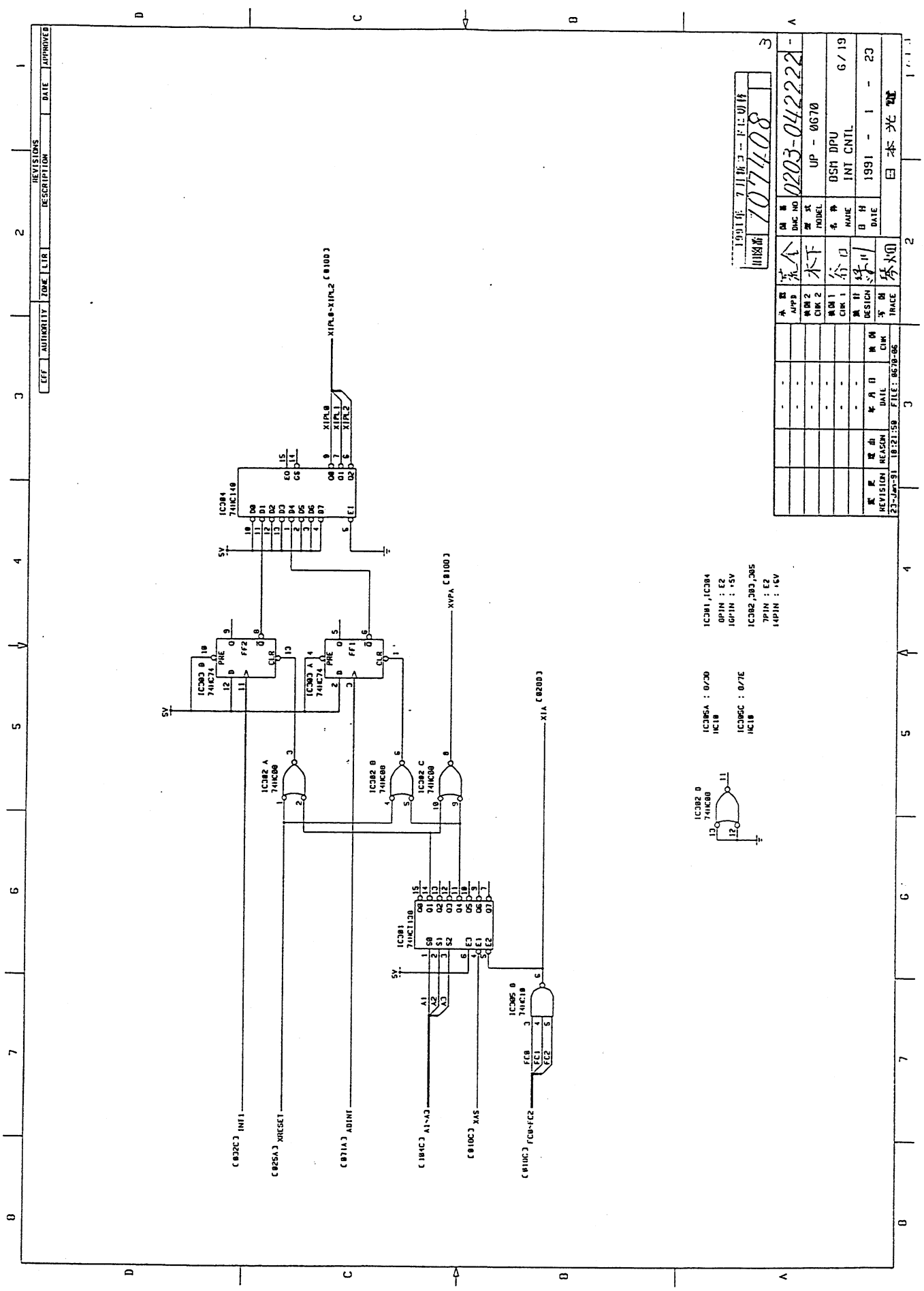


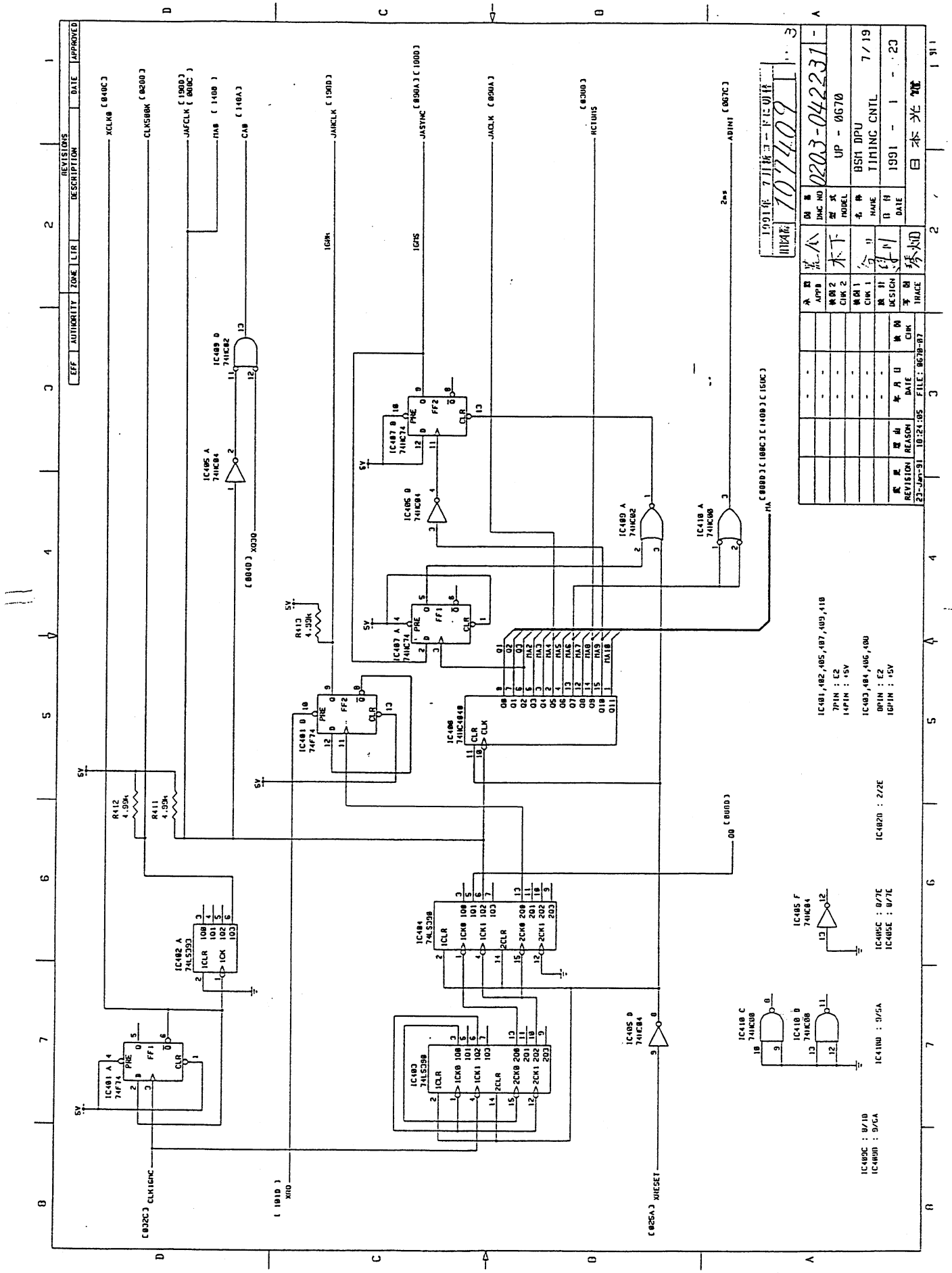
12. CIRCUIT DIAGRAM



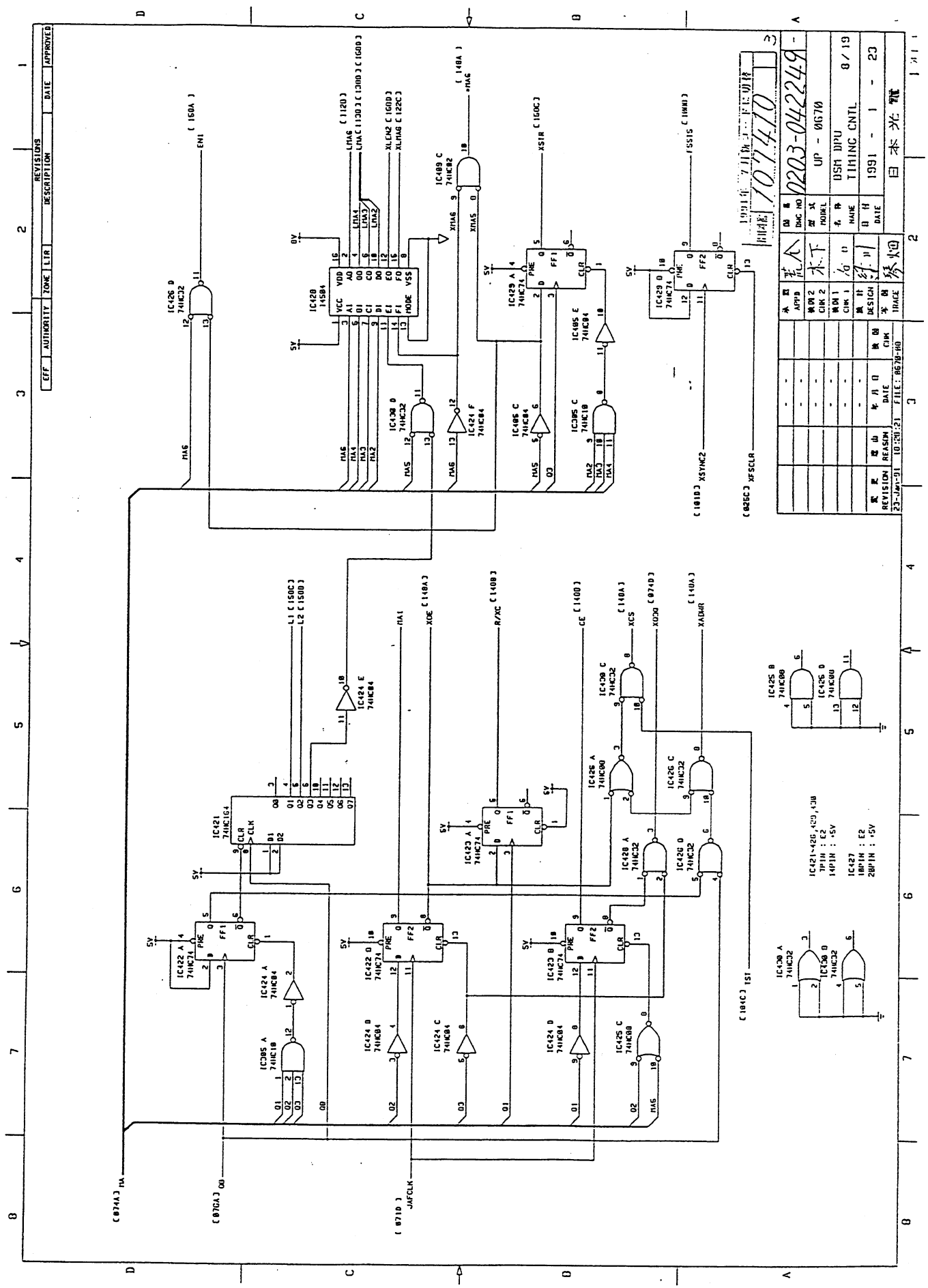


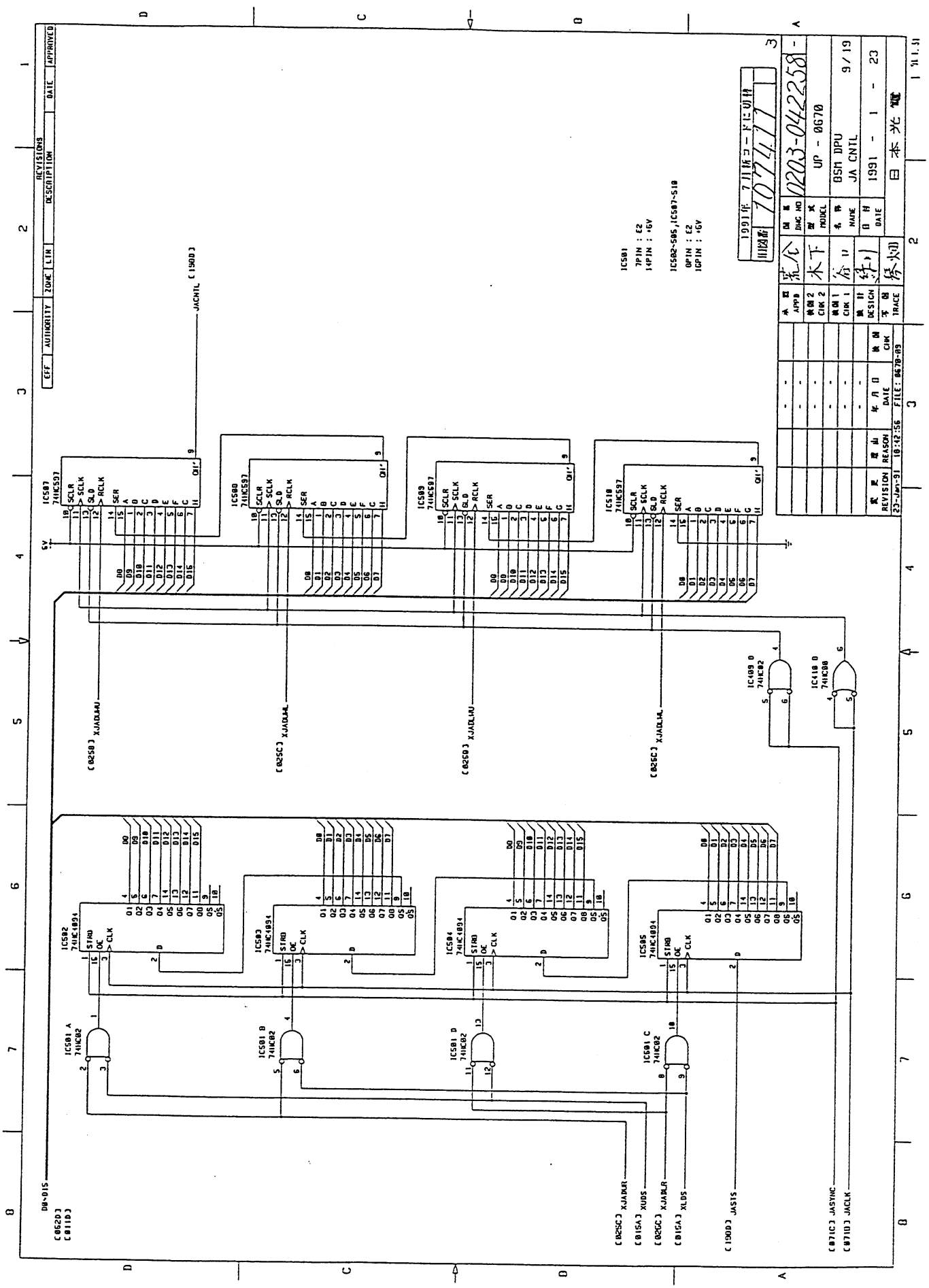
12. CIRCUIT DIAGRAM



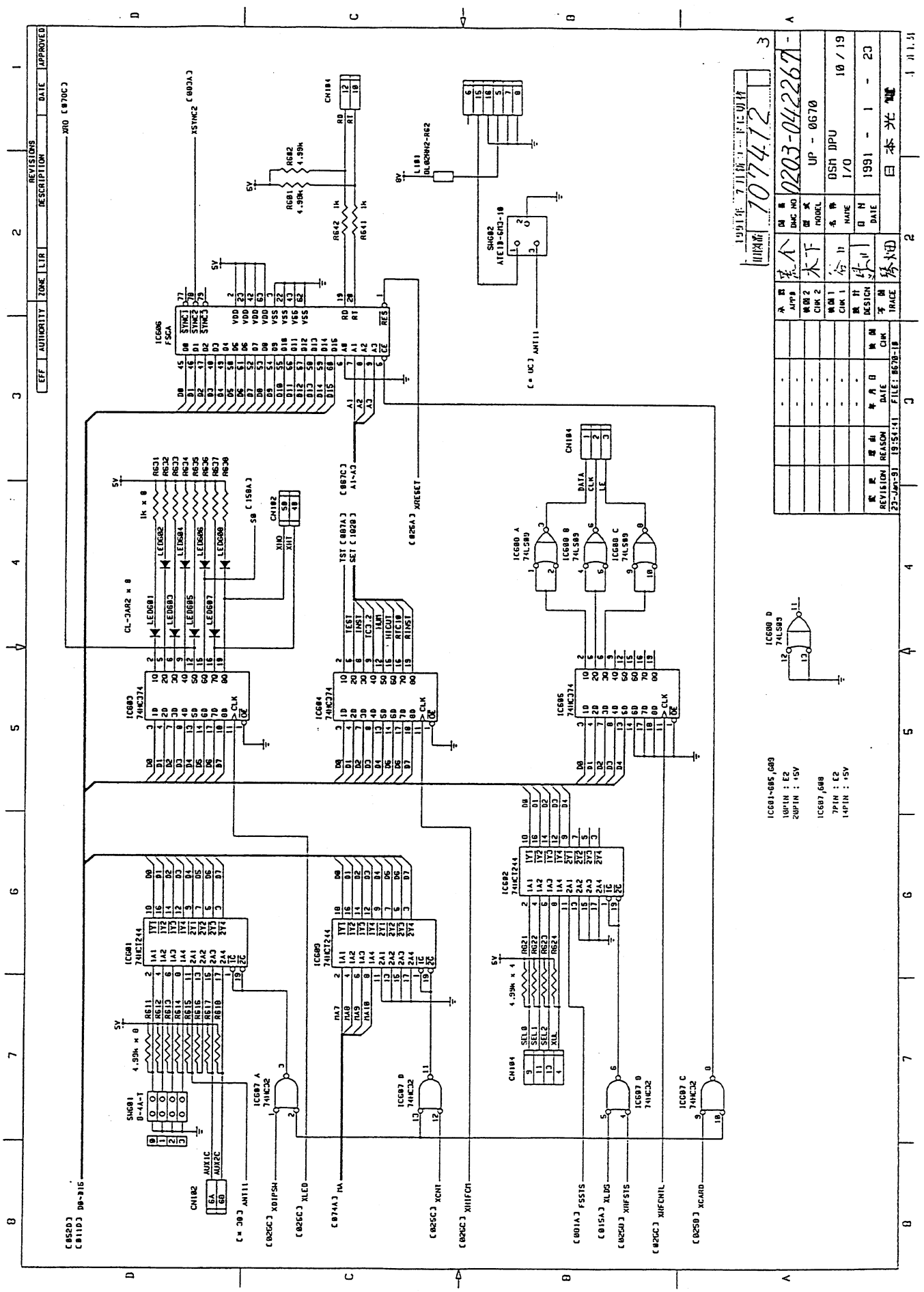


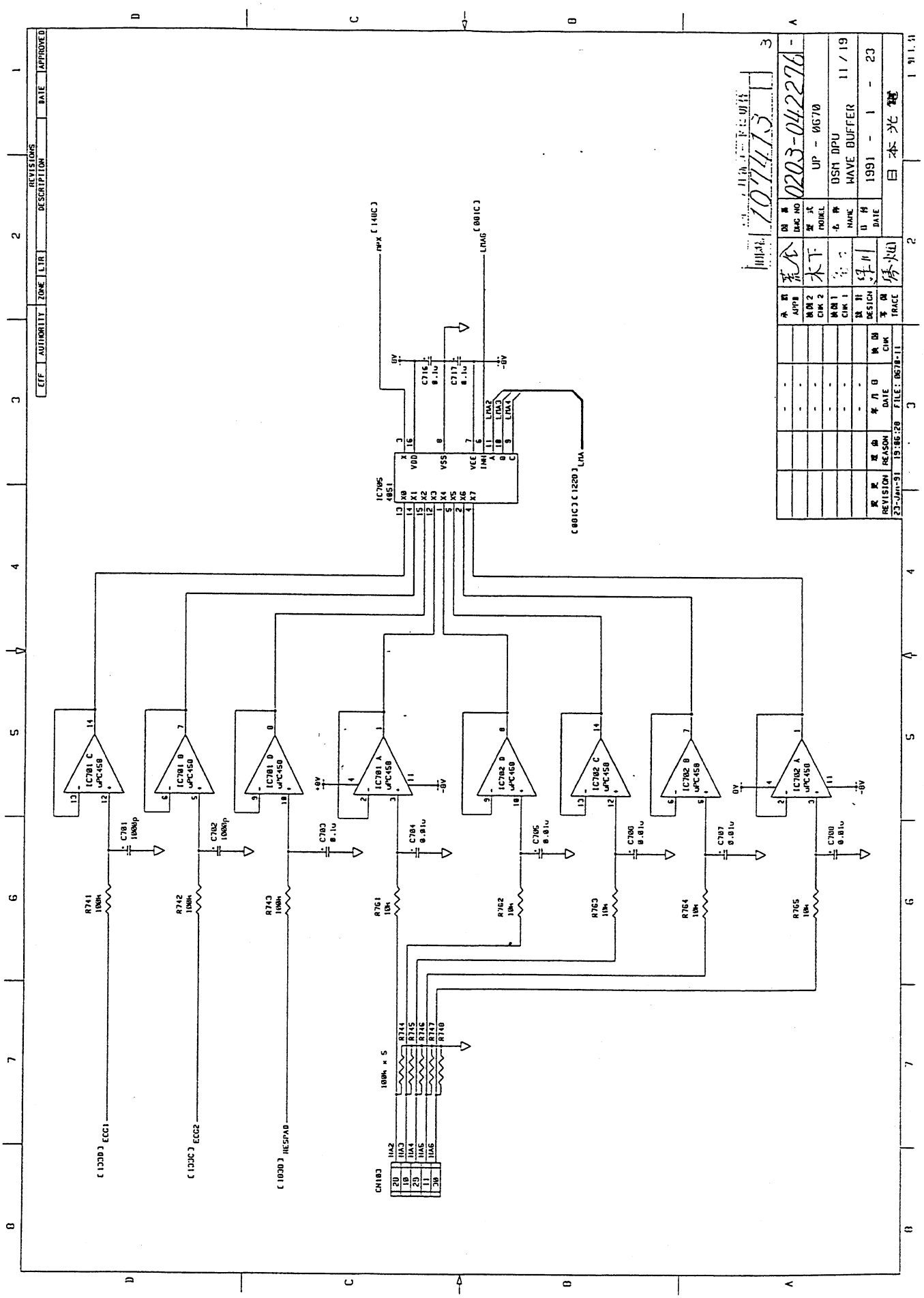
12. CIRCUIT DIAGRAM



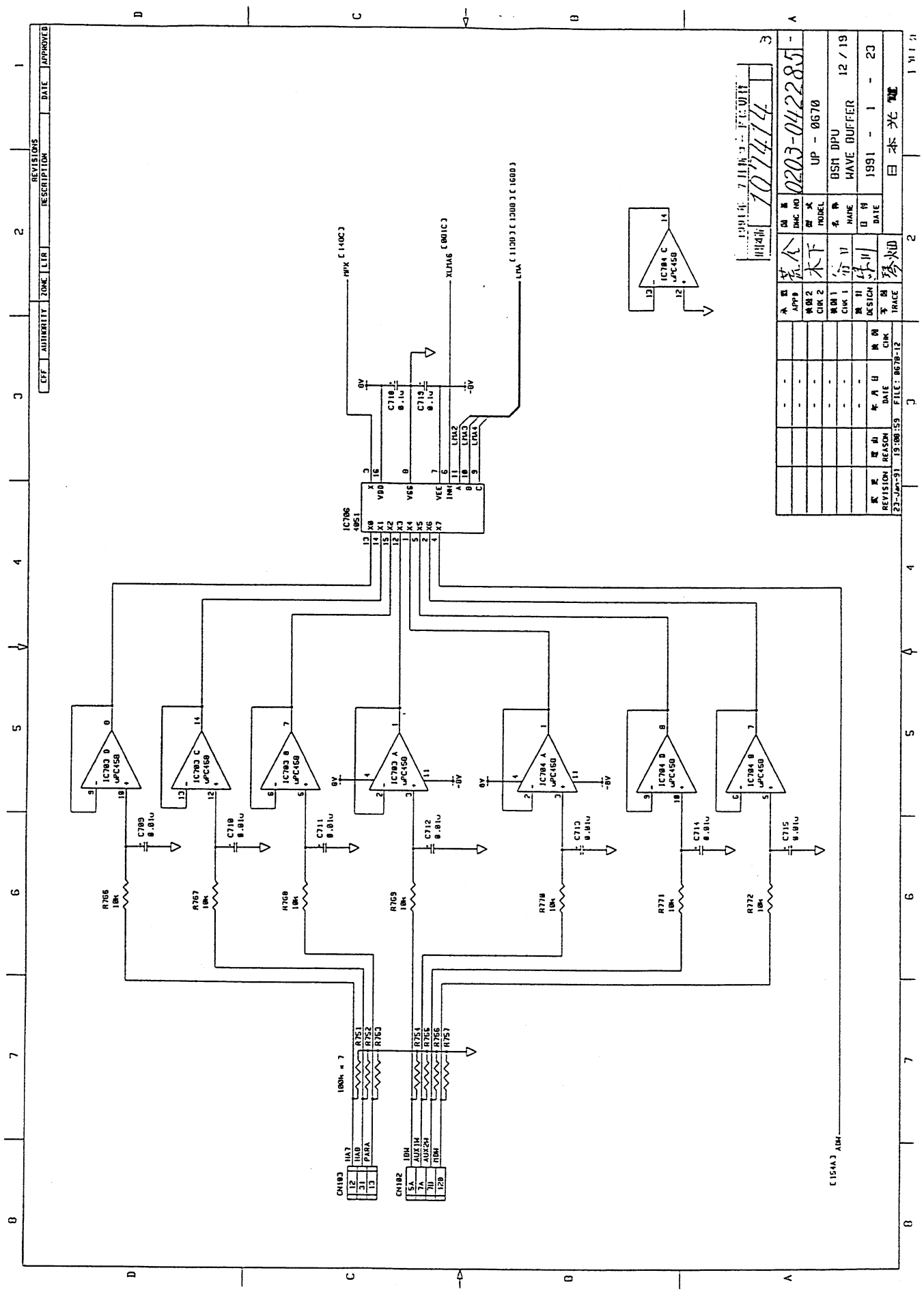


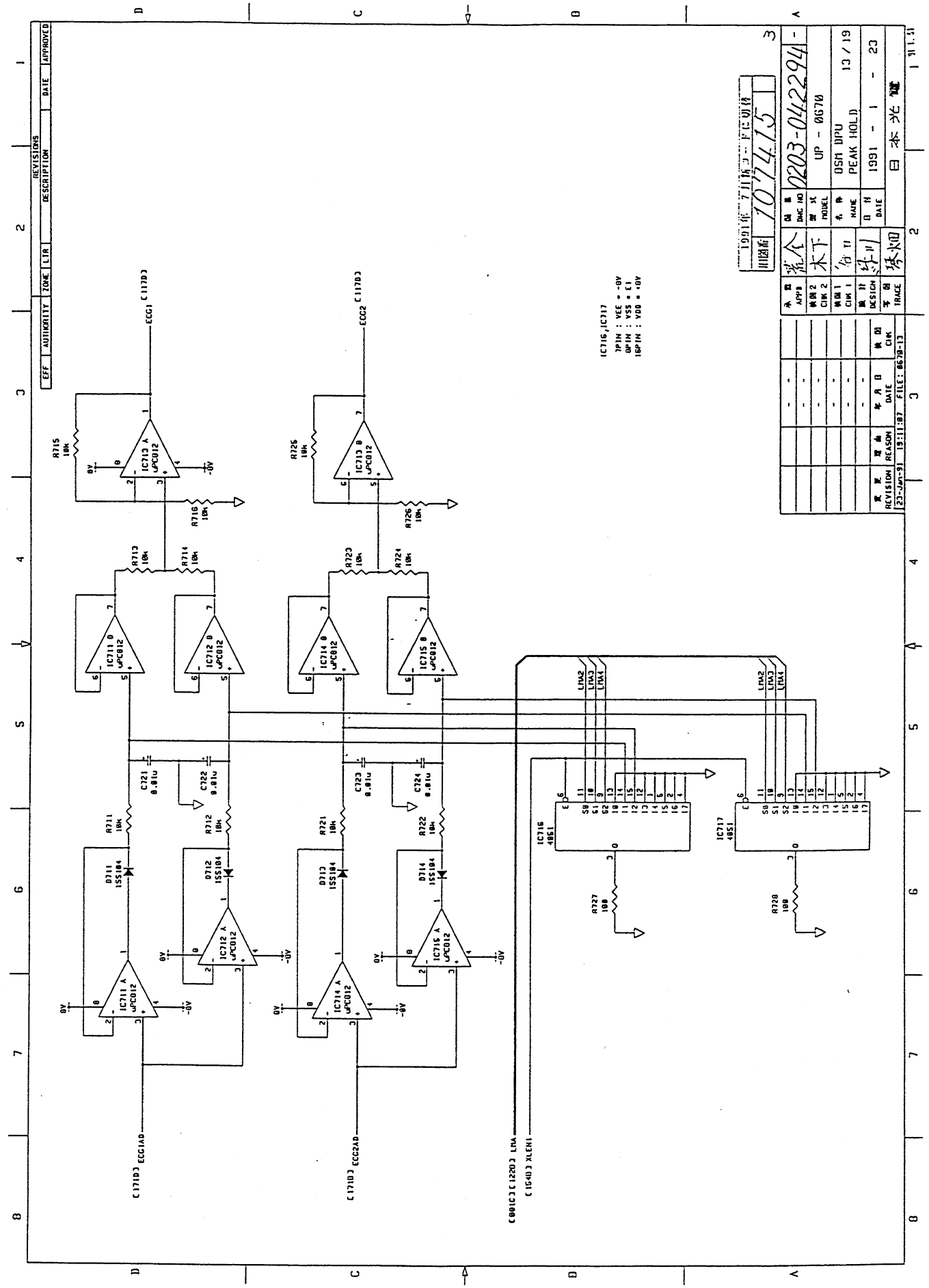
12. CIRCUIT DIAGRAM



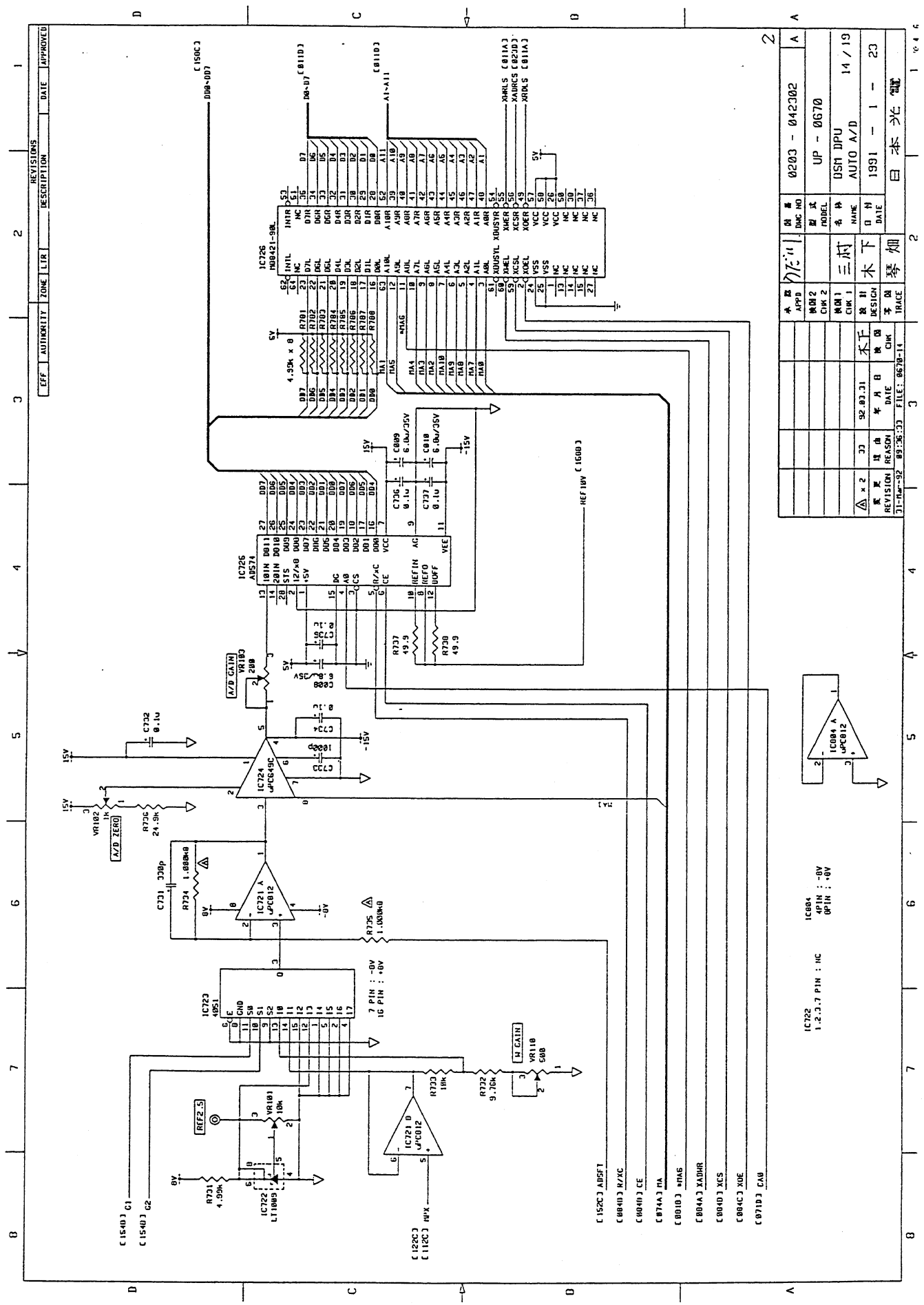


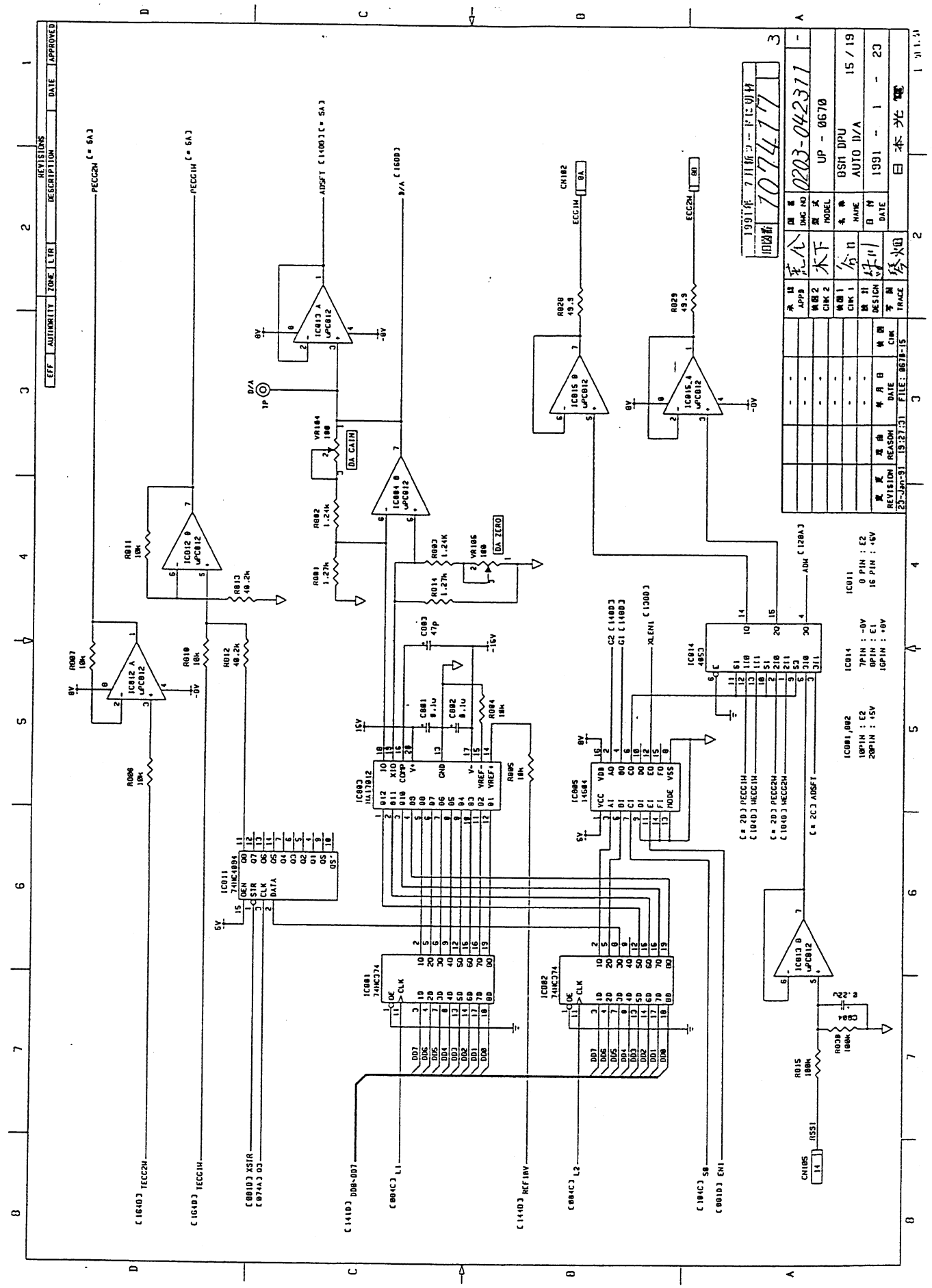
12. CIRCUIT DIAGRAM



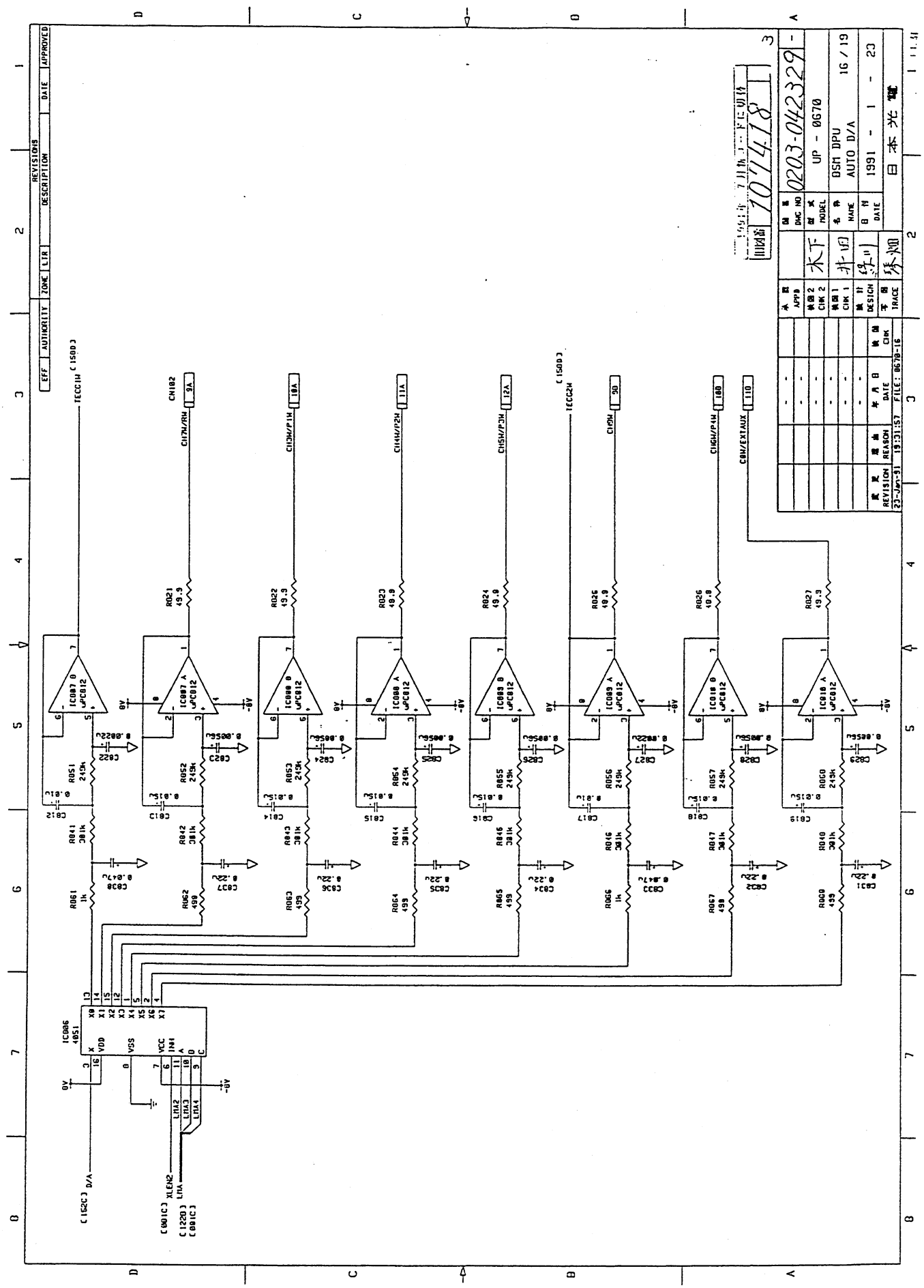


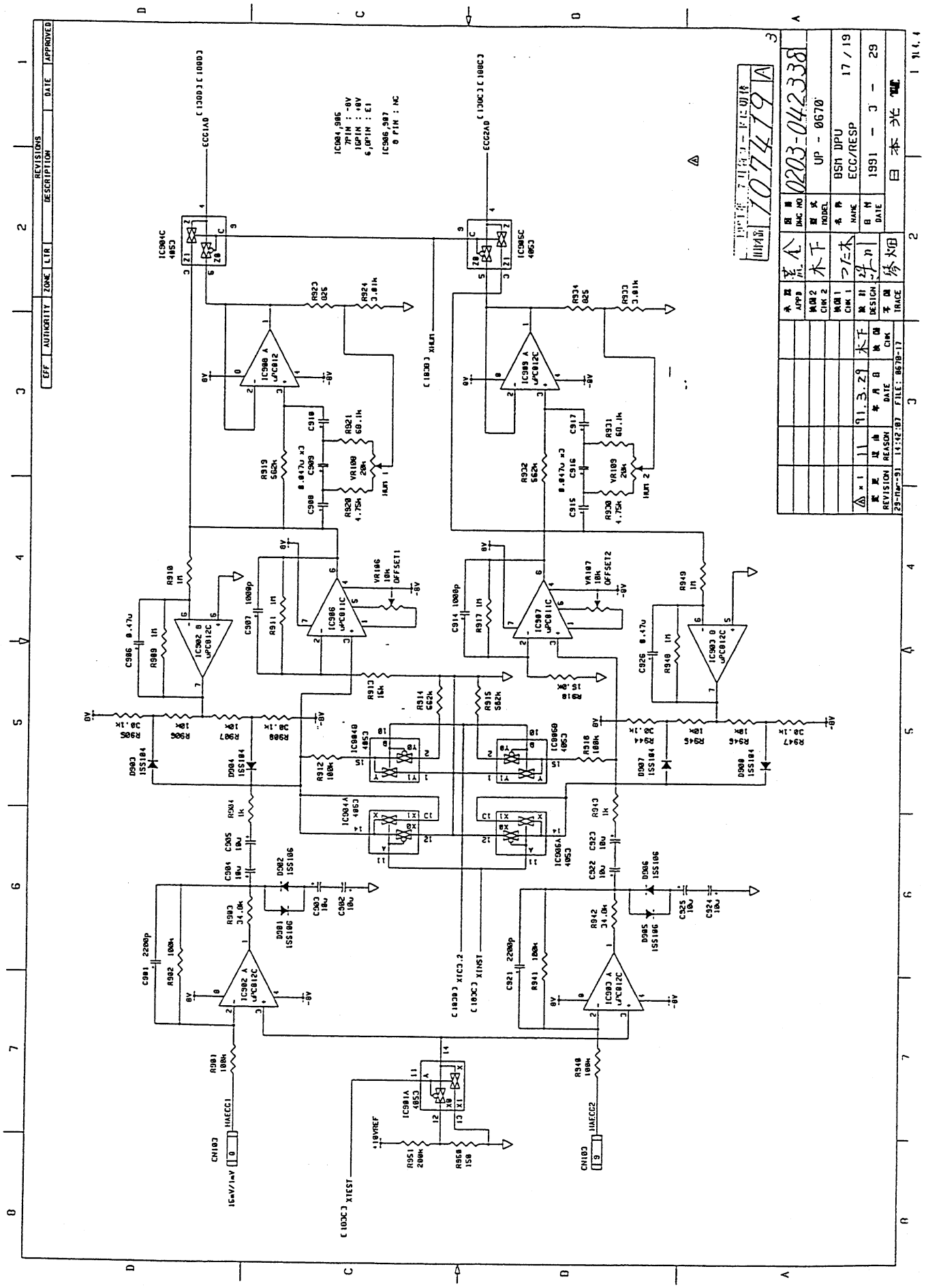
12. CIRCUIT DIAGRAM



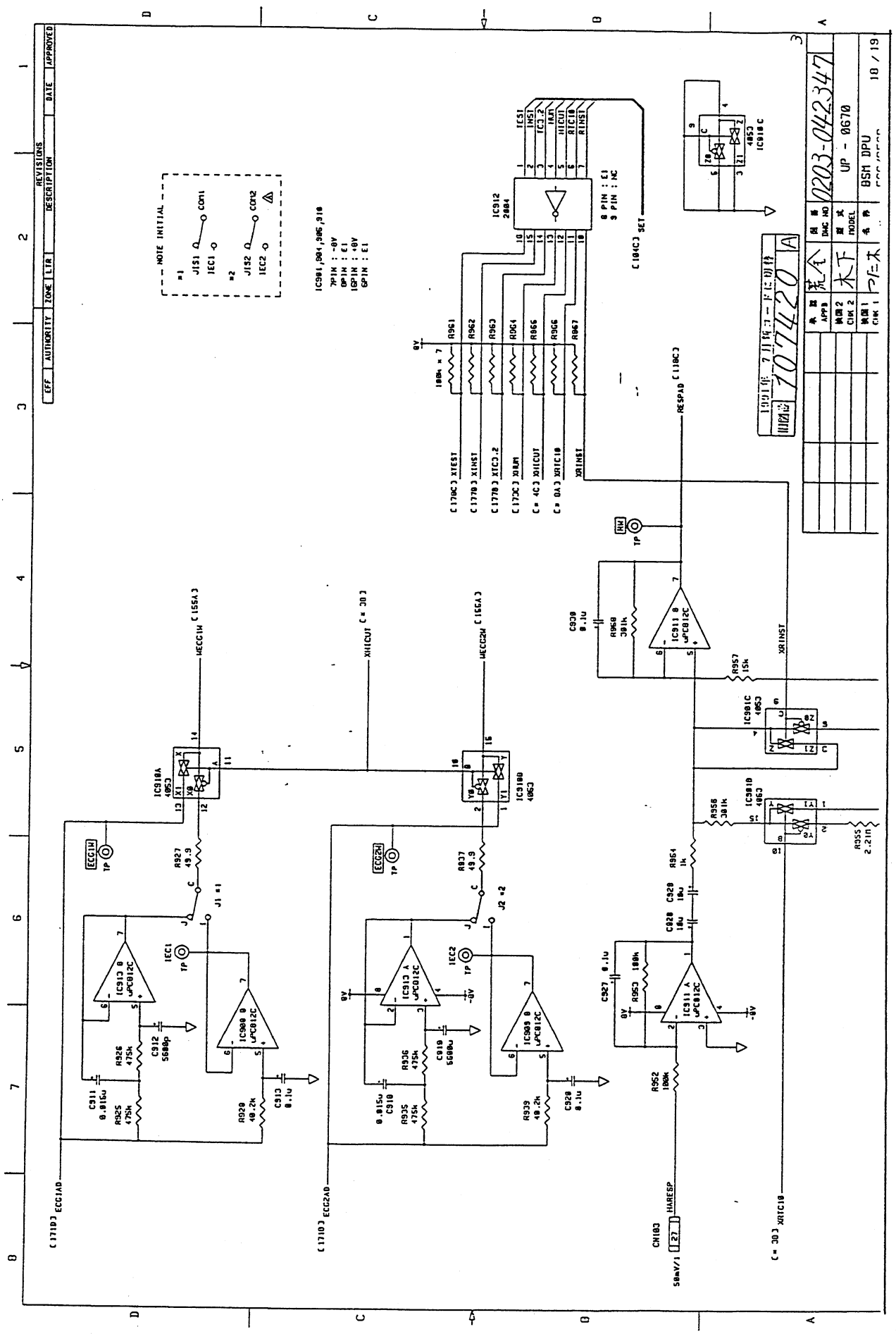


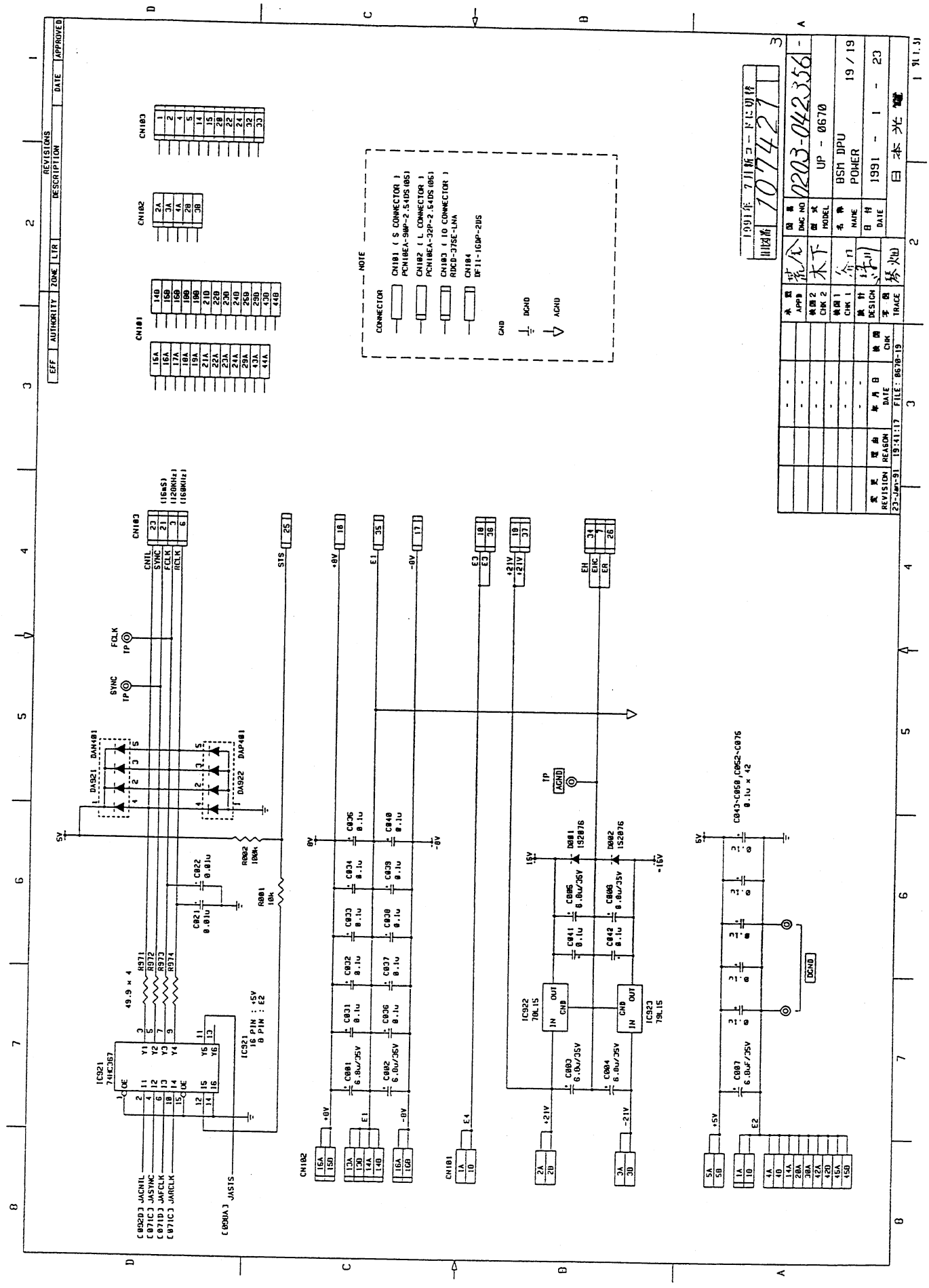
12. CIRCUIT DIAGRAM

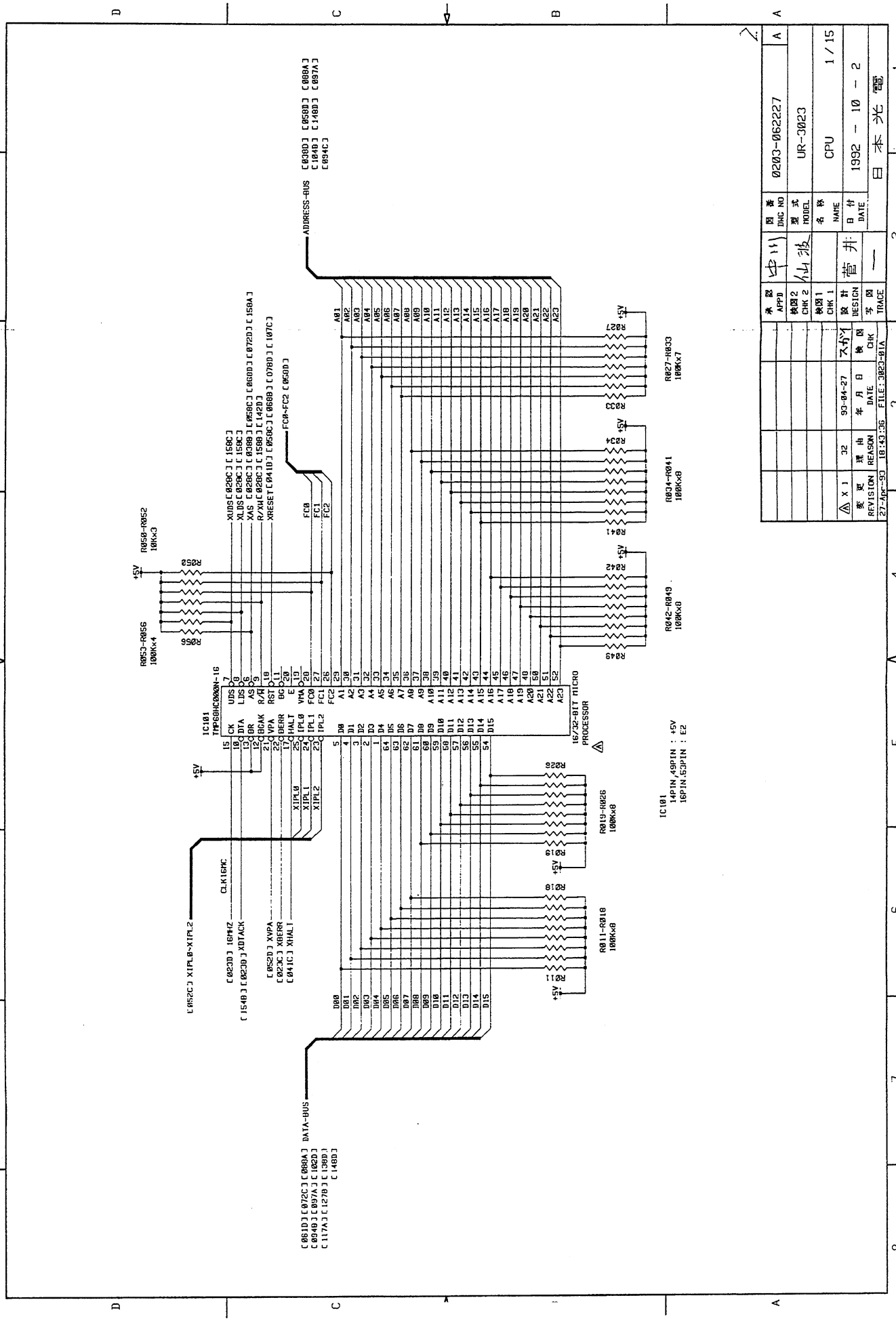


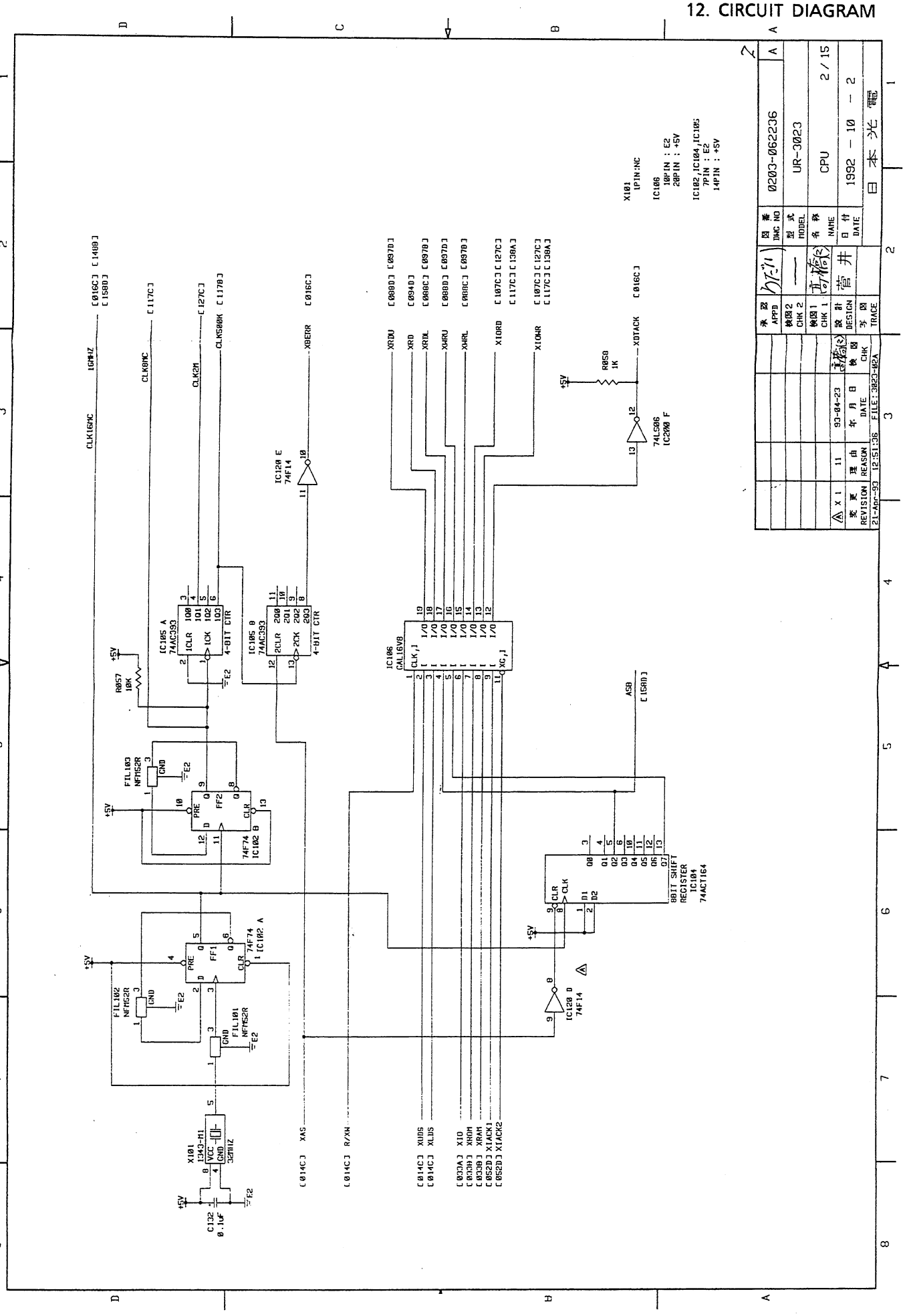


12. CIRCUIT DIAGRAM

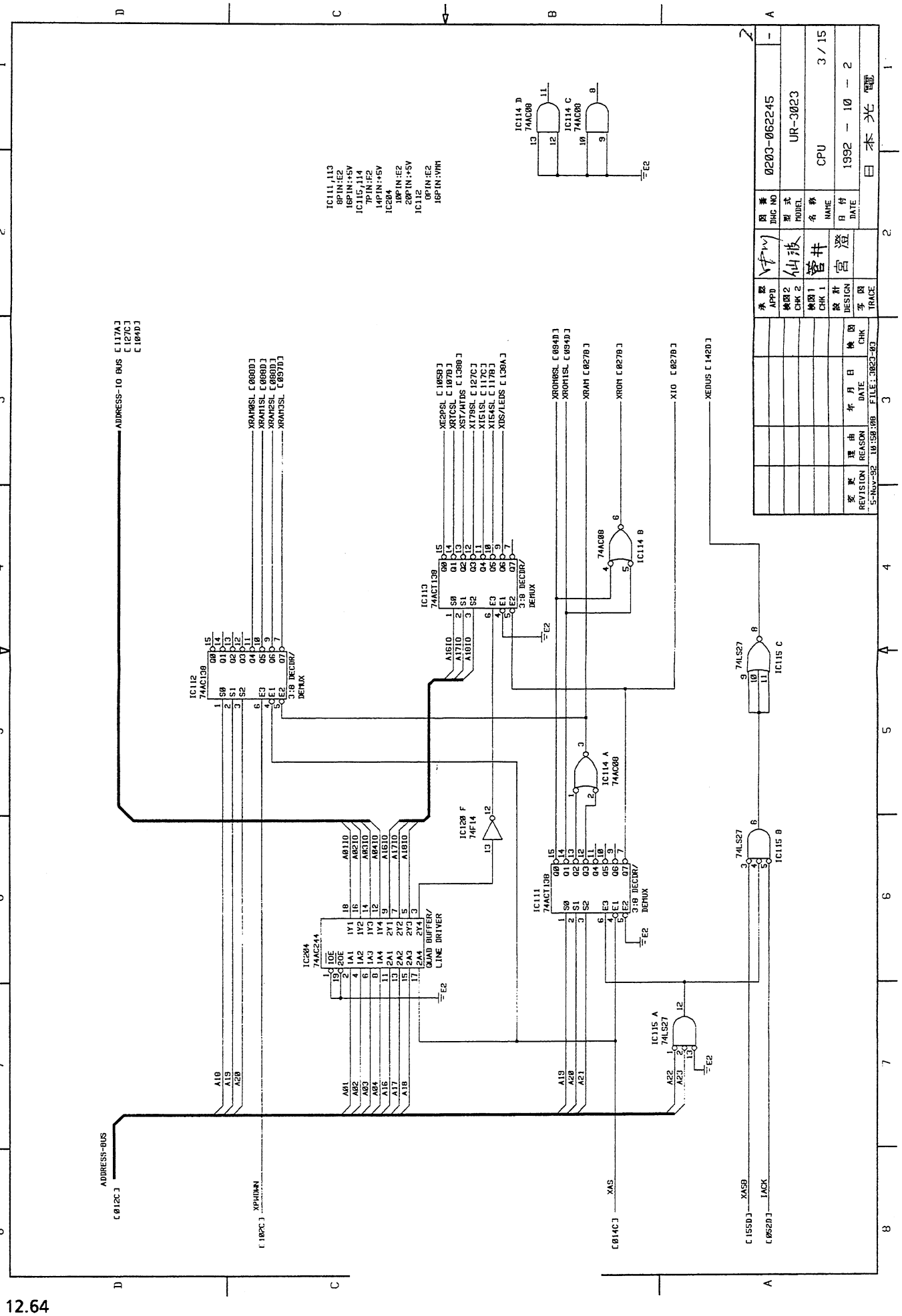


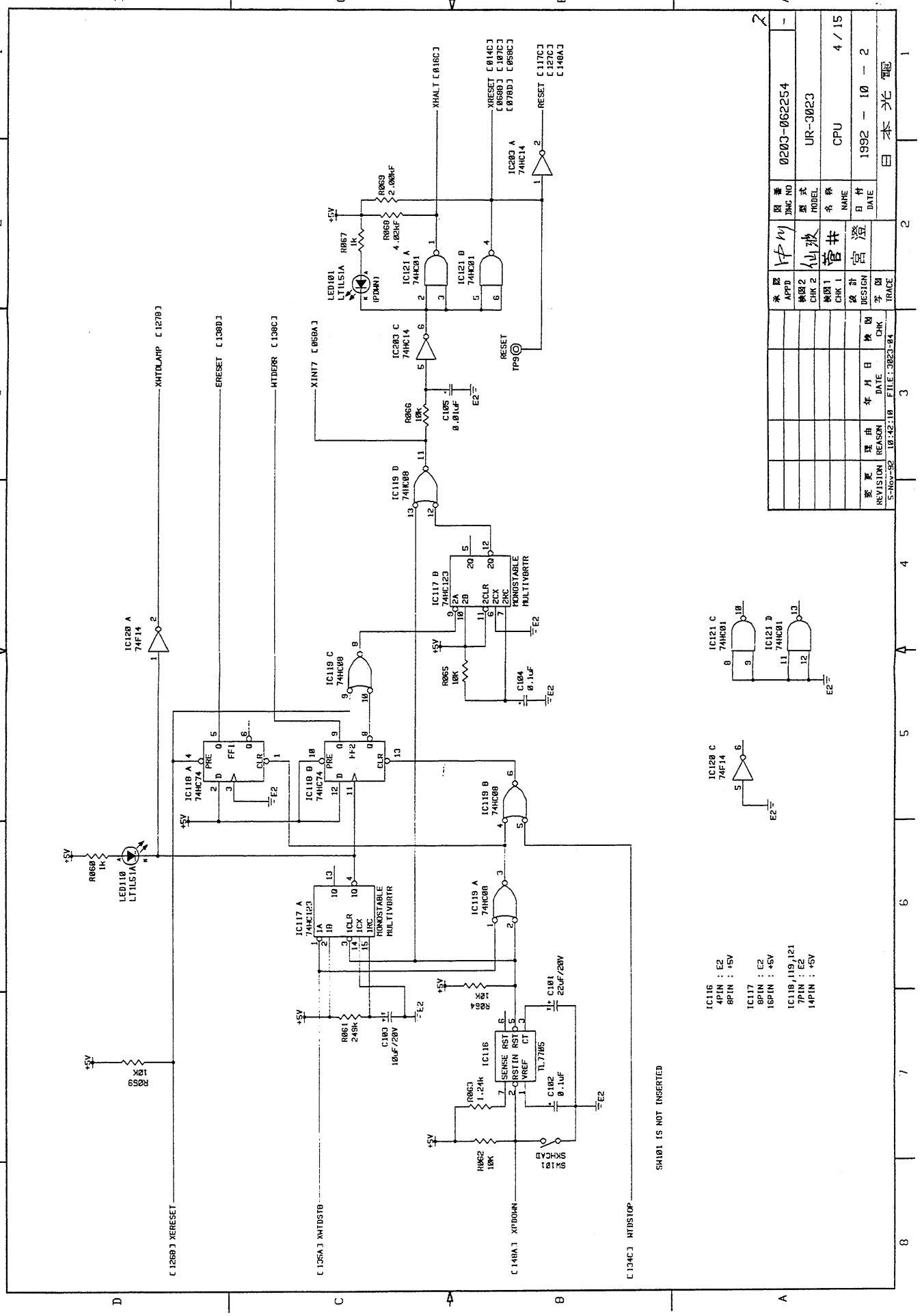



IC101
TMP68HC000N-16
16/32-BIT MICRO PROCESSOR
ADDRESS-BUS
DATA-BUS
R050-R052
100Kx3
R053-R056
100Kx4
R011-R018
100Kx8
R019-R026
100Kx8
R027-R033
100Kx7
R034-R041
100Kx8
R042-R049
100Kx8
IC101
14PIN,49PIN : +5V
16PIN,65PIN : E2
CLK16MC
16MHZ
XDTACK
XVPA
XBERR
XHALT
XIPL0-XIPL2
XIPL0
XIPL1
XIPL2
FC0-FC2
FC0
FC1
FC2
XUDS
XLDS
XAS
R/XW
XRESET
0203-062227
UR-3023
CPU
1992 - 10 - 2
日本光電
27-Apr-93
16:43:36
FILE: 3023-01A

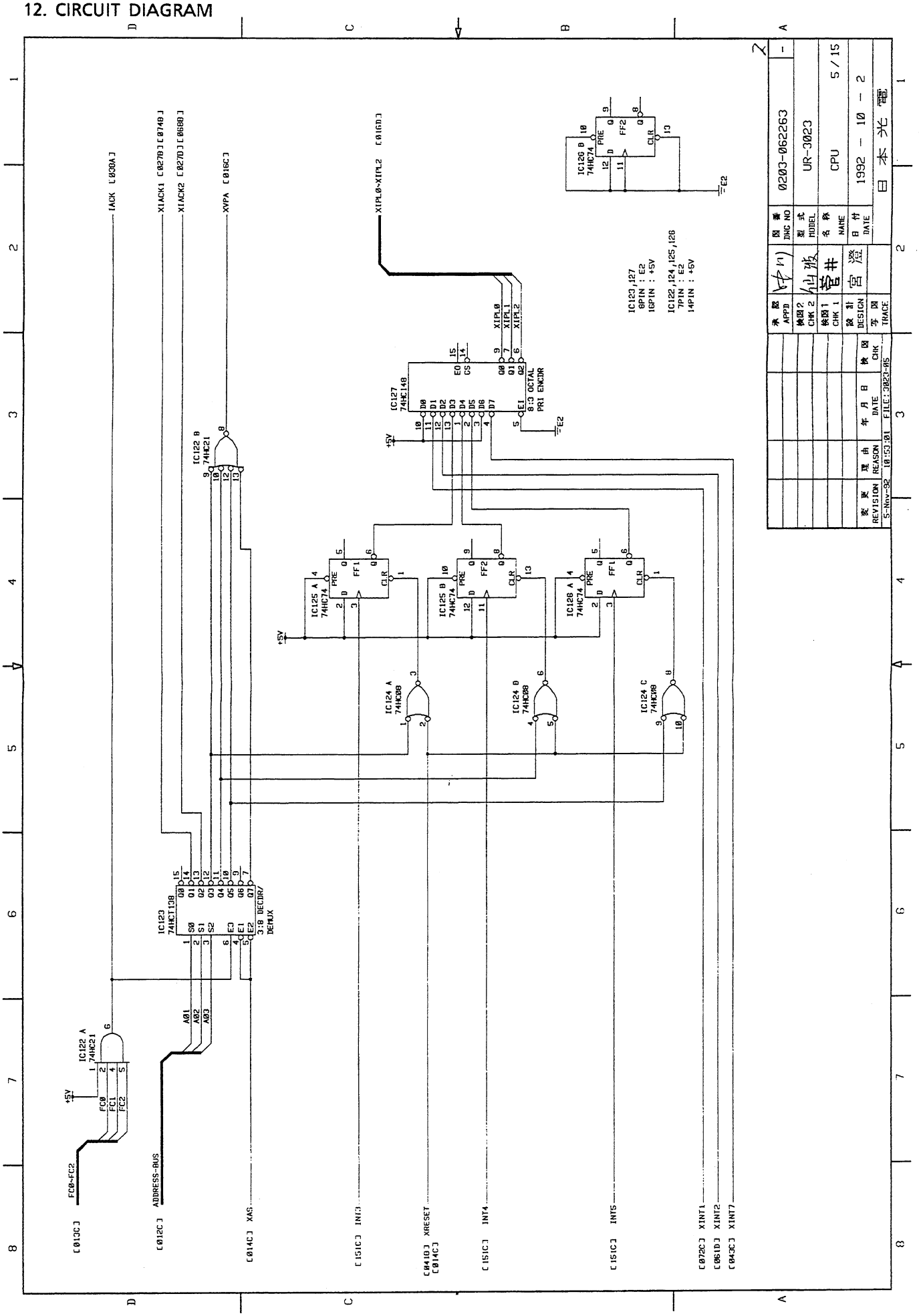

0203-062236
UR-3023
CPU
2 / 15
1992 - 10 - 2
日本光電
CLK16MC
16MHZ
CLK8MC
CLK2M
CLK500K
IC105 A 74AC393
IC105 B 74AC393
4-BIT CTR
IC120 E 74F14
IC102 A 74F74
IC102 B 74F74
FIL101 NFM52R
FIL102 NFM52R
FIL103 NFM52R
X101 13MHZ
C132 0.1uF
R057 10K
R058 1K
IC106 CAL16V8
IC107 74AC164
8BIT SHIFT REGISTER
74ACT164
74LS06 IC200 F
XRDU
XRD
XRWU
XWRL
X10RD
X10WR
XDTACK
XBERR
XA5
R/XW
XUDS
XLDS
X10
XROM
XRAM
X1ACK1
X1ACK2

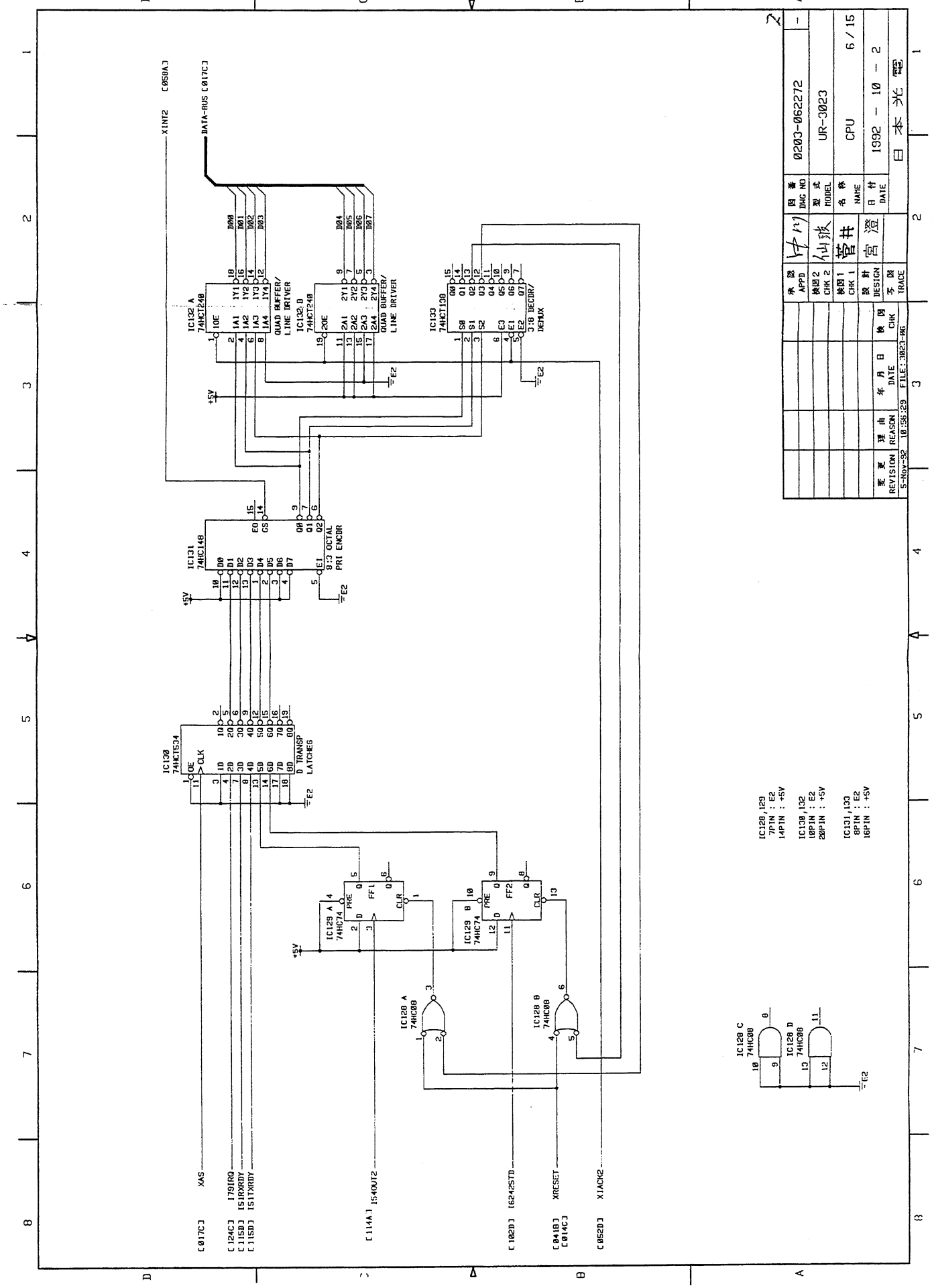
12. CIRCUIT DIAGRAM



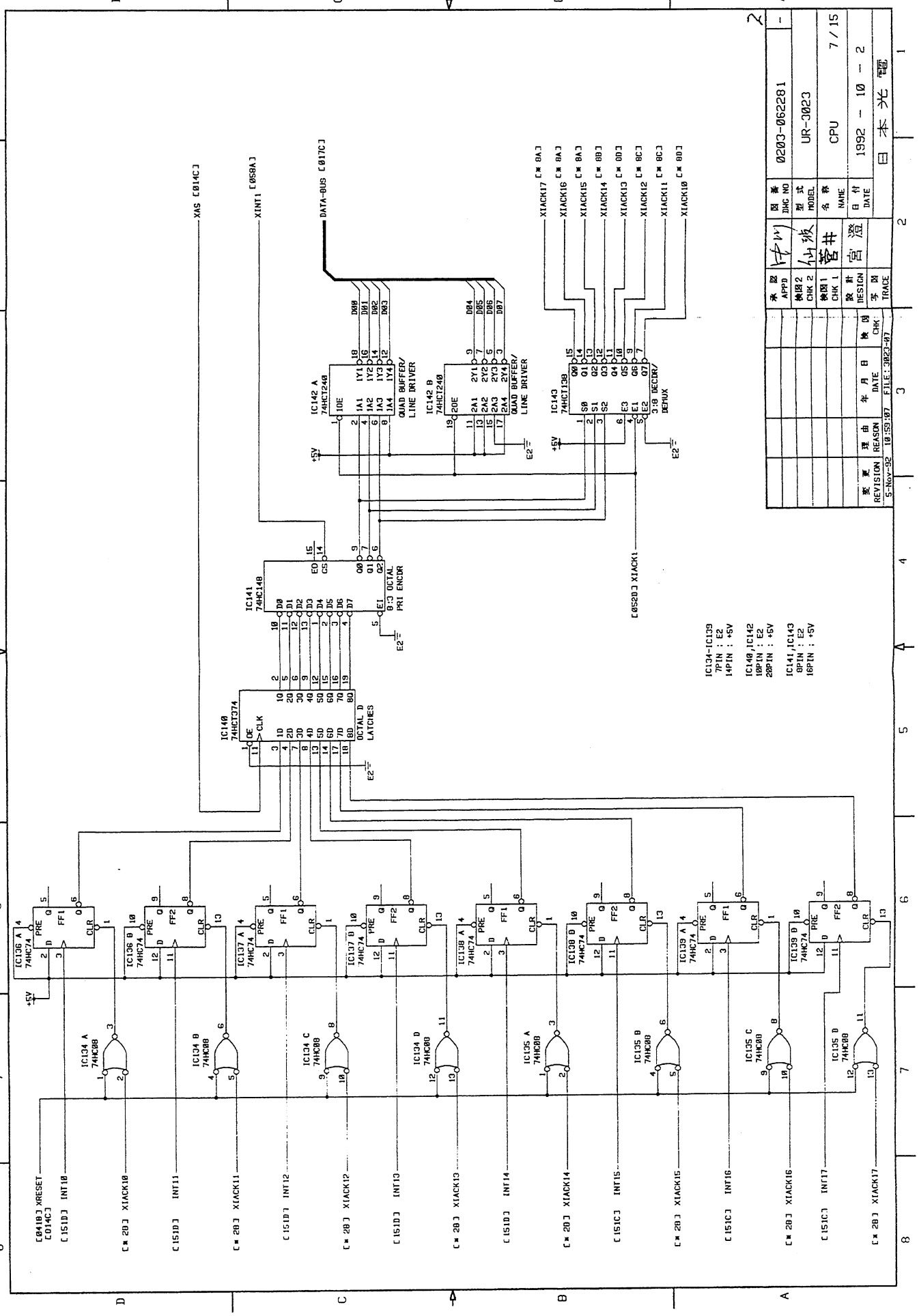

0203-062254
UR-3023
CPU
4 / 15
1992 - 10 - 2
日本光電
SH101 IS NOT INSERTED

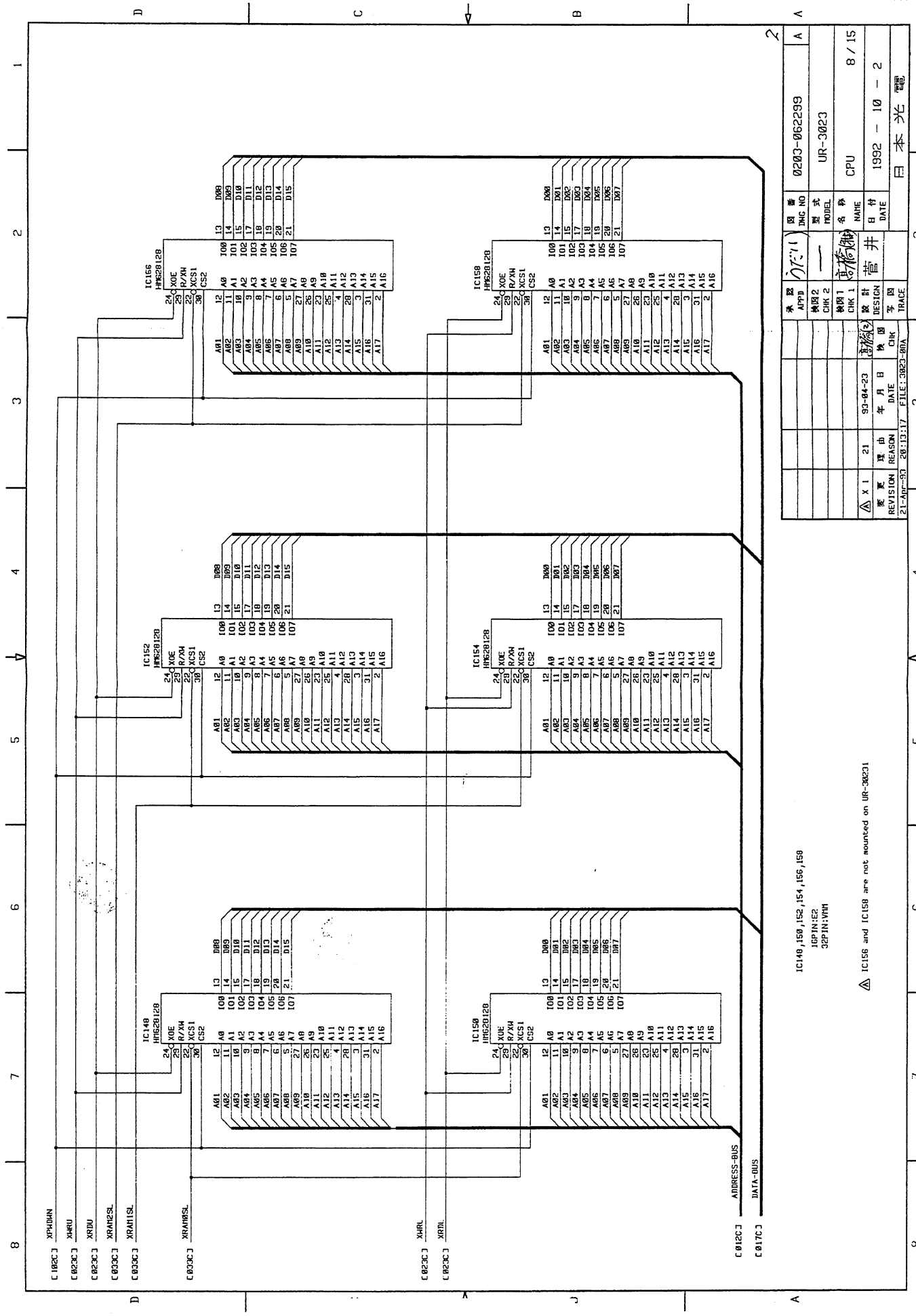
12. CIRCUIT DIAGRAM



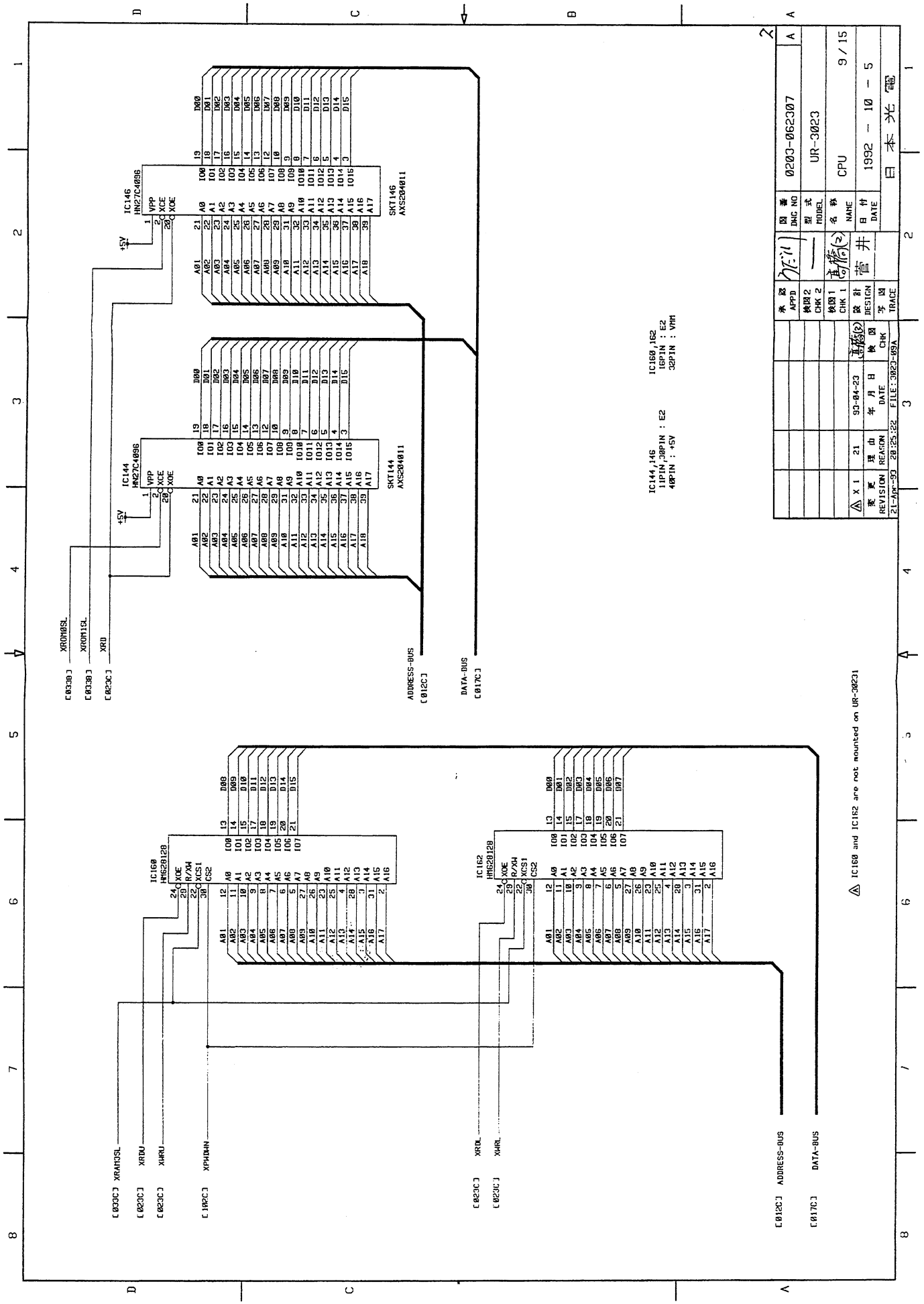

XINT2
DATA-BUS
IC132 A
74HCT240
QUAD BUFFER/
LINE DRIVER
IC132 B
74HCT240
QUAD BUFFER/
LINE DRIVER
IC133
74HCT138
3:8 DECODR/
DEMUX
IC131
74HC148
8:3 OCTAL
PRI ENCDR
IC130
74HC1534
D TRANSP
LATCHES
IC129 A
74HC74
FF1
IC129 B
74HC74
FF2
IC128 A
74HC08
IC128 B
74HC08
IC128 C
74HC08
IC128 D
74HC08
+5V
E2
XAS
I791RQ
IS1RXRDY
IS1TXRDY
IS40UT2
I6242STD
XRESET
X1ACK2
IC128,129
7PIN : E2
14PIN : +5V
IC130,132
10PIN : E2
20PIN : +5V
IC131,133
8PIN : E2
16PIN : +5V
REVISION
REASON
DATE
CHK
APPD
CHK 2
CHK 1
DESIGN
TRACE
DWG NO
0203-062272
MODEL
UR-3023
NAME
CPU
DATE
1992 - 10 - 2
6 / 15
日本光電

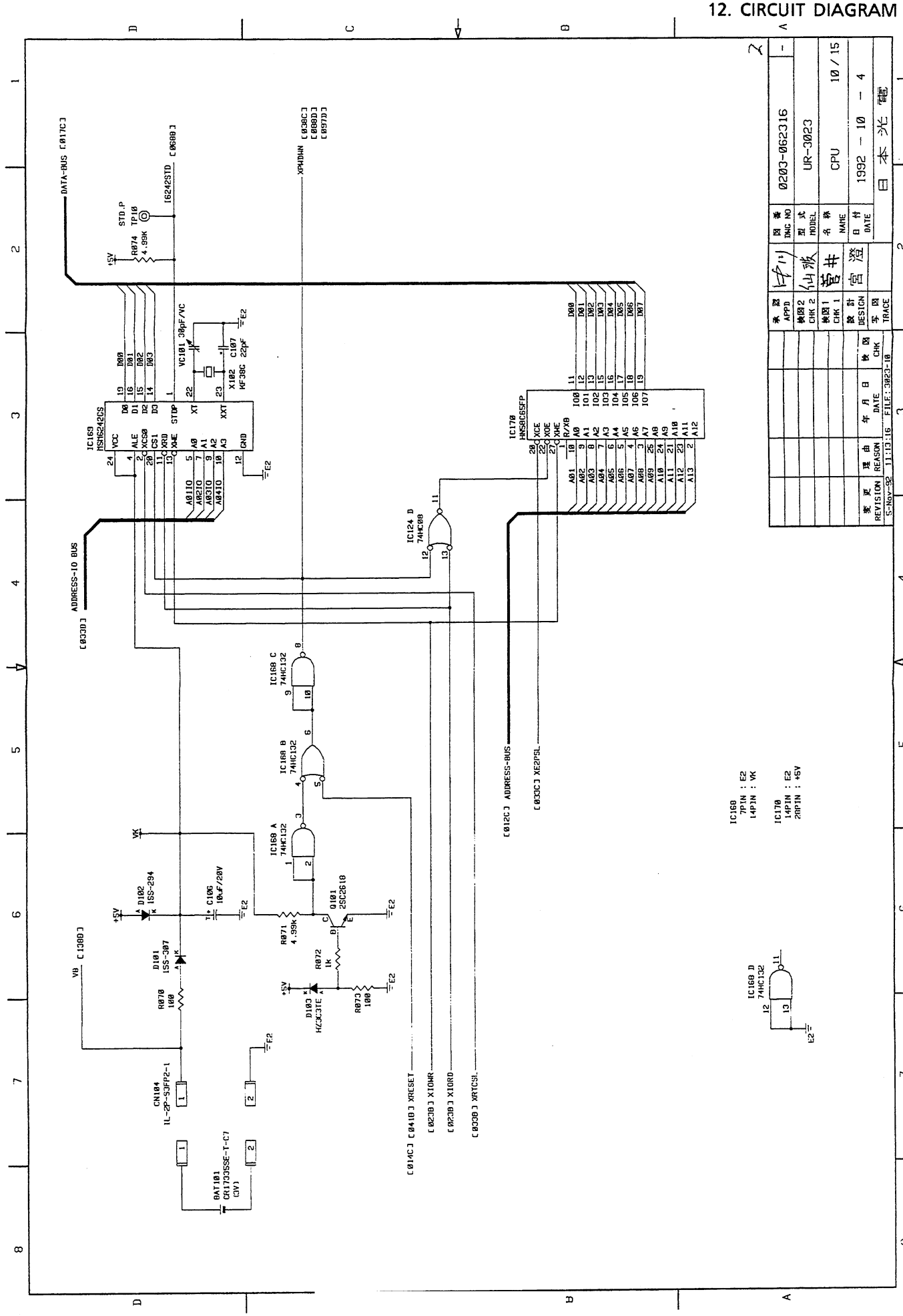
12. CIRCUIT DIAGRAM



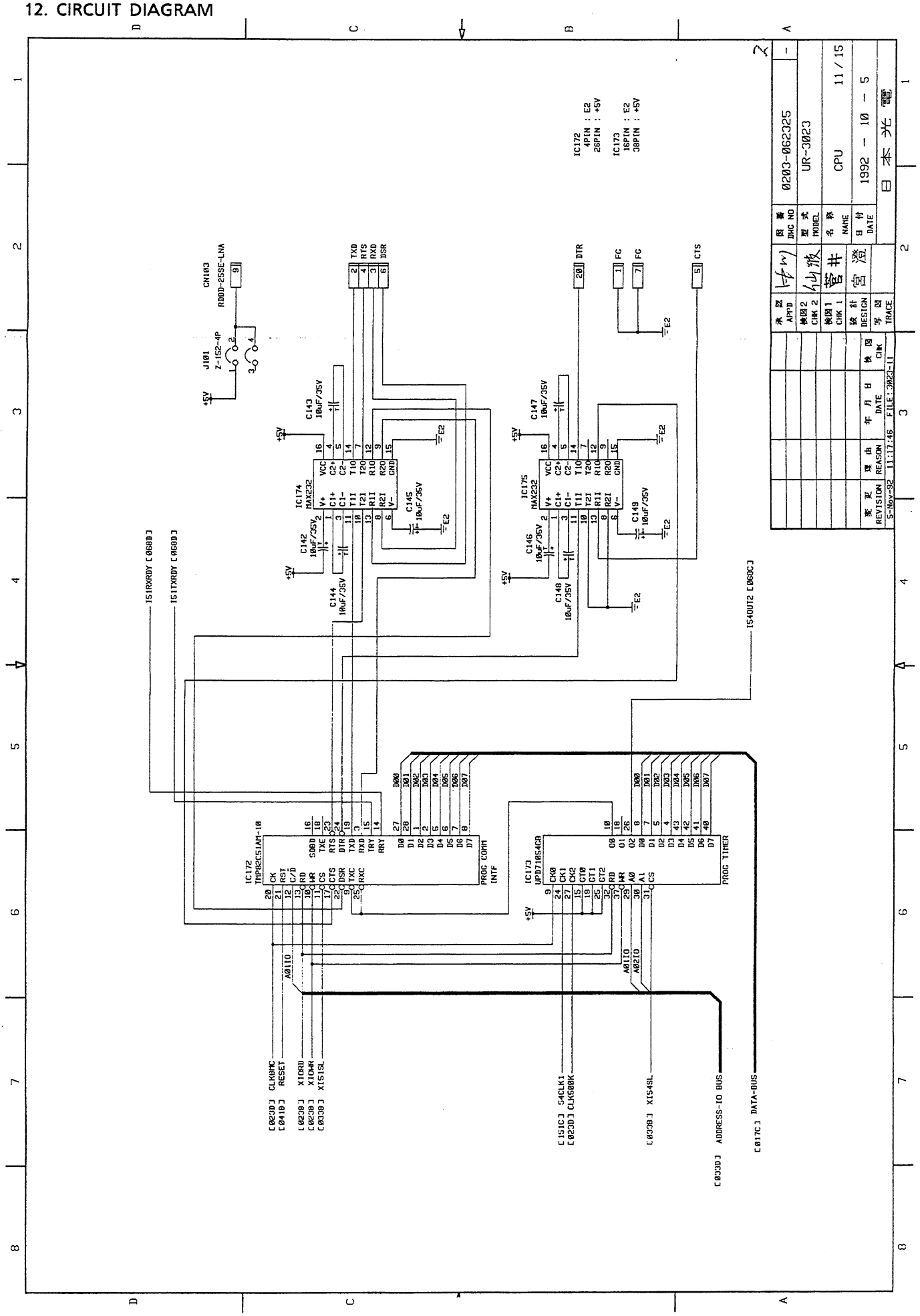

IC140,150,152,154,156,158
16PIN:E2
32PIN:WM
IC156 and IC158 are not mounted on UR-3023I
ADDRESS-BUS
DATA-BUS
XPWDWN
XWRU
XRDU
XRAM2SL
XRAM1SL
XRAM0SL
XWRL
XRDL
IC140 HM628128
IC150 HM628128
IC152 HM628128
IC154 HM628128
IC156 HM628128
IC158 HM628128
IC166 HM628128
REVISION
REASON
DATE
CHK
DESIGN
TRACE
APPD
CHK 2
CHK 1
IMG NO
MODEL
NAME
DATE
0203-062299
UR-3023
CPU
1992 - 10 - 2
日本光電
8 / 15

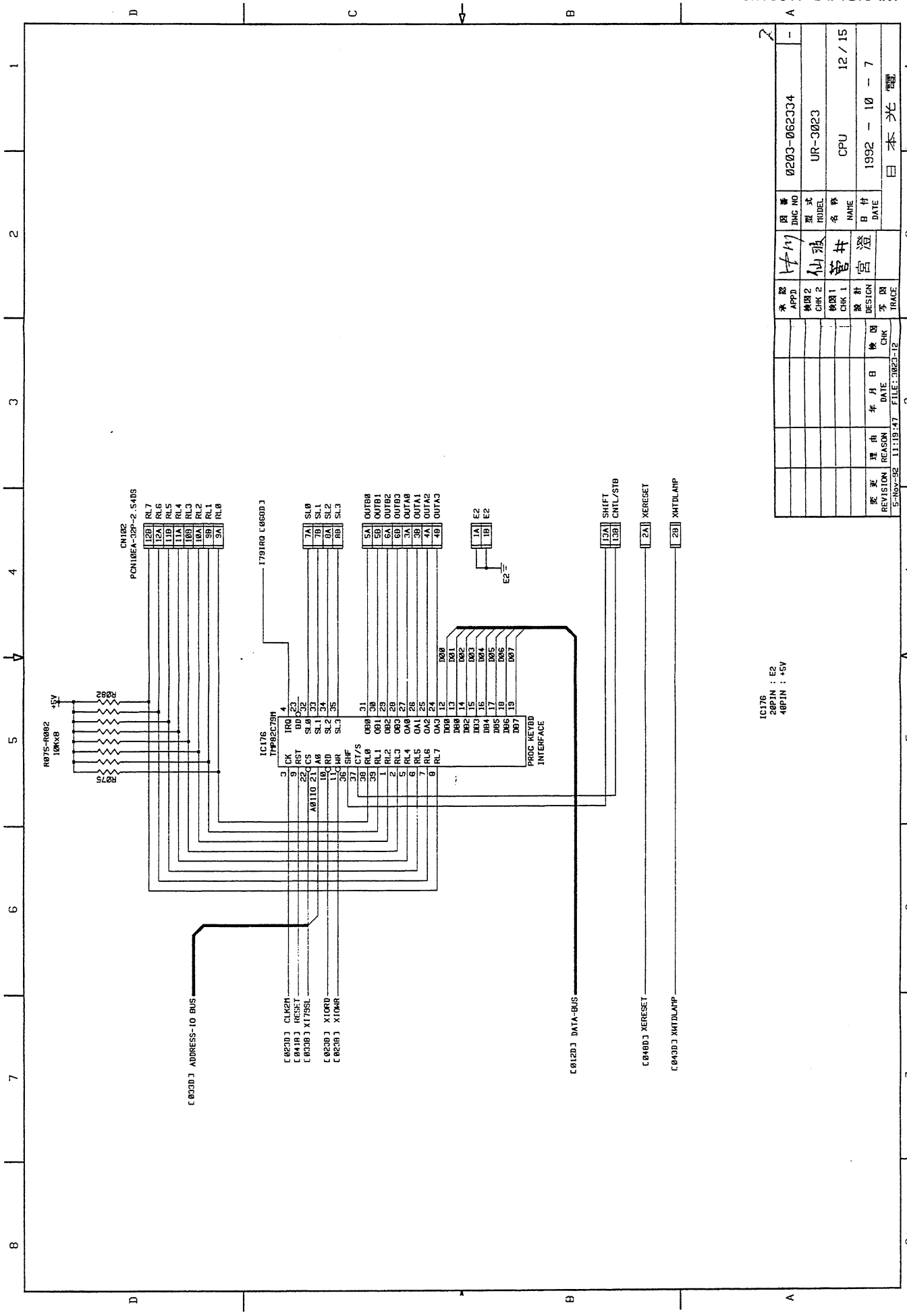
12. CIRCUIT DIAGRAM



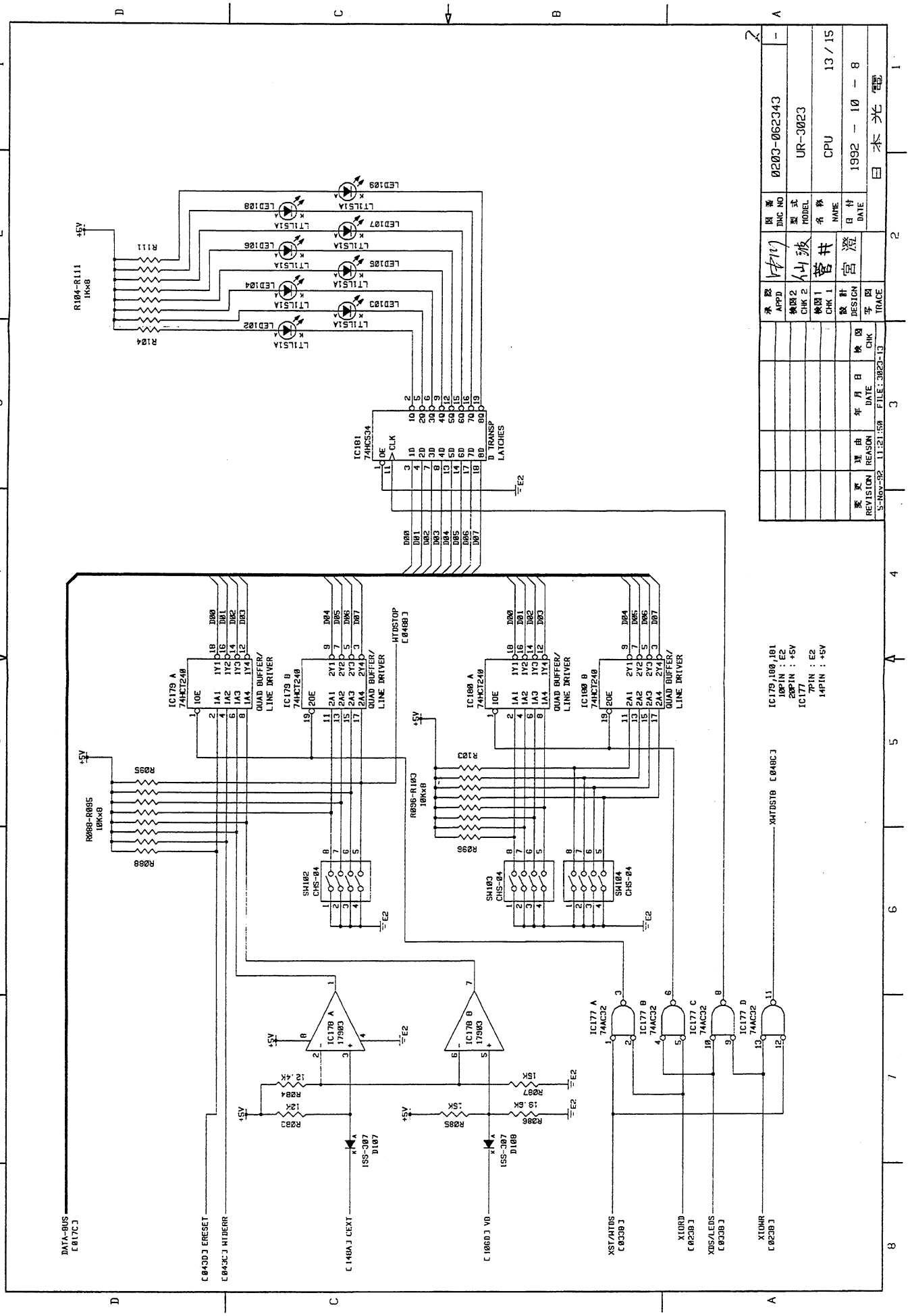

DATA-BUS
ADDRESS-IO BUS
IC169 MSM6242GS
IC170 HN58C65FP
IC124 D 74HC08
IC168 A 74HC132
IC168 B 74HC132
IC168 C 74HC132
IC168 D 74HC132
D101 1SS-307
D102 1SS-294
D103 HZC3.3TE
Q101 2SC2618
R070 100
R071 4.99K
R072 1K
R073 100
R074 4.99K
C106 10uF/20V
C107 22pF
VC101 30pF/VC
X102 MF38G
BAT101 CR1733SSE-T-C7 (3V)
CN104 IL-2P-S3FP2-1
TP10
+5V
E2
VB
VK
XRESET
XIOWR
XIORD
XRTCSL
XEXPSL
ADDRESS-BUS
XPWDWN
I6242STD
STD.P
IC168 7PIN : E2
14PIN : VK
IC170 14PIN : E2
28PIN : +5V
0203-062316
UR-3023
CPU
10 / 15
1992 - 10 - 4
日本光電

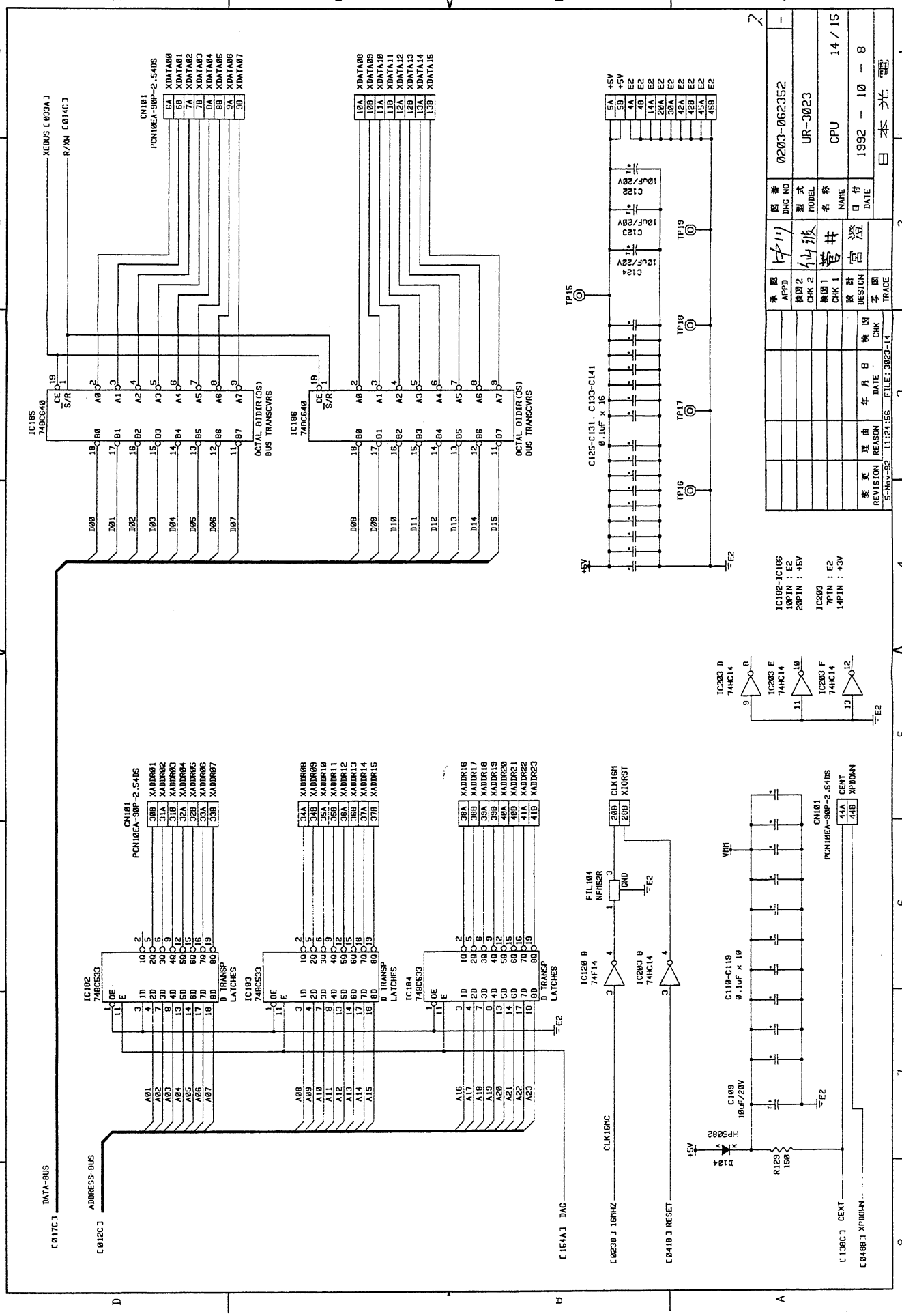
12. CIRCUIT DIAGRAM



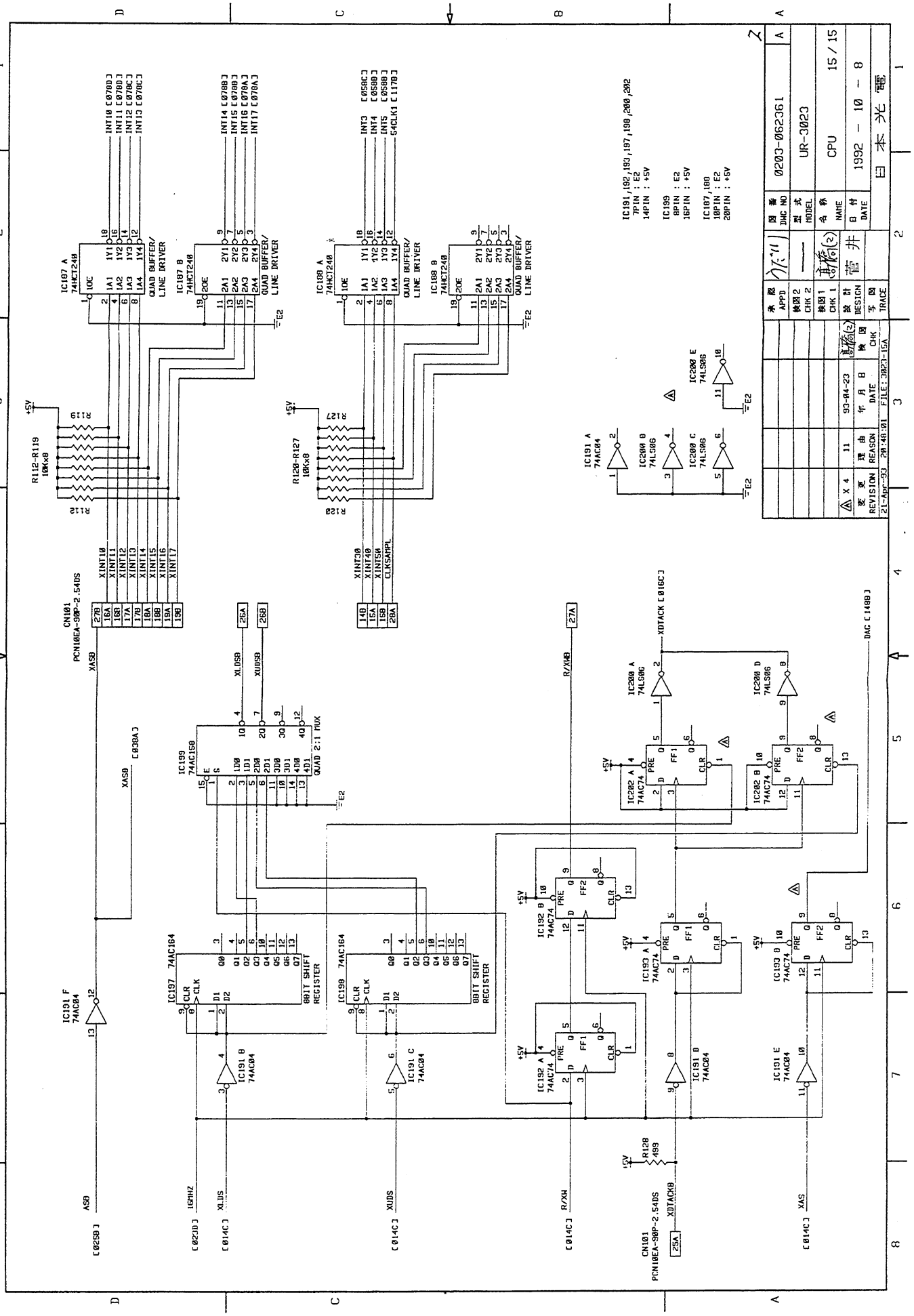

CN102
PCN10EA-32P-2.54DS
RL7
RL6
RL5
RL4
RL3
RL2
RL1
RL0
R075-R082
10Kx8
+5V
IC176
TMP82C79M
PROG KEYBD
INTERFACE
SL0
SL1
SL2
SL3
OUTB0
OUTB1
OUTB2
OUTB3
OUTA0
OUTA1
OUTA2
OUTA3
E2
SHIFT
CNTL/STB
XERESET
XHTDLAMP
ADDRESS-IO BUS
DATA-BUS
CLK2M
RESET
X179SL
X10RD
X10WR
IC176
20PIN : E2
40PIN : +5V
REVISION
REASON
DATE
CHK
APPD
DESIGN
TRACE
DWG NO
Ø203-062334
MODEL
UR-3023
NAME
CPU
12 / 15
DATE
1992 - 10 - 7
5-Nov-92 11:19:47 FILE:3023-12
日本光電

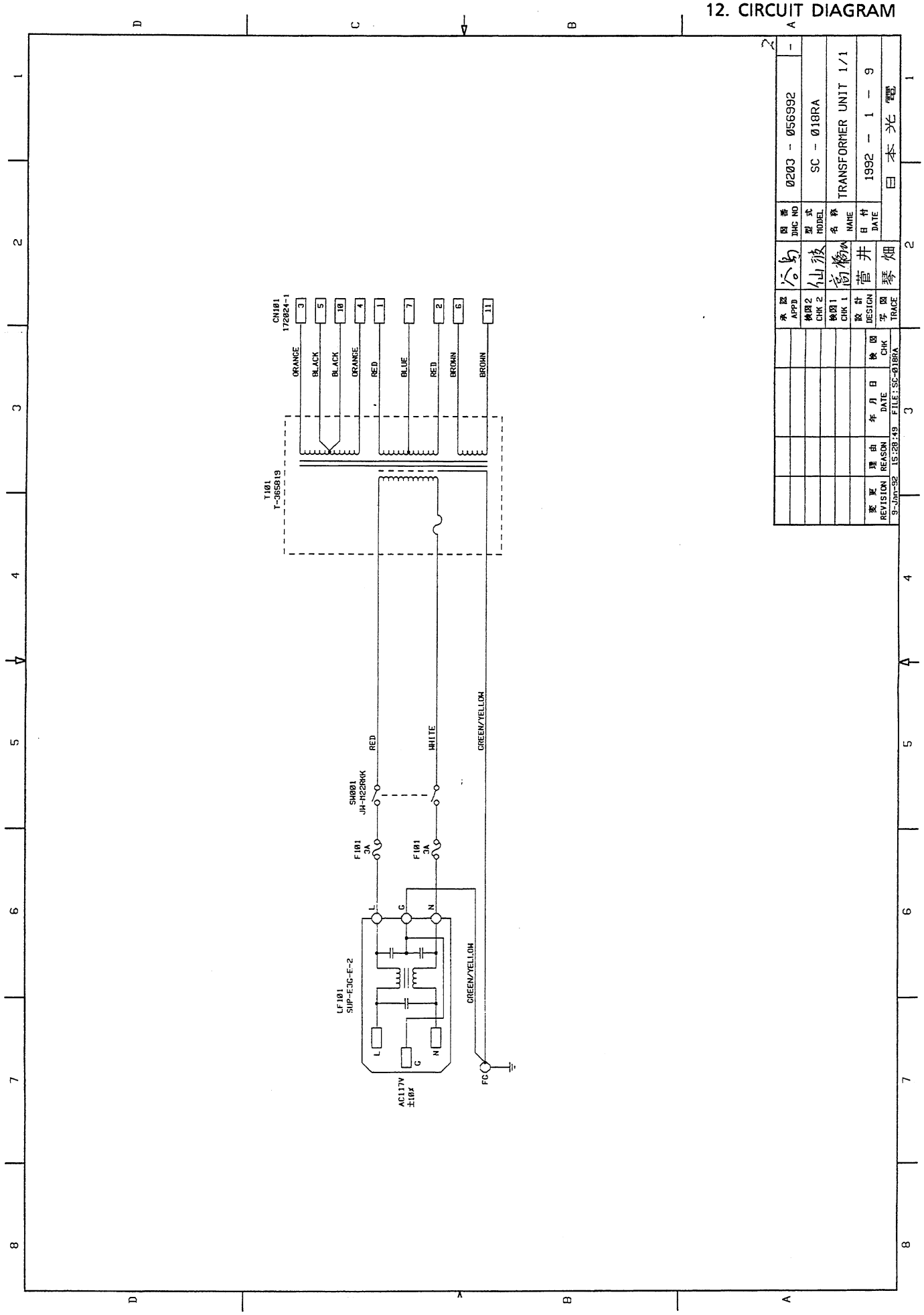
12. CIRCUIT DIAGRAM



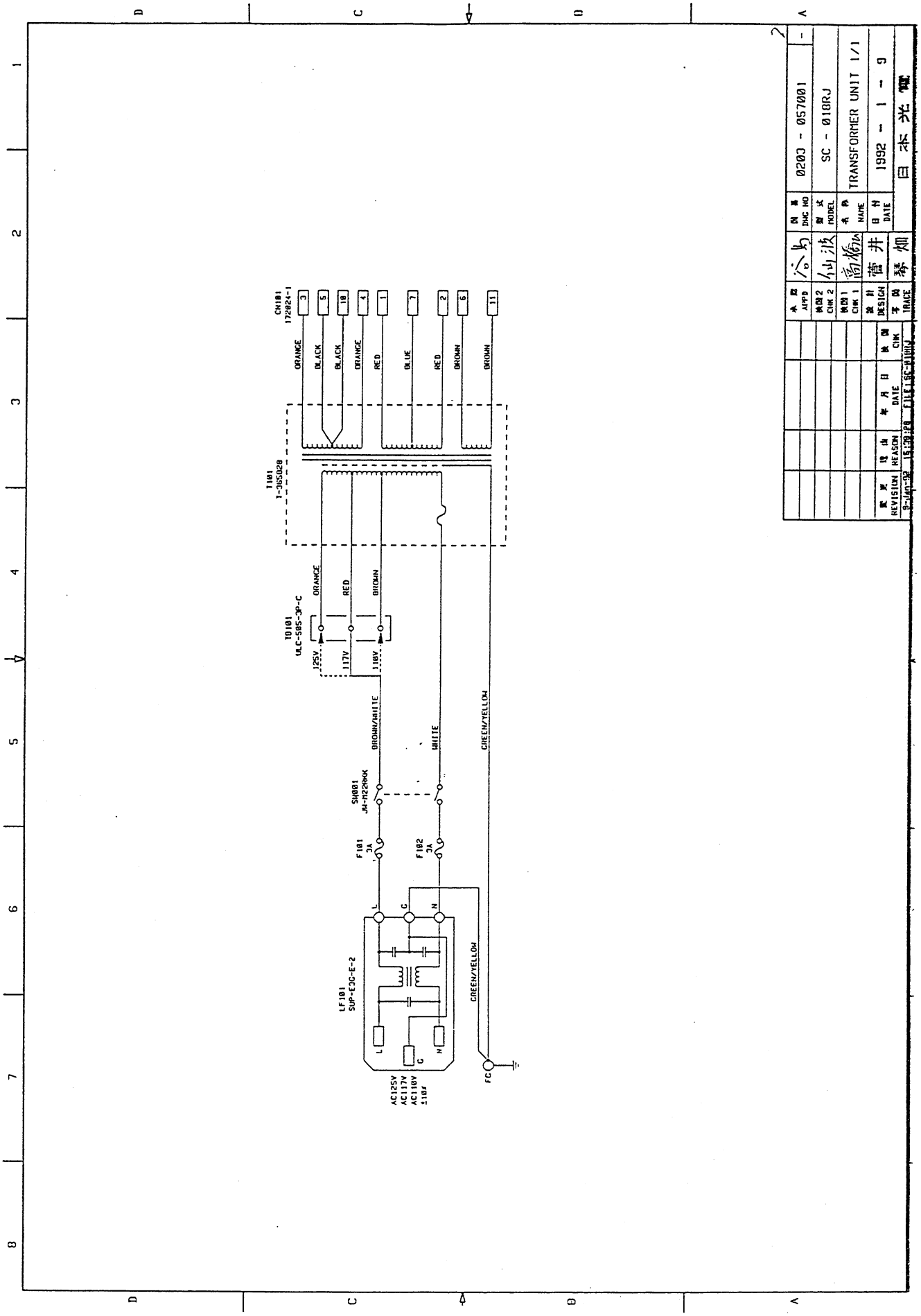

0203-062352
UR-3023
CPU
14 / 15
1992 - 10 - 8
日本光電
IC185 74HC640
IC186 74HC640
OCTAL BIDIR(3S) BUS TRANSCVRS
CN101 PCN10EA-90P-2.54DS
XDATA00
XDATA01
XDATA02
XDATA03
XDATA04
XDATA05
XDATA06
XDATA07
XDATA08
XDATA09
XDATA10
XDATA11
XDATA12
XDATA13
XDATA14
XDATA15
XEBUS [033A]
R/XW [014C]
C125-C131, C133-C141 0.1uF x 16
10uF/20V
TP15
TP16
TP17
TP18
TP19
IC102 74HC533
IC103 74HC533
IC104 74HC533
D TRANSP LATCHES
XADDR01
XADDR02
XADDR03
XADDR04
XADDR05
XADDR06
XADDR07
XADDR08
XADDR09
XADDR10
XADDR11
XADDR12
XADDR13
XADDR14
XADDR15
XADDR16
XADDR17
XADDR18
XADDR19
XADDR20
XADDR21
XADDR22
XADDR23
DATA-BUS
ADDRESS-BUS
[017C]
[012C]
[154A] DAC
[023D] 16MHZ
[041B] RESET
[138C] CEXT
[048B] XPDOWN
CLK16MC
CLK16M
X10RST
FIL104 NFM52R
IC120 B 74F14
IC203 B 74HC14
IC203 D 74HC14
IC203 E 74HC14
IC203 F 74HC14
C110-C119 0.1uF x 10
C109 10uF/20V
D124 1PS082
R129 150
VBH
CENT
XPDOWN
IC102-IC106 10PIN : E2 20PIN : +5V
IC203 7PIN : E2 14PIN : +3V
DESIGN
DRAWN
CHK
APP'D
CHK 2
CHK 1
REVISION
REASON
DATE
TRACE
S-Nov-92 11:24:56 FILE: 3023-14

12. CIRCUIT DIAGRAM

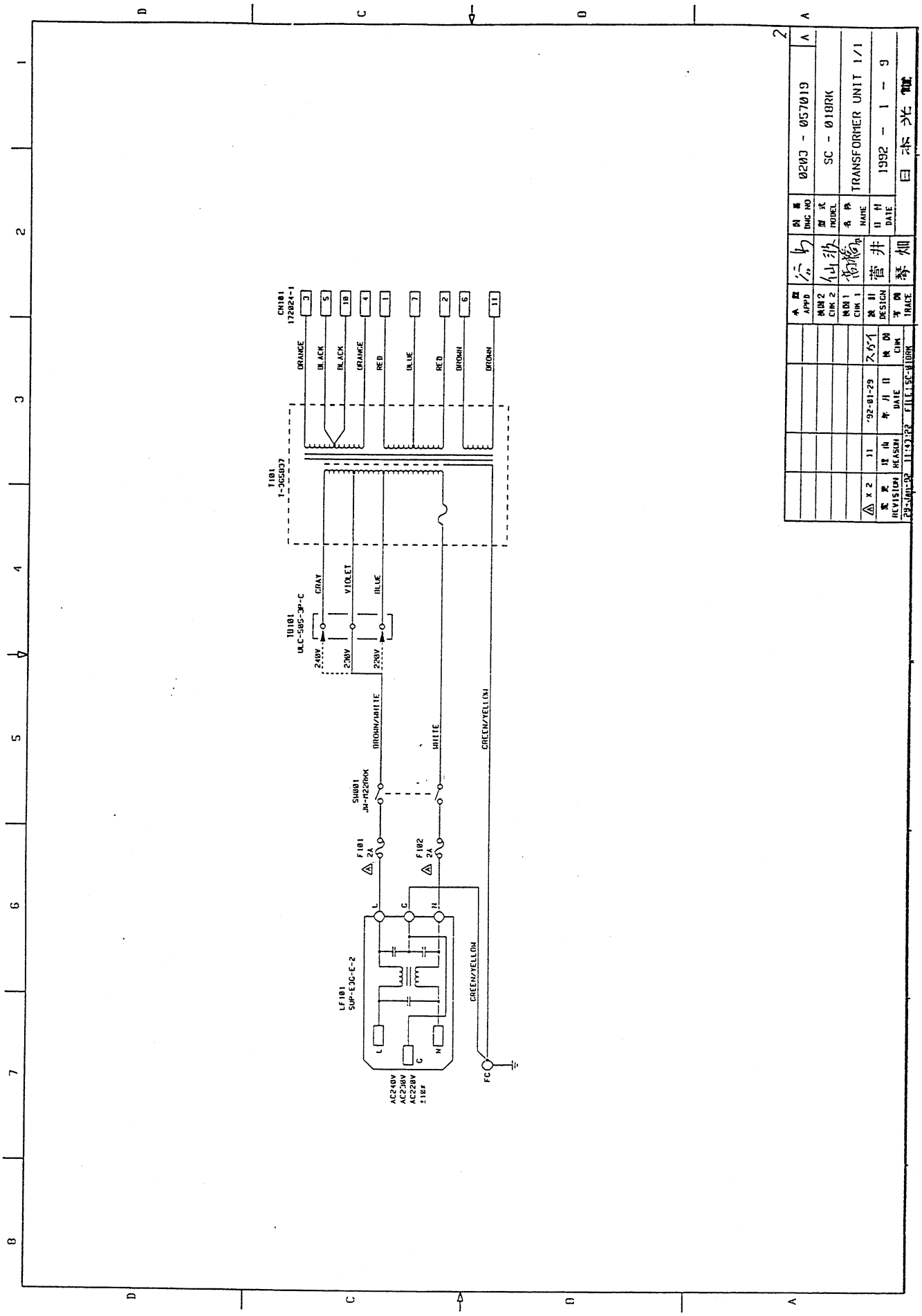


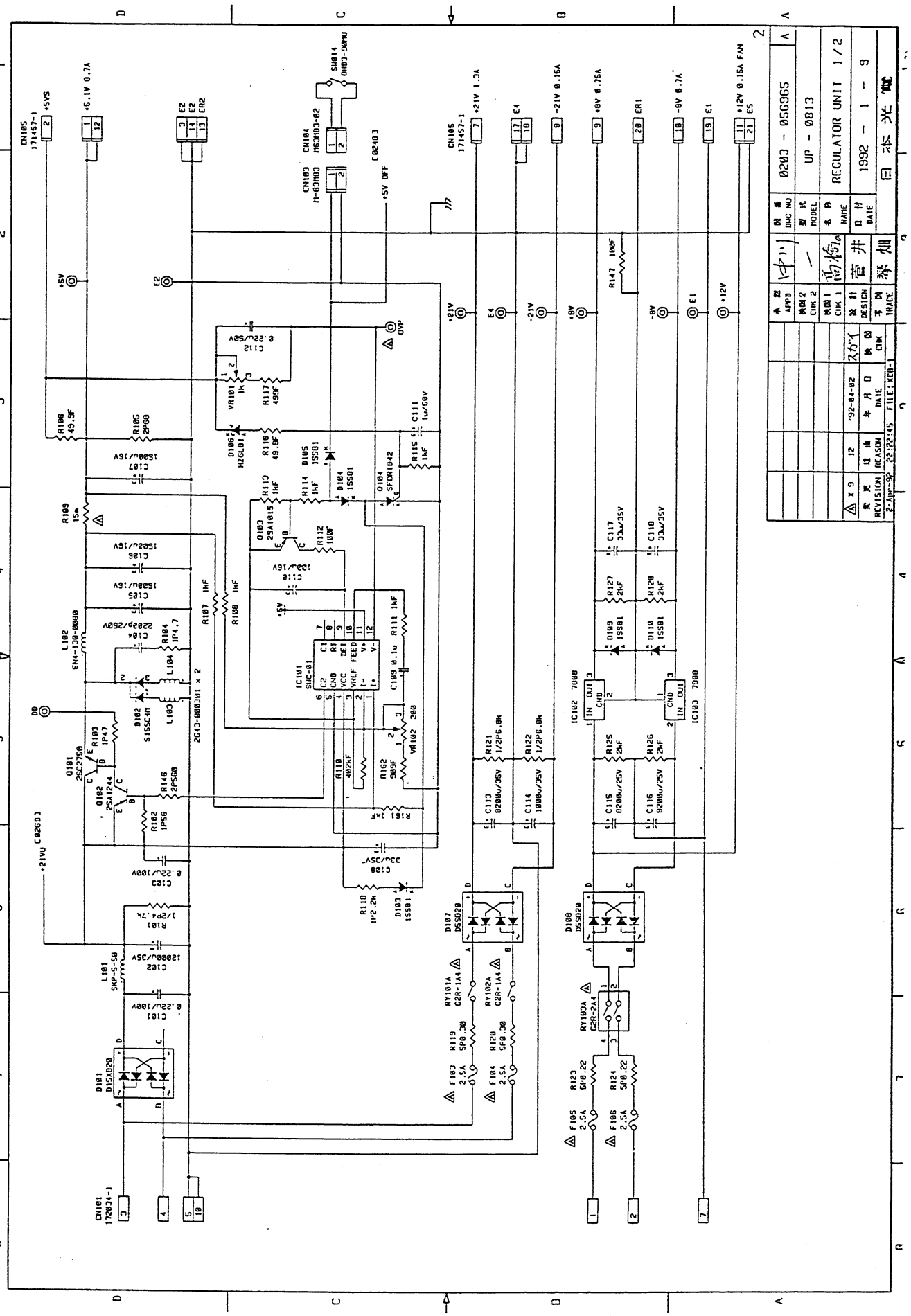

CN101
172024-1
3
5
10
4
1
7
2
6
11
ORANGE
BLACK
BLACK
ORANGE
RED
BLUE
RED
BROWN
BROWN
T101
T-365819
SW001
JA-M22RKK
RED
WHITE
GREEN/YELLOW
F101
3A
F101
3A
LF101
SUP-E3G-E-2
L
G
N
AC117V
±10%
FG
図番 DHC NO 0203 - 056992
型式 MODEL SC - 018RA
名称 NAME TRANSFORMER UNIT 1/1
日付 DATE 1992 - 1 - 9
日本光電
承認 APPD 冷助
検図2 CHK 2 仙波
検図1 CHK 1 窓榊
設計 DESIGN 菅井
写図 TRACE 琴畑
検図 CHK
年月日 DATE
理由 REASON
変更 REVISION
9-Jan-92 15:28:49 FILE:SC-018RA

NO CONTENTS

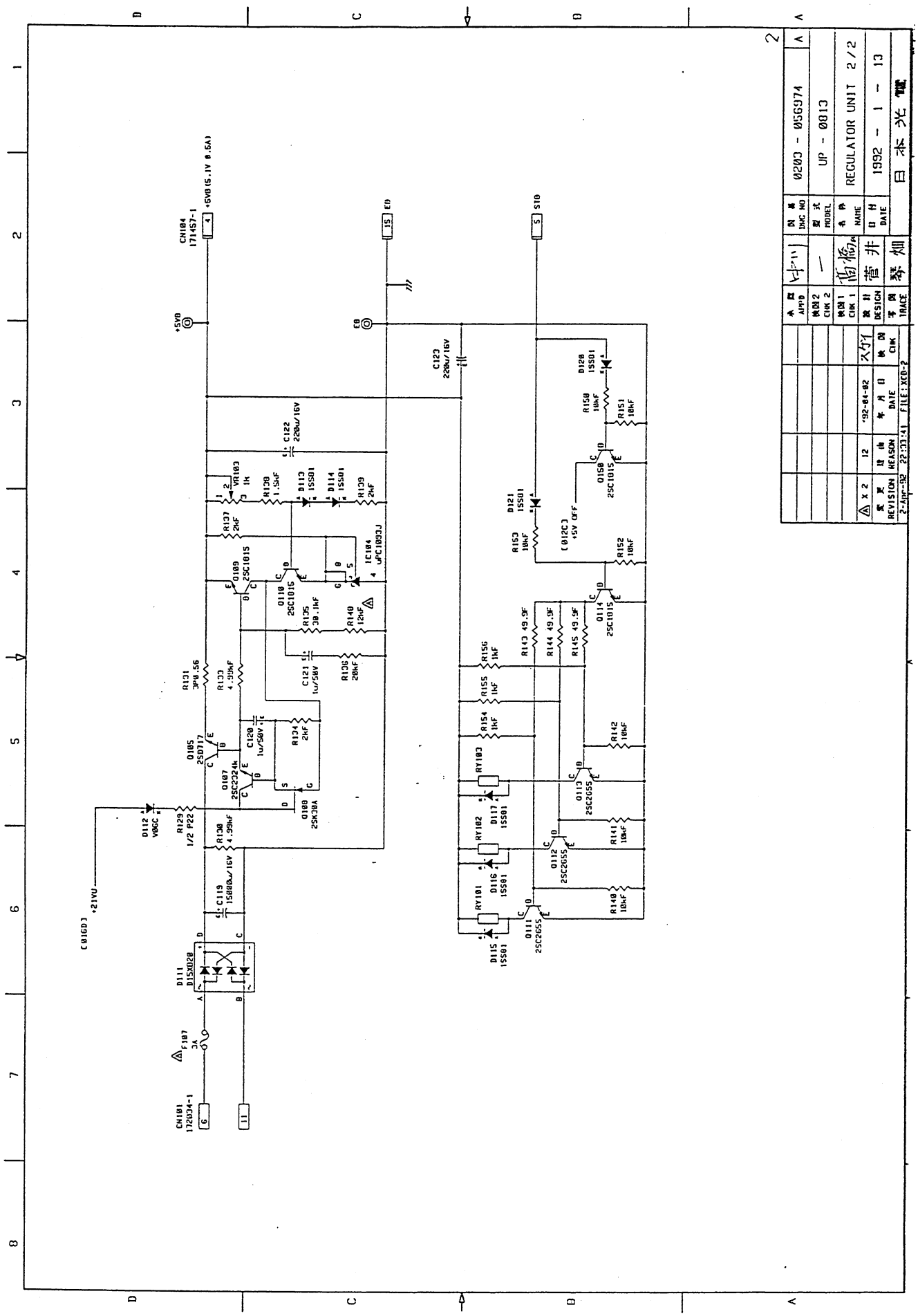

CN101
172024-1
ORANGE
BLACK
BLACK
ORANGE
RED
BLUE
RED
BROWN
BROWN
T101
1-365028
TD101
ULC-505-3P-C
ORANGE
RED
BROWN
125V
117V
110V
SW01
JA-M22MK
BROWN/WHITE
WHITE
GREEN/YELLOW
F101
3A
F102
3A
LF101
SUP-E3G-E-2
L
G
N
AC125V
AC117V
AC110V
50/60Hz
FG
A 図 APPD
図 CHK 2
図 CHK 1
設 計 DESIGN
作 図 TRACE
製 CHK
図 番 DWG NO
0203 - 057001
型 式 MODEL
SC - 010RJ
名 称 NAME
TRANSFORMER UNIT 1/1
日 付 DATE
1992 - 1 - 9
日本光電
改 訂 REVISION
理 由 REASON
年 月 日 DATE
9-JAN-92 15:30:28 FILE SC-010RJ

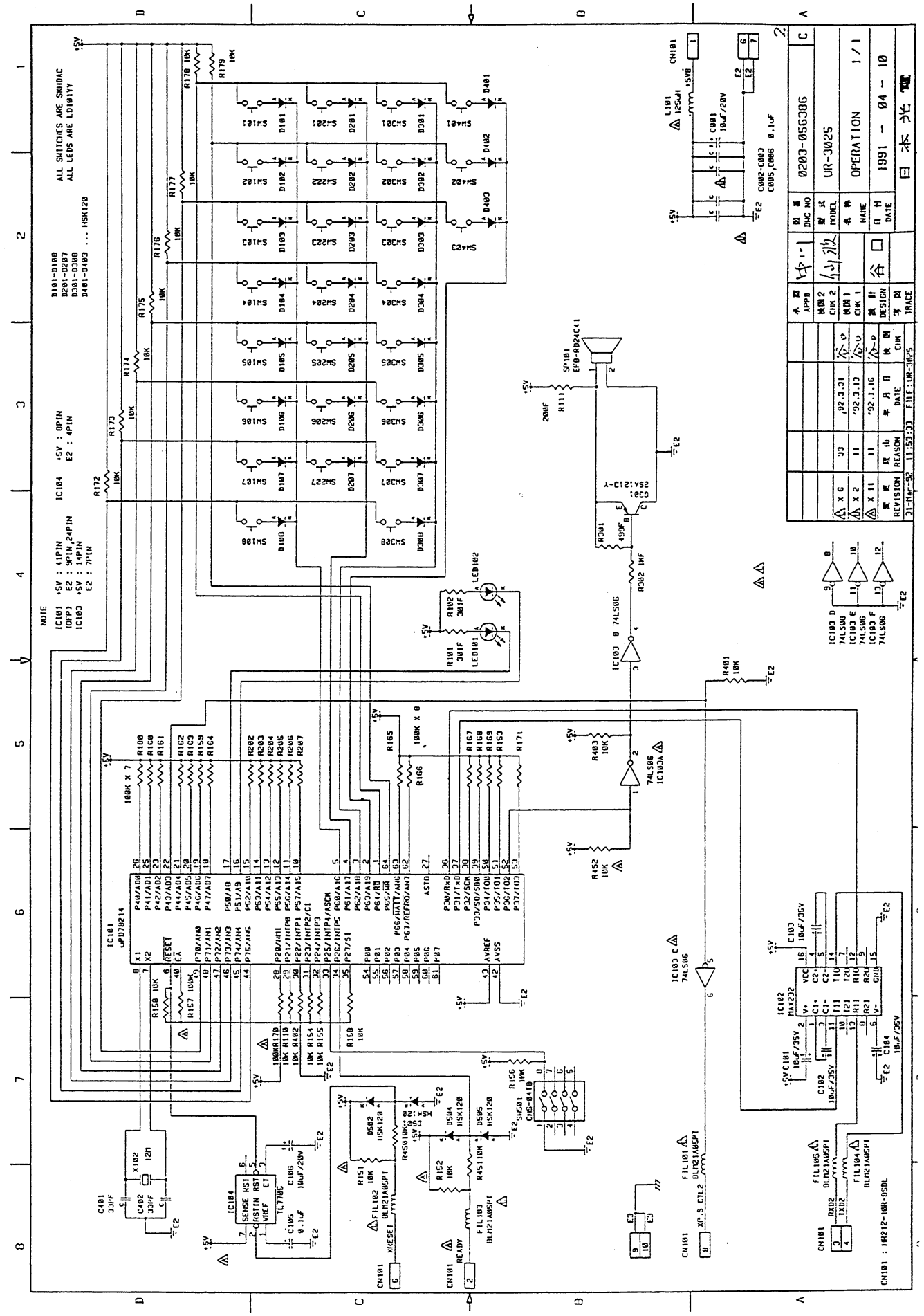
12. CIRCUIT DIAGRAM



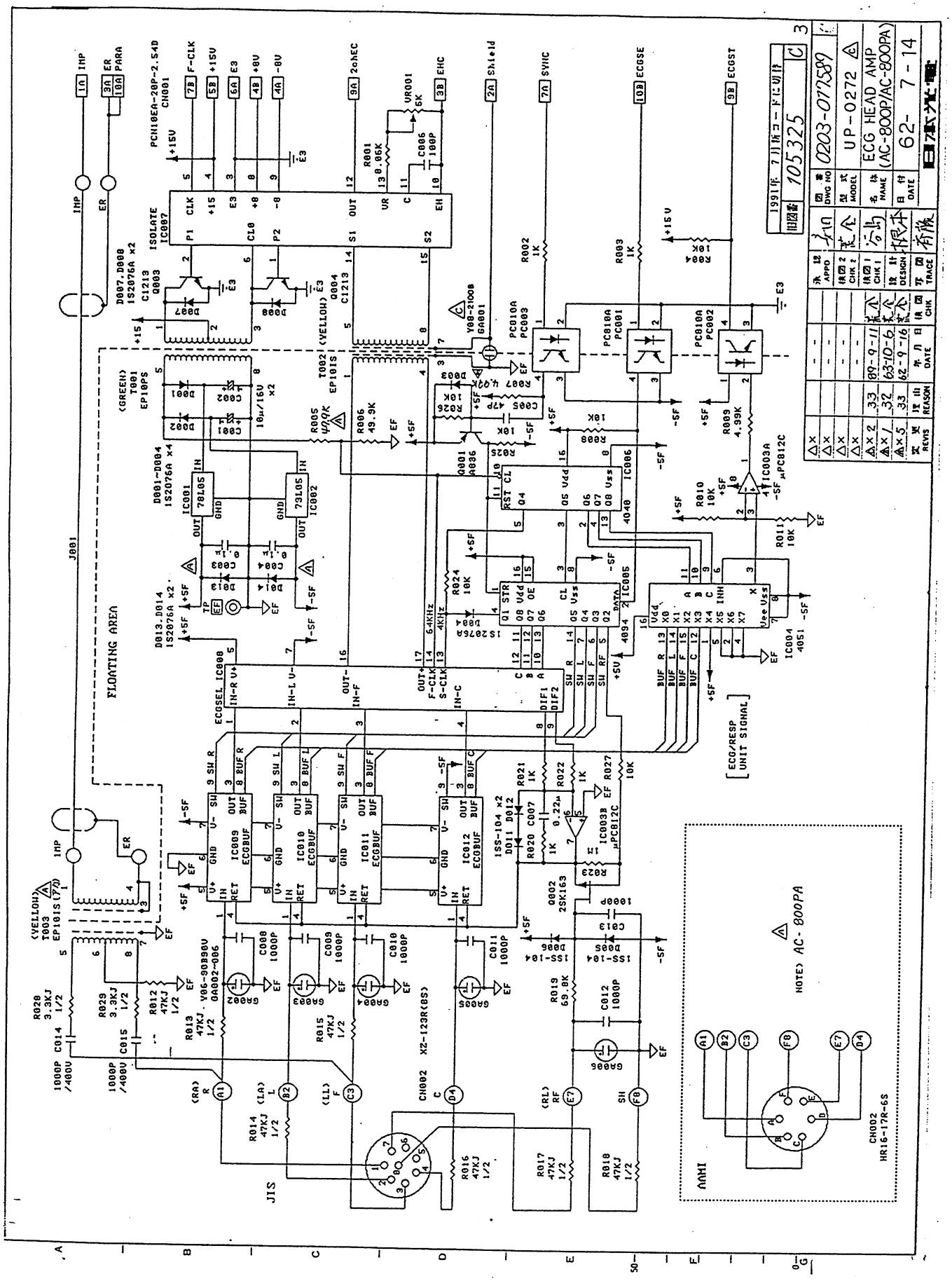

0203 - 0S6965
UP - 0813
REGULATOR UNIT 1/2
1992 - 1 - 9
日本光電
CN105
CN104
CN103
CN101
IC101
IC102
IC103
D101
D102
D103
D104
D105
D106
D107
D108
D109
D110
Q101
Q102
Q103
Q104
L101
L102
L103
L104
SW101
+5V
+6.1V 0.7A
+21V 1.3A
-21V 0.16A
+8V 0.75A
-8V 0.7A
+12V 0.15A FAN
+5V OFF
OVP
+21VU

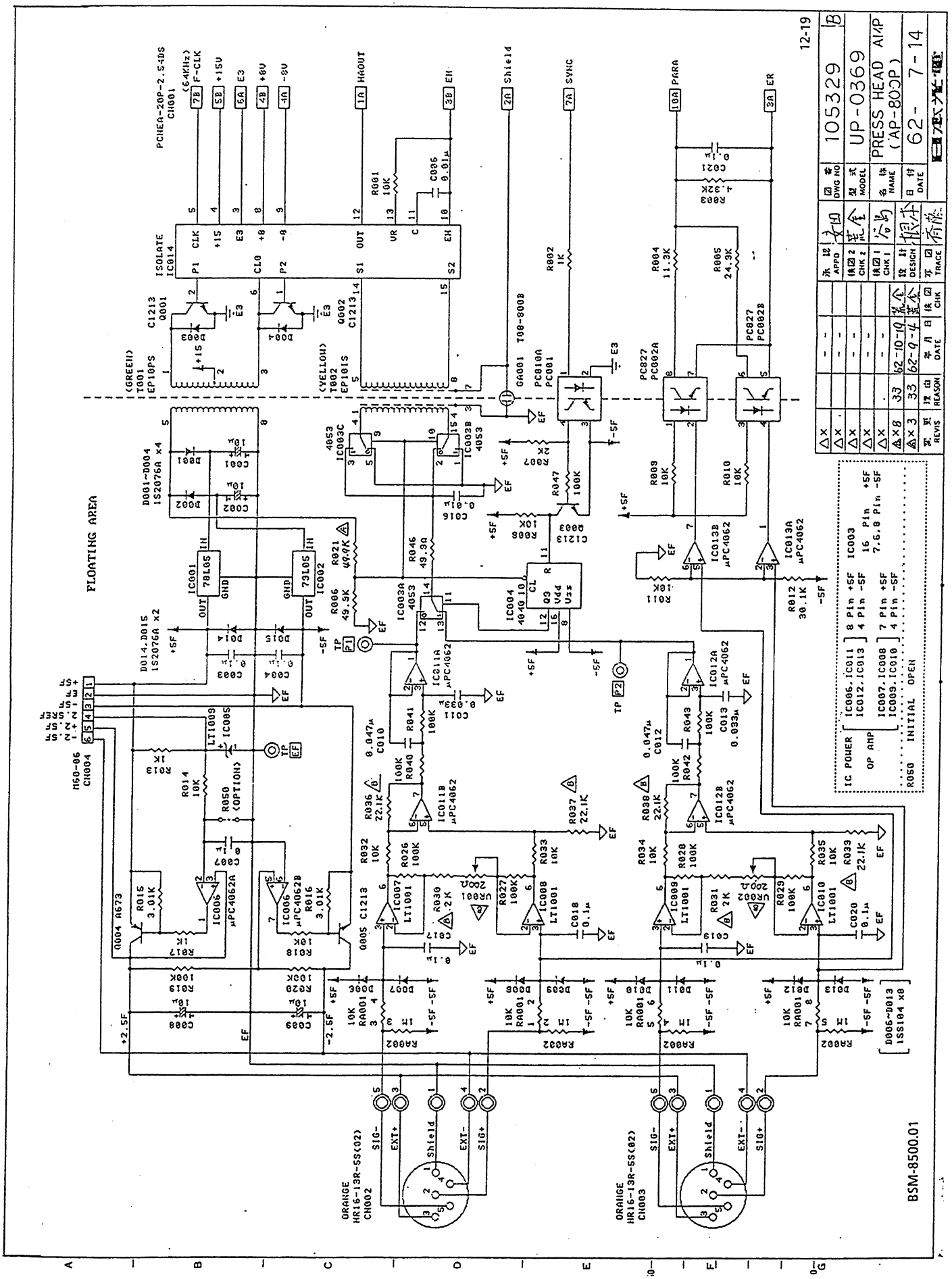
12. CIRCUIT DIAGRAM



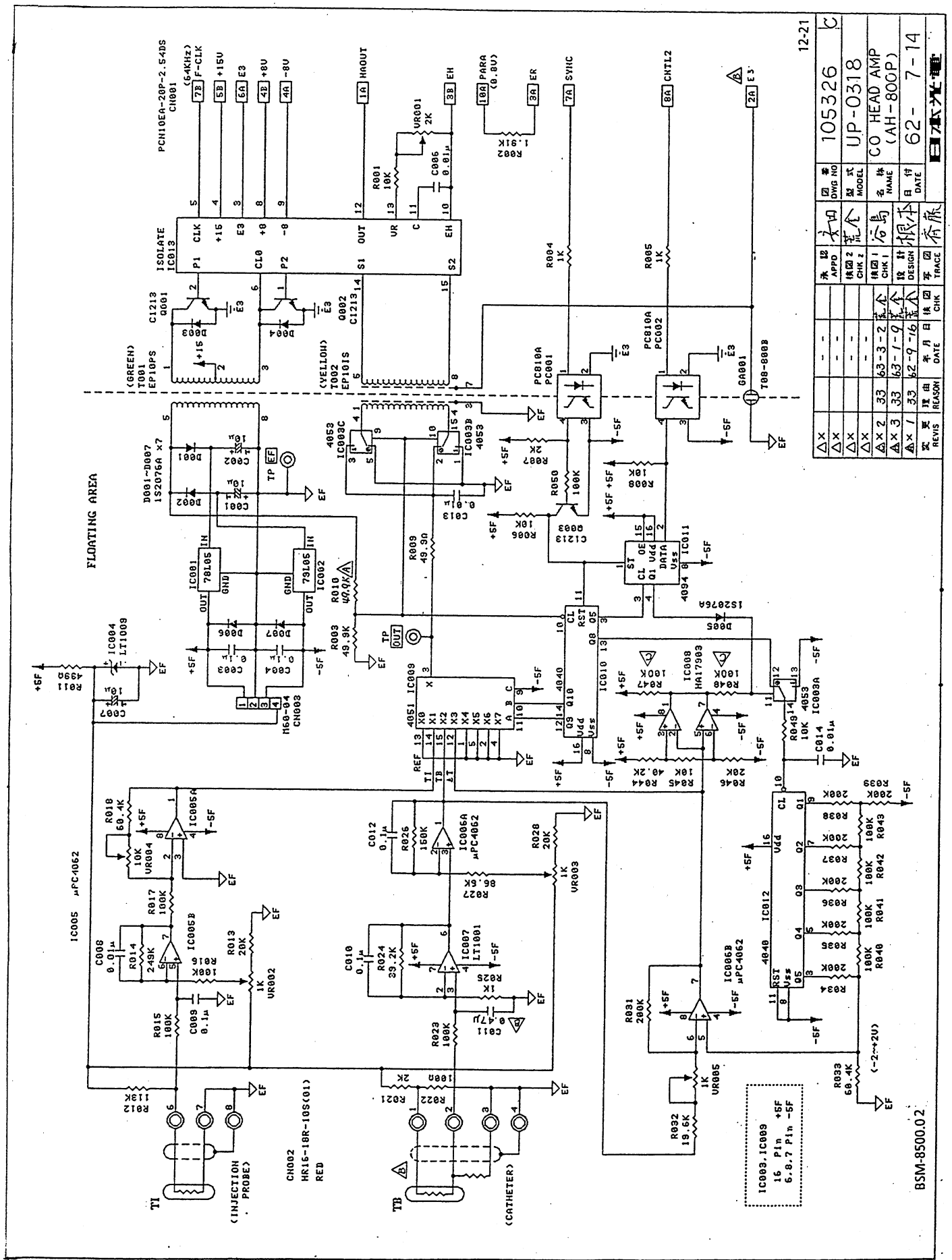


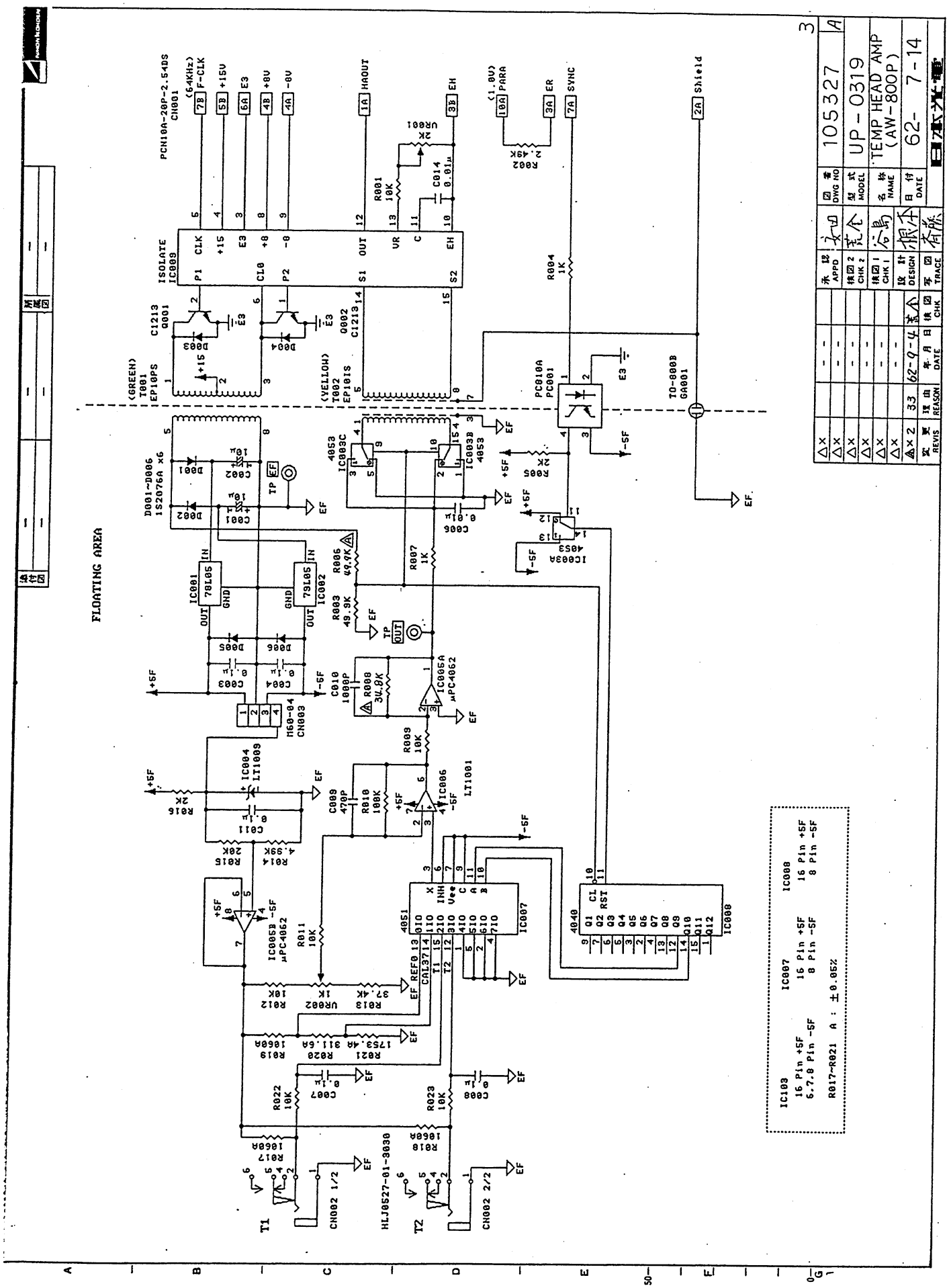
12. CIRCUIT DIAGRAM



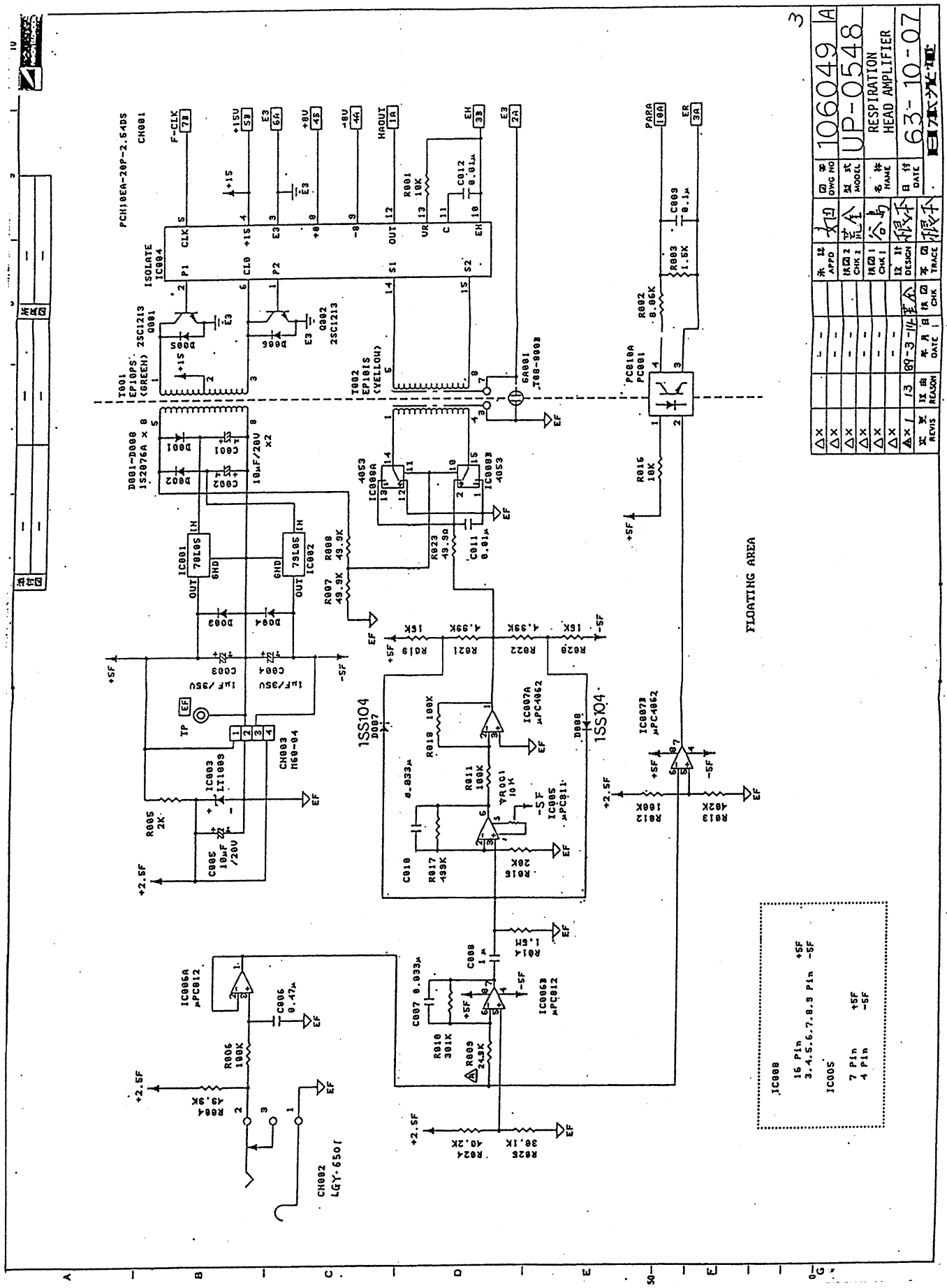

FLOATING AREA
12-19
105329
UP-0369
PRESS HEAD AMP
(AP-800)
62- 7- 14
BSM-8500.01

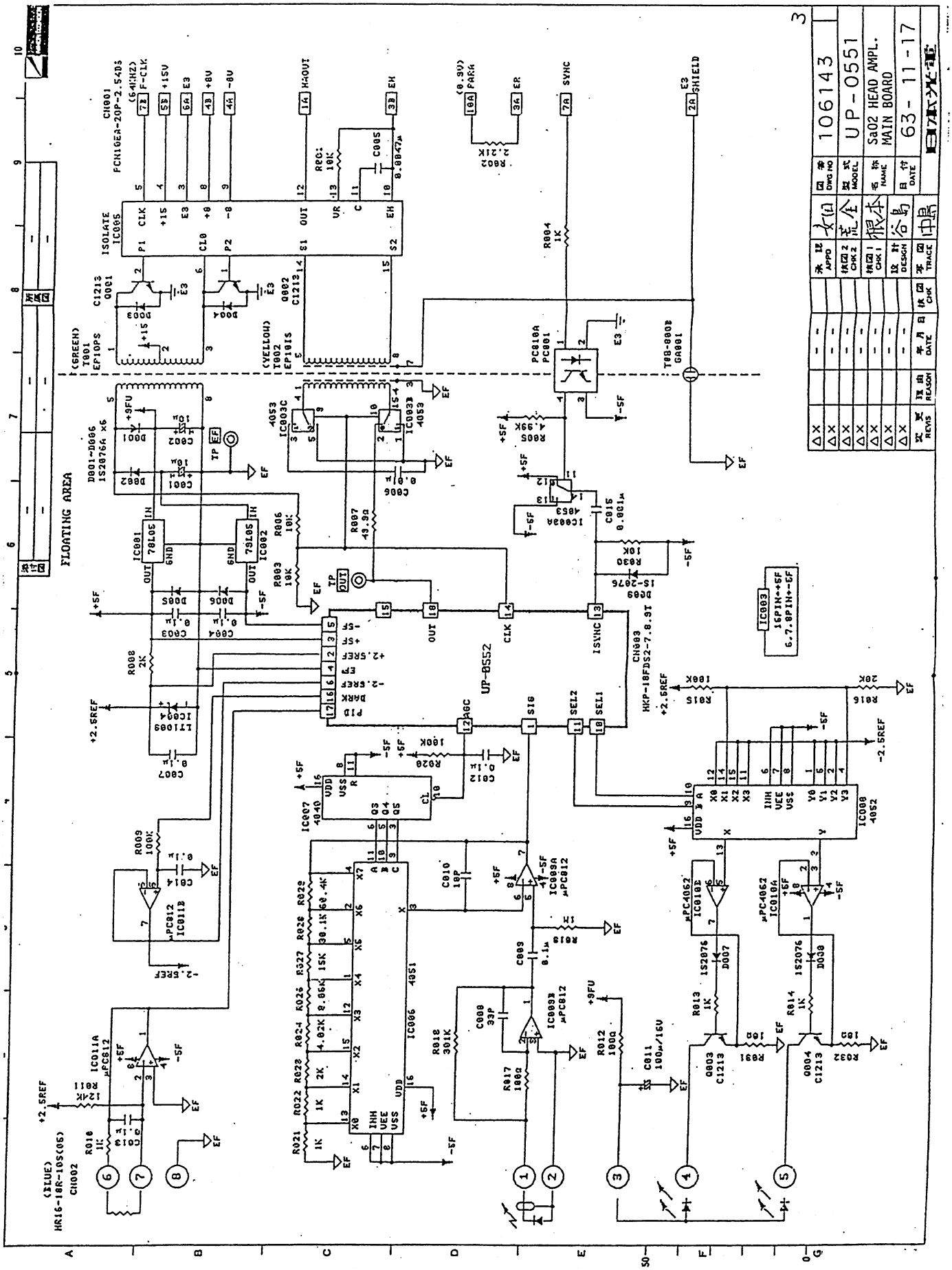
12. CIRCUIT DIAGRAM



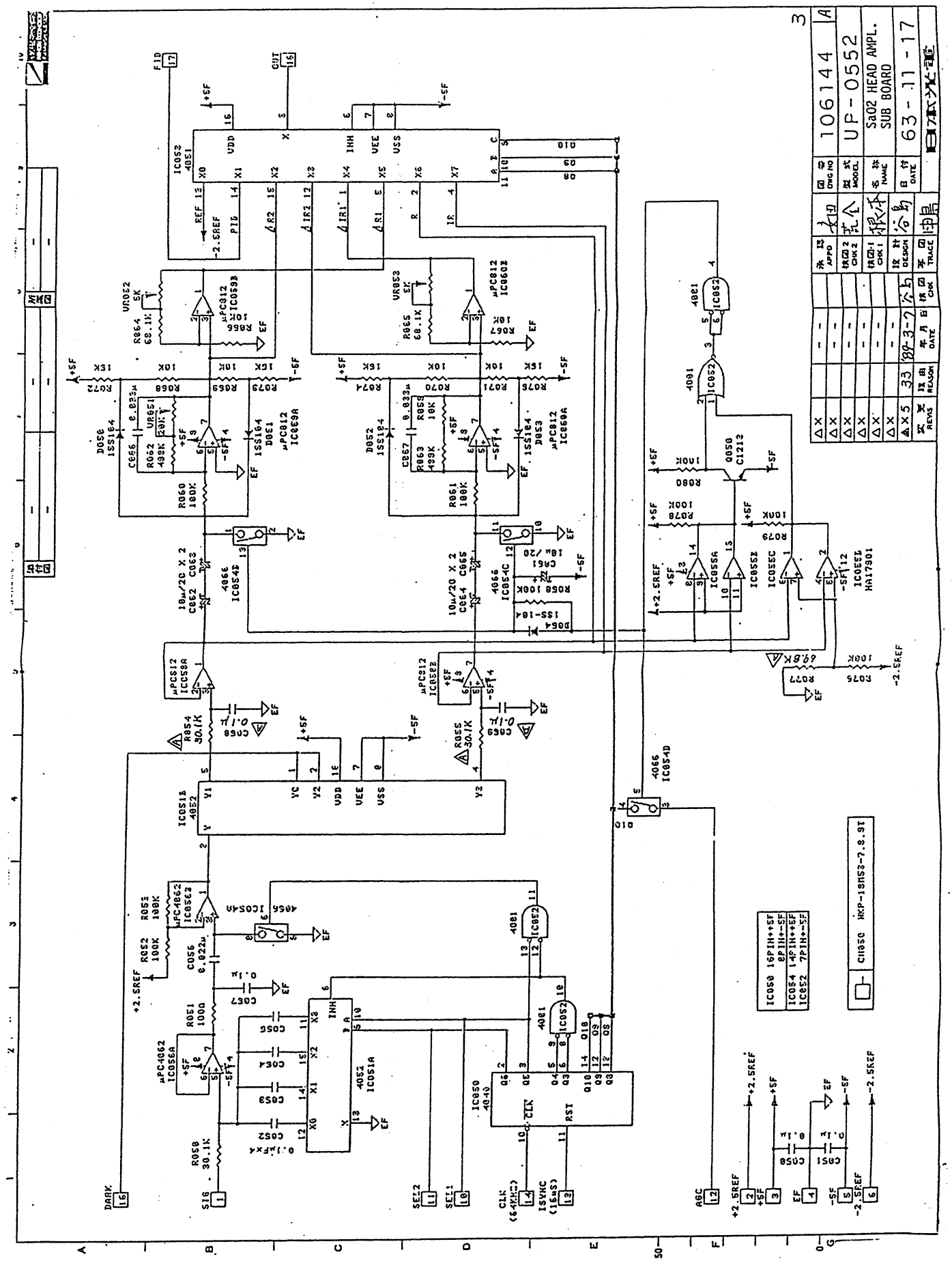

105327
UP-0319
TEMP HEAD AMP
(AW-800P)
62- 7-14
FLOATING AREA
IC103
16 Pin +5F
6.7.8 Pin -5F
IC007
16 Pin +5F
8 Pin -5F
IC008
16 Pin +5F
8 Pin -5F
R017~R021 A : ±0.05%

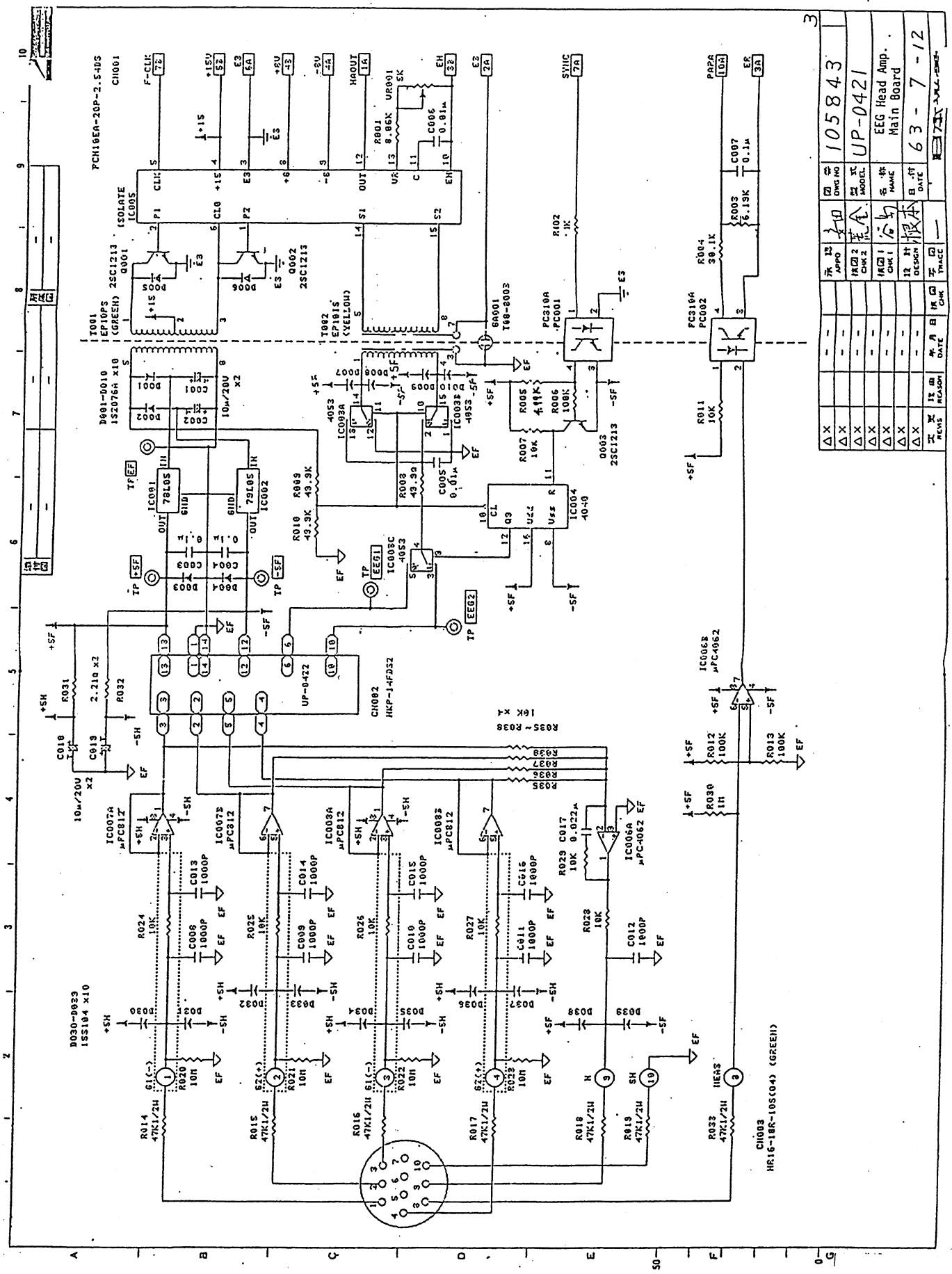
12. CIRCUIT DIAGRAM



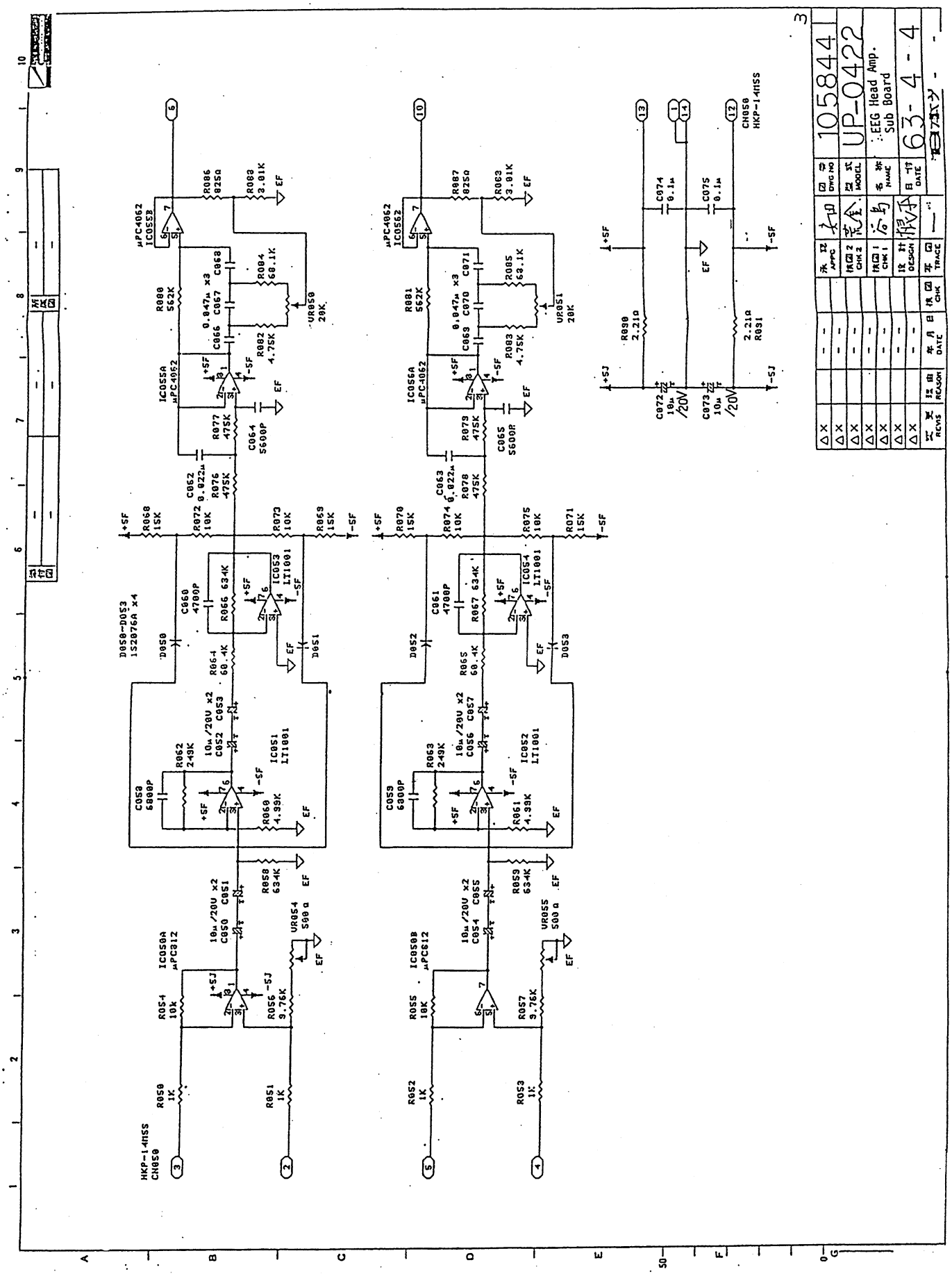

106143
UP-0551
SA02 HEAD AMPL. MAIN BOARD
63-11-17
FLOATING AREA
UP-8552
CN003
HKP-18FDS2-7.8.9T
IC003
16PIN→+5F
6,7,8PIN→-5F
CN001
FCN16EA-20P-2.54DS
(64MHZ) F-CLK
+15V
E3
+8V
-8V
H-OUT
EH
(0.3V) PARA
ER
SYNC
E3 SHIELD
(GREEN) T001 EP10PS
(YELLOW) T002 EP10IS
PC810A PC001
T80-0008 GA001
ISOLATE IC005
REG: 10K
8.0047μ
R804 1K
R805 4.99K
R802 2.21K
D001-0006 1S2076A ×6
IC001 78L05
IC002 79L05
IC003C 4053
IC003B 4053
IC008A 4053
R003 10K
R006 10K
R007 49.9Ω
R008 2K
R009 100K
R028 100K
R030 10K
R015 100K
R016 20K
IC007 4040
IC008 4052
IC006 4051
IC009A μPC812
IC009B μPC812
IC011A μPC812
IC011B μPC812
IC010A μPC4052
IC010B μPC4052
R011 2K
R010 1K
R012 100Ω
R017 100Ω
R018 301K
R019 1K
C009 0.1μ
C010 18P
C008 33P
C011 100μ/16V
R013 1K
R014 1K
R031 10Ω
R032 10Ω
Q003 C1213
Q004 C1213
D007 1S2076
D008 1S2076
(BLUE) HR16-18R-10S(06) CN002

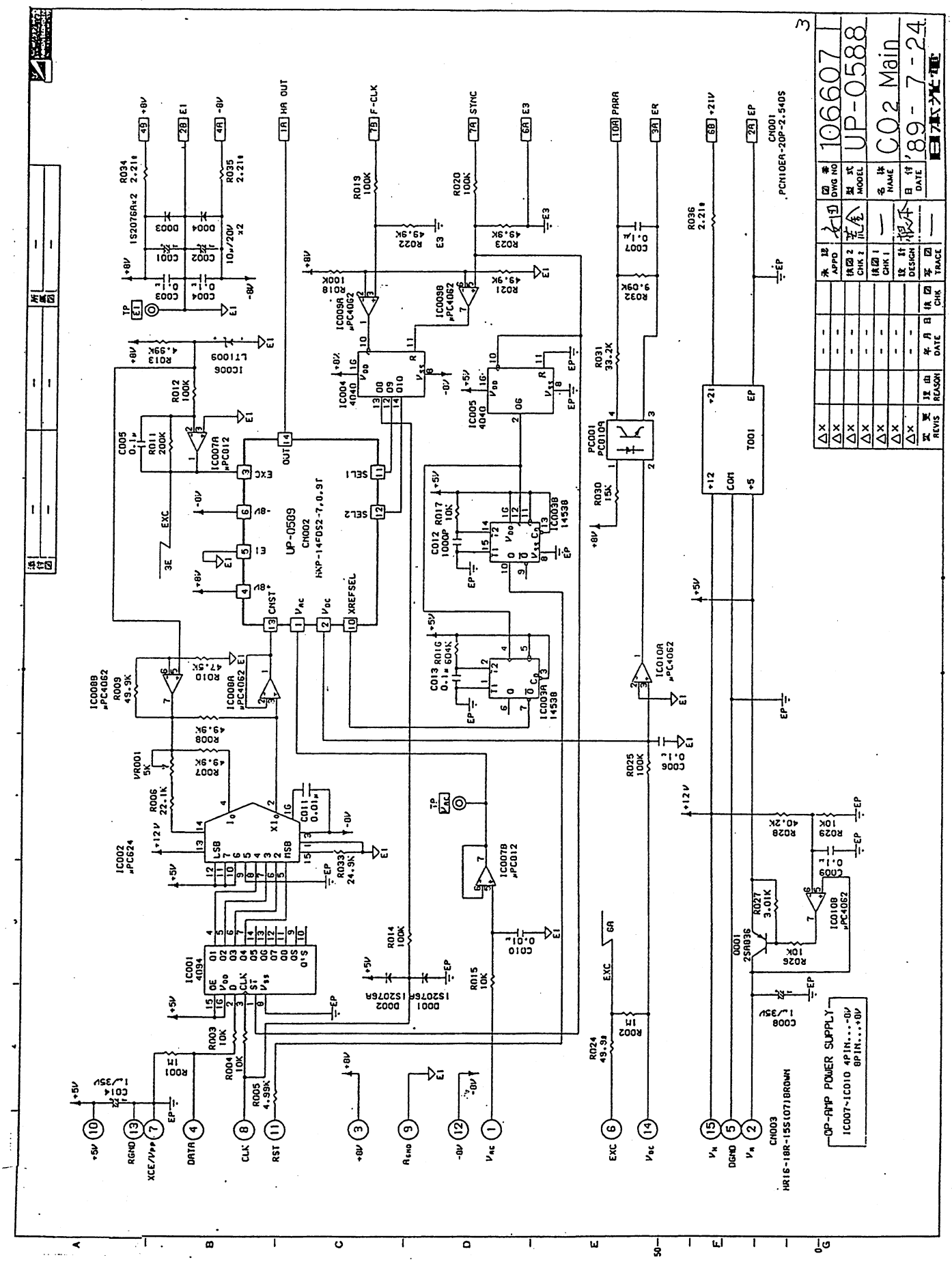
12. CIRCUIT DIAGRAM



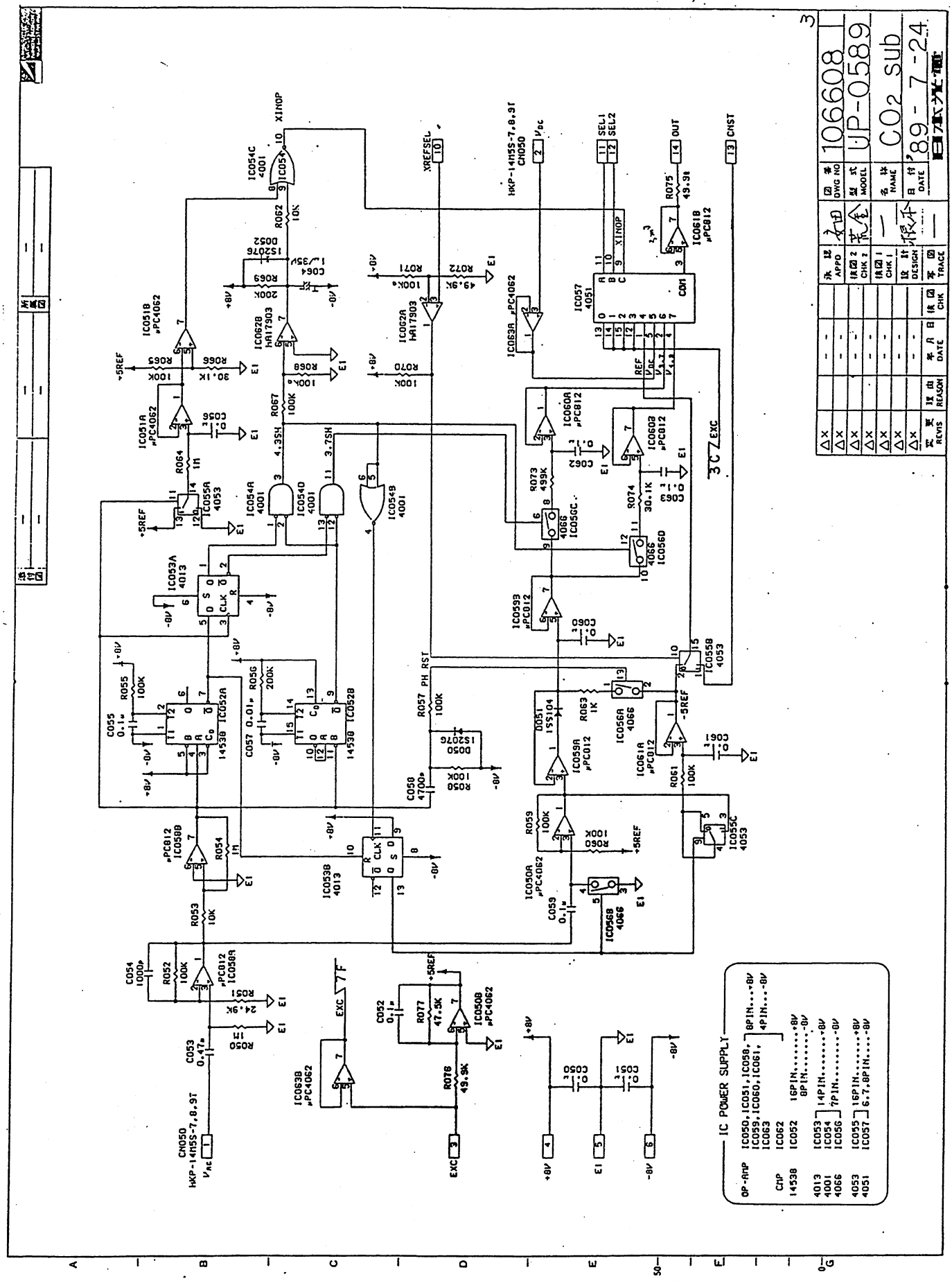

105843
UP-0421
EEG Head Amp.
Main Board
63 - 7 - 12

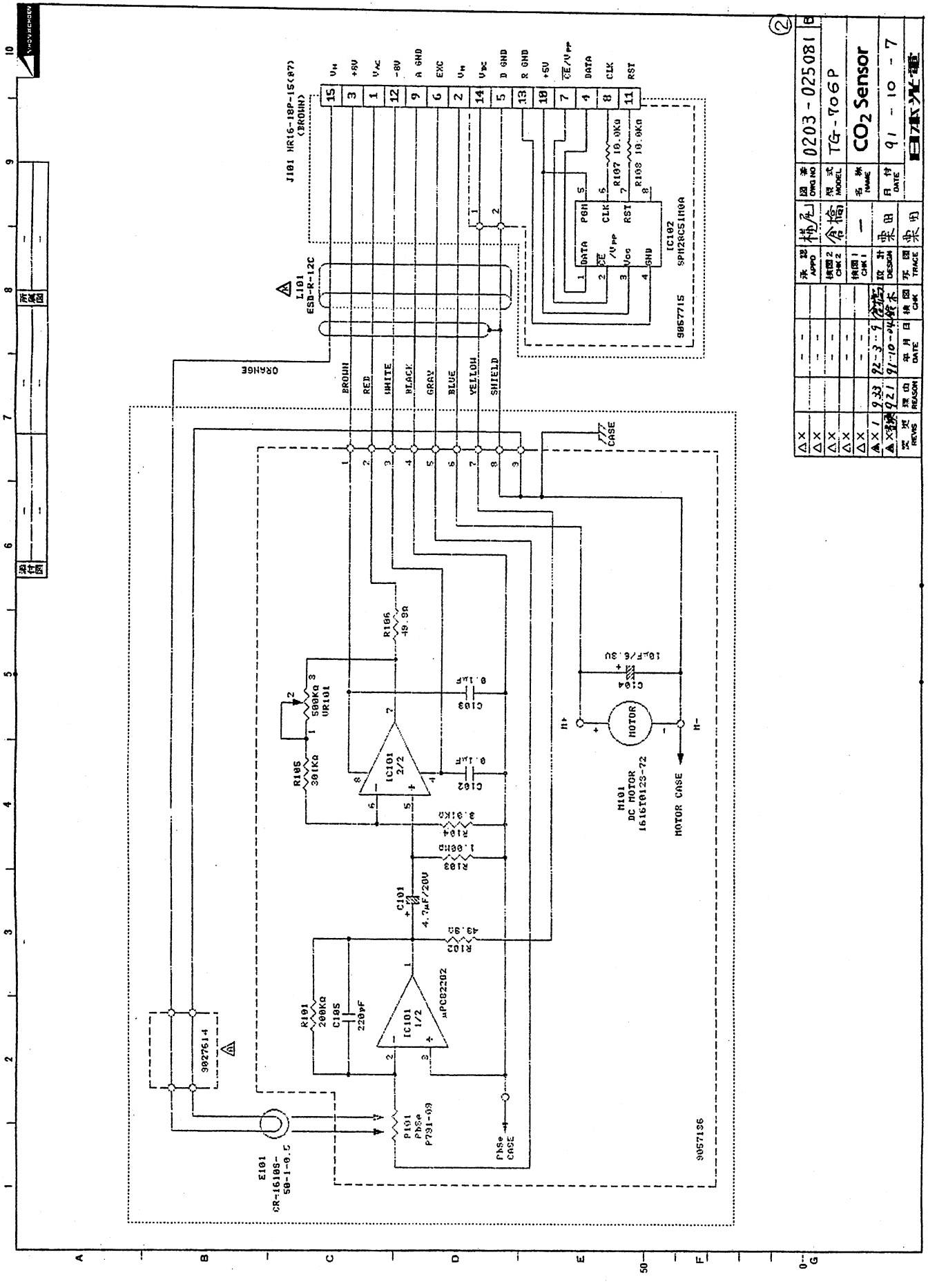
12. CIRCUIT DIAGRAM



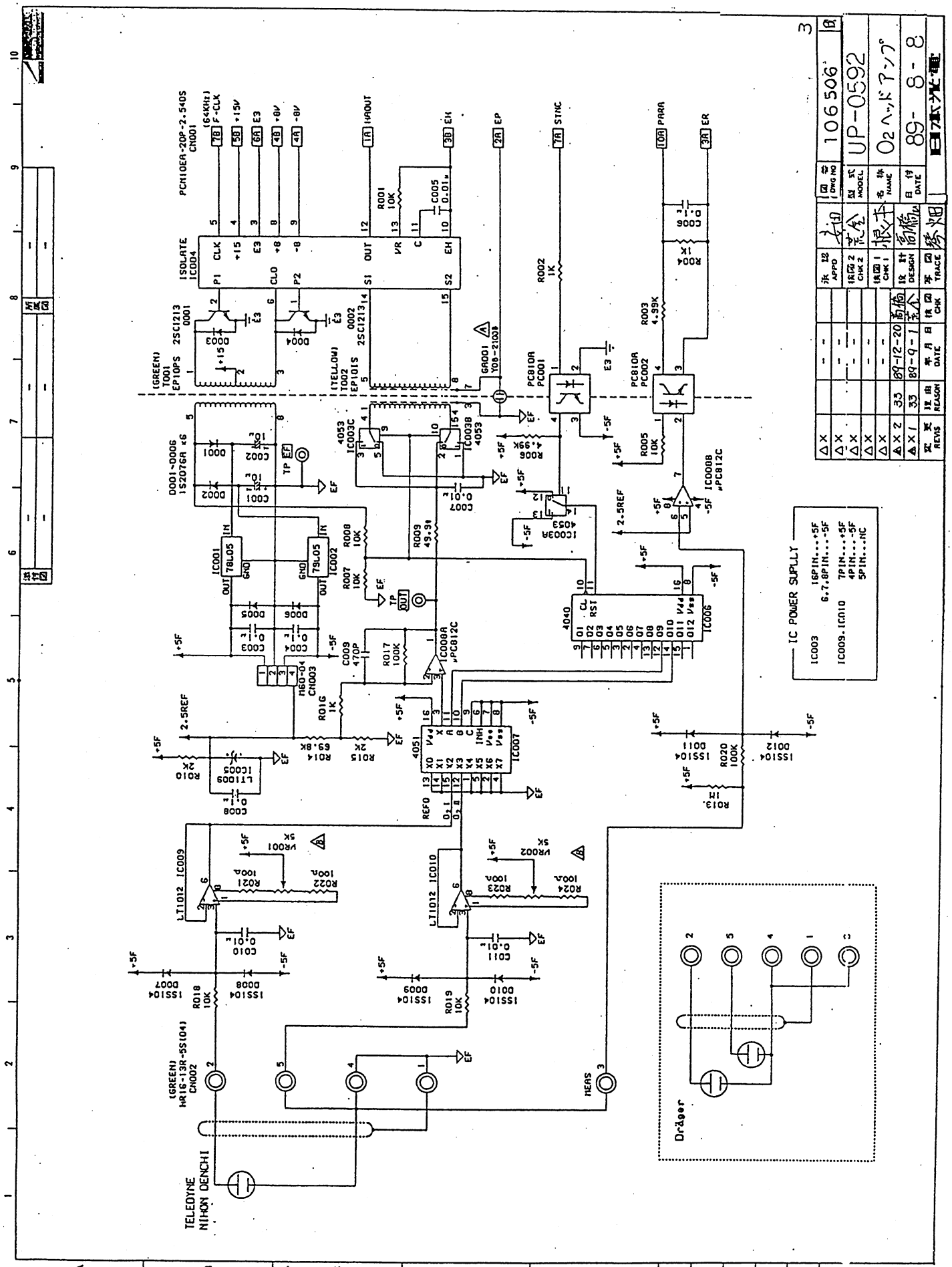

106607
UP-0588
C02 Main
'89-7-24
UP-0509
CN002
HKP-14FDS2-7,0.9I
OP-AMP POWER SUPPLY
IC007~IC010 4PIN...-8V
8PIN...+8V
CN003
HR16-18R-15S(07)BROWN
CN001
PCN10EA-20P-2.54DS
+5V
RGND
XCE/Vpp
DATA
CLK
RST
+8V
AGND
-8V
VAC
EXC
VDC
VM
DGND
VM
+12V
+21V
EP
HA OUT
F-CLK
SYNC
PARA
ER
E1
E2
E3
GA

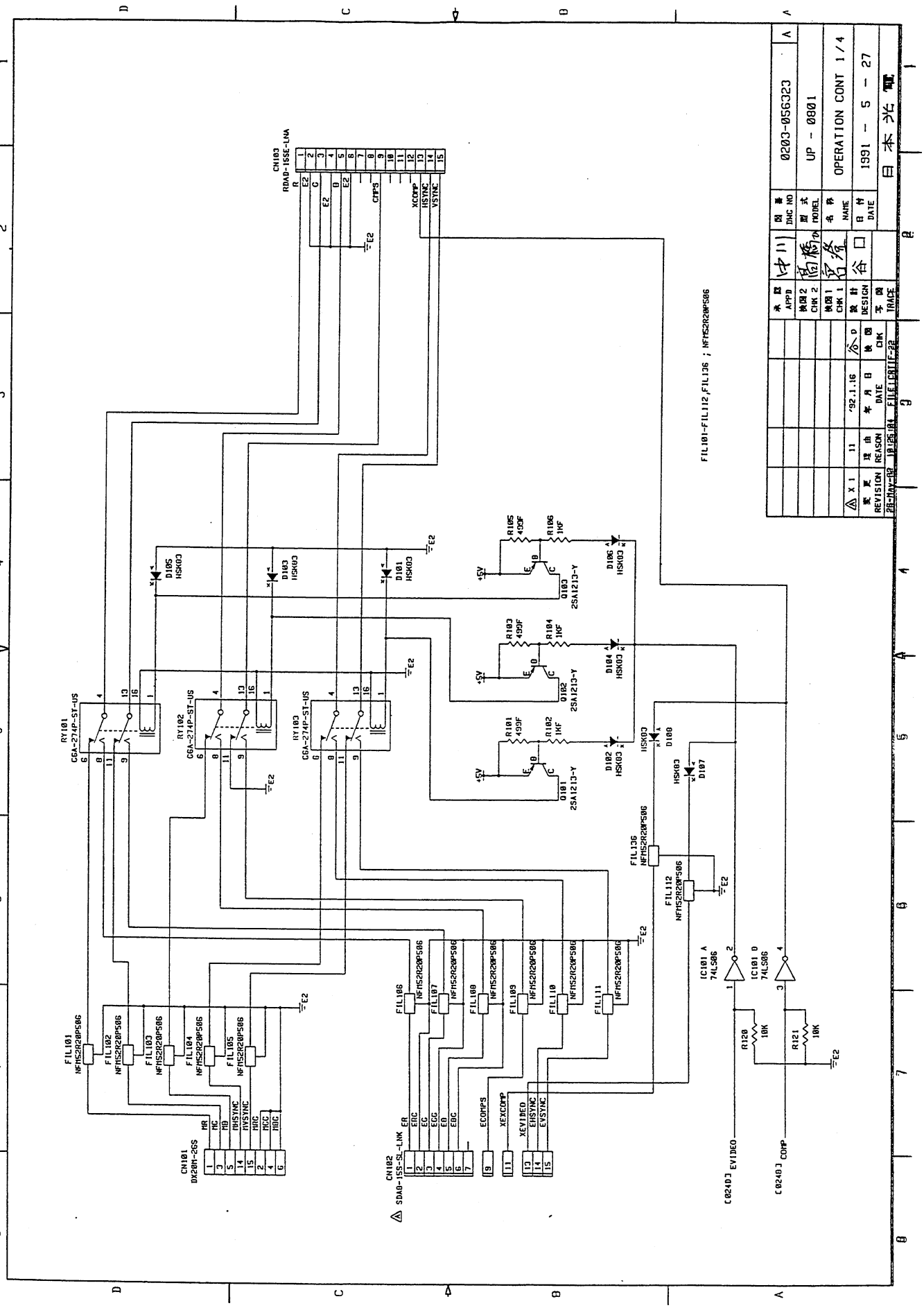
12. CIRCUIT DIAGRAM



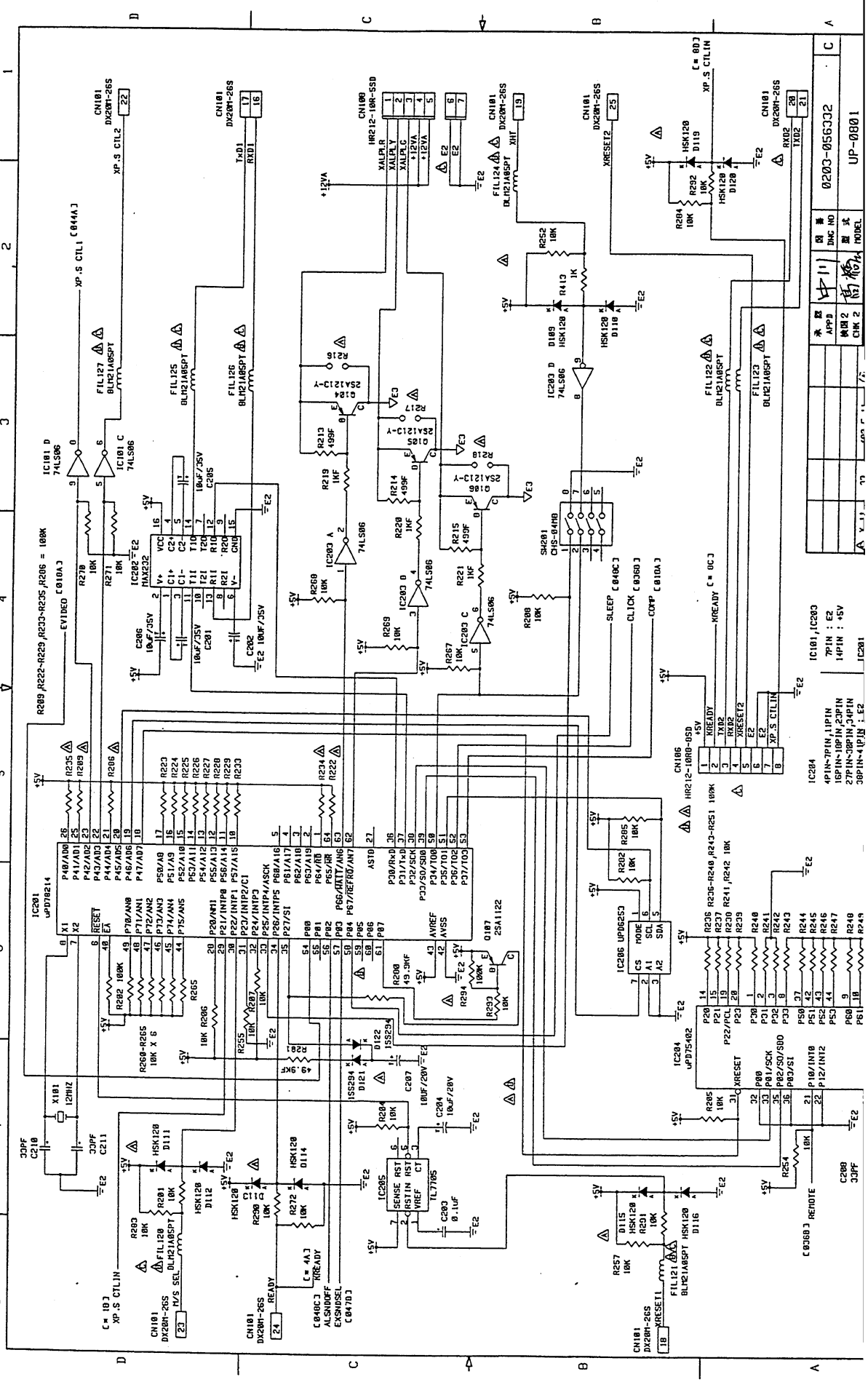

0203-025081
TG-706P
CO2 Sensor
91-10-7
J101 HR16-10P-15(87) (BROWN)
L101 ESD-R-12C
IC102 SPM28C51M0A
9057715
ORANGE
BROWN
RED
WHITE
BLACK
GRAY
BLUE
YELLOW
SHIELD
CASE
R106 49.9Ω
VR101 500KΩ
R105 301KΩ
IC101 2/2
C103 0.1μF
C102 0.1μF
R104 3.01KΩ
R103 1.00MΩ
C101 4.7μF/20V
R102 43.2Ω
IC101 1/2
μPC82202
R101 200KΩ
C105 220pF
P101 Phase P731-09
Phse CASE
E101 CR-16108-50-1-0.5
3027614
9057136
C104 10μF/6.3V
M+
M-
M101 DC MOTOR 1616T0123-72
MOTOR CASE
MOTOR

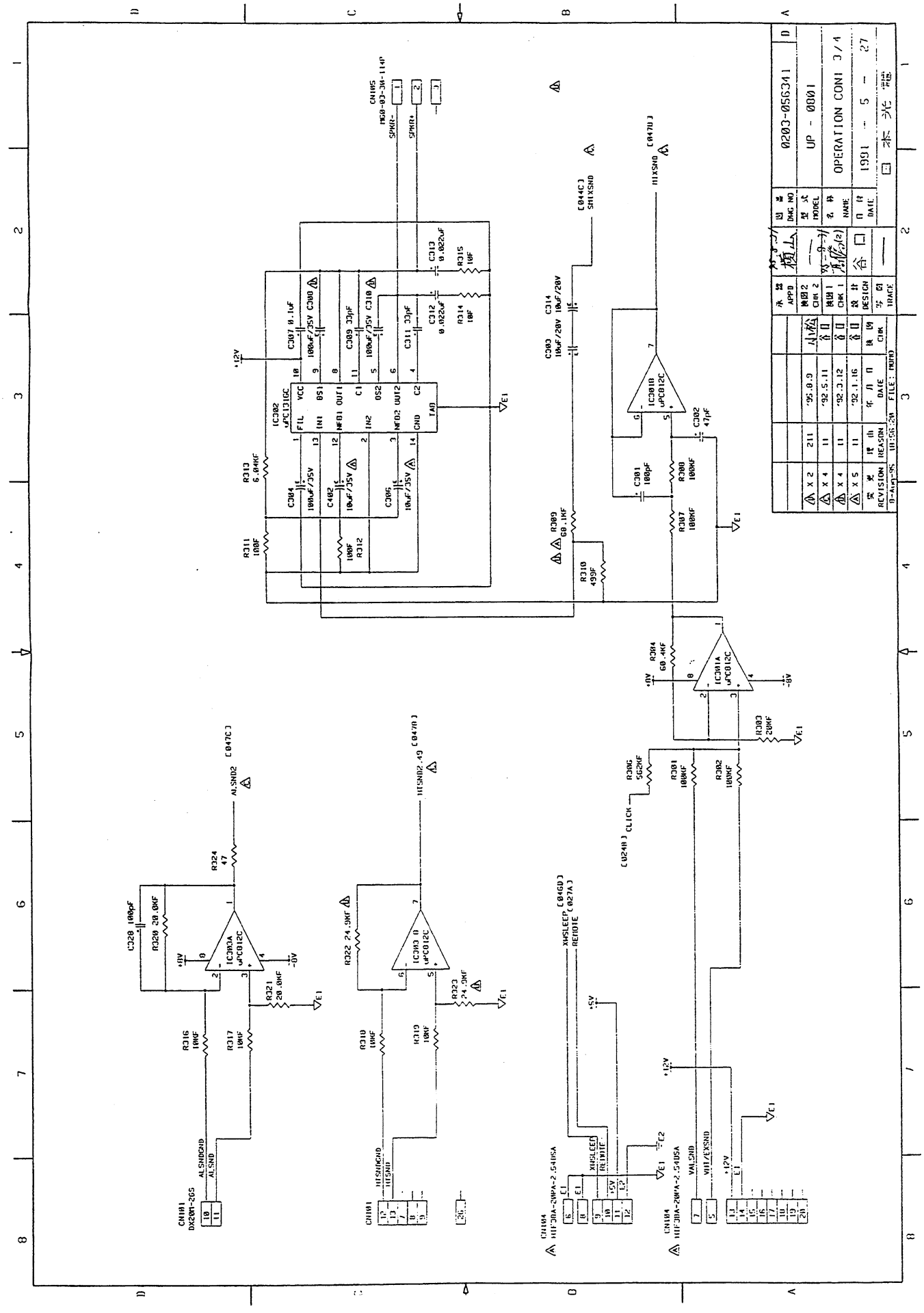
12. CIRCUIT DIAGRAM



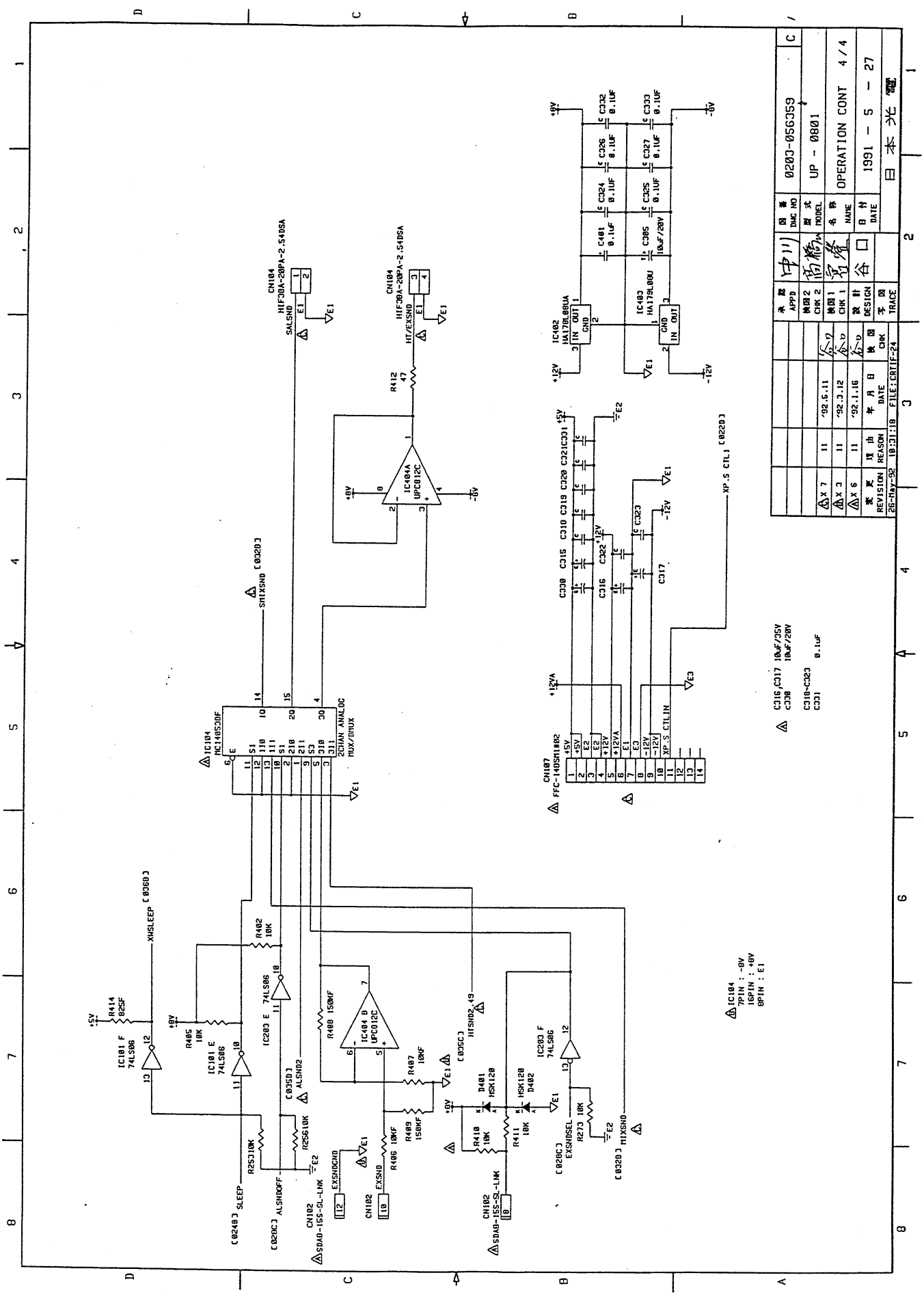

0203-056323
UP - 0901
OPERATION CONT 1/4
1991 - 5 - 27
日本光電
FIL101-FIL112,FIL136 ; NFM52R20P506
CN103 RDA0-15SE-LNA
CN101 DX20M-26S
CN102 SDA0-15S-SL-LNK
RY101 CGA-274P-ST-US
RY102 CGA-274P-ST-US
RY103 CGA-274P-ST-US
D105 HSK03
D103 HSK03
D101 HSK03
D106 HSK03
D104 HSK03
D102 HSK03
D108 HSK03
D107 HSK03
Q103 2SA1213-Y
Q102 2SA1213-Y
Q101 2SA1213-Y
R105 499F
R106 1KF
R103 499F
R104 1KF
R101 499F
R102 1KF
FIL101 NFM52R20P506
FIL102 NFM52R20P506
FIL103 NFM52R20P506
FIL104 NFM52R20P506
FIL105 NFM52R20P506
FIL106 NFM52R20P506
FIL107 NFM52R20P506
FIL108 NFM52R20P506
FIL109 NFM52R20P506
FIL110 NFM52R20P506
FIL111 NFM52R20P506
FIL136 NFM52R20P506
FIL112 NFM52R20P506
IC101 A 74LS06
IC101 D 74LS06
R120 10K
R121 10K
C0240J EVIDEO
C0240J COMP
+5V
E2

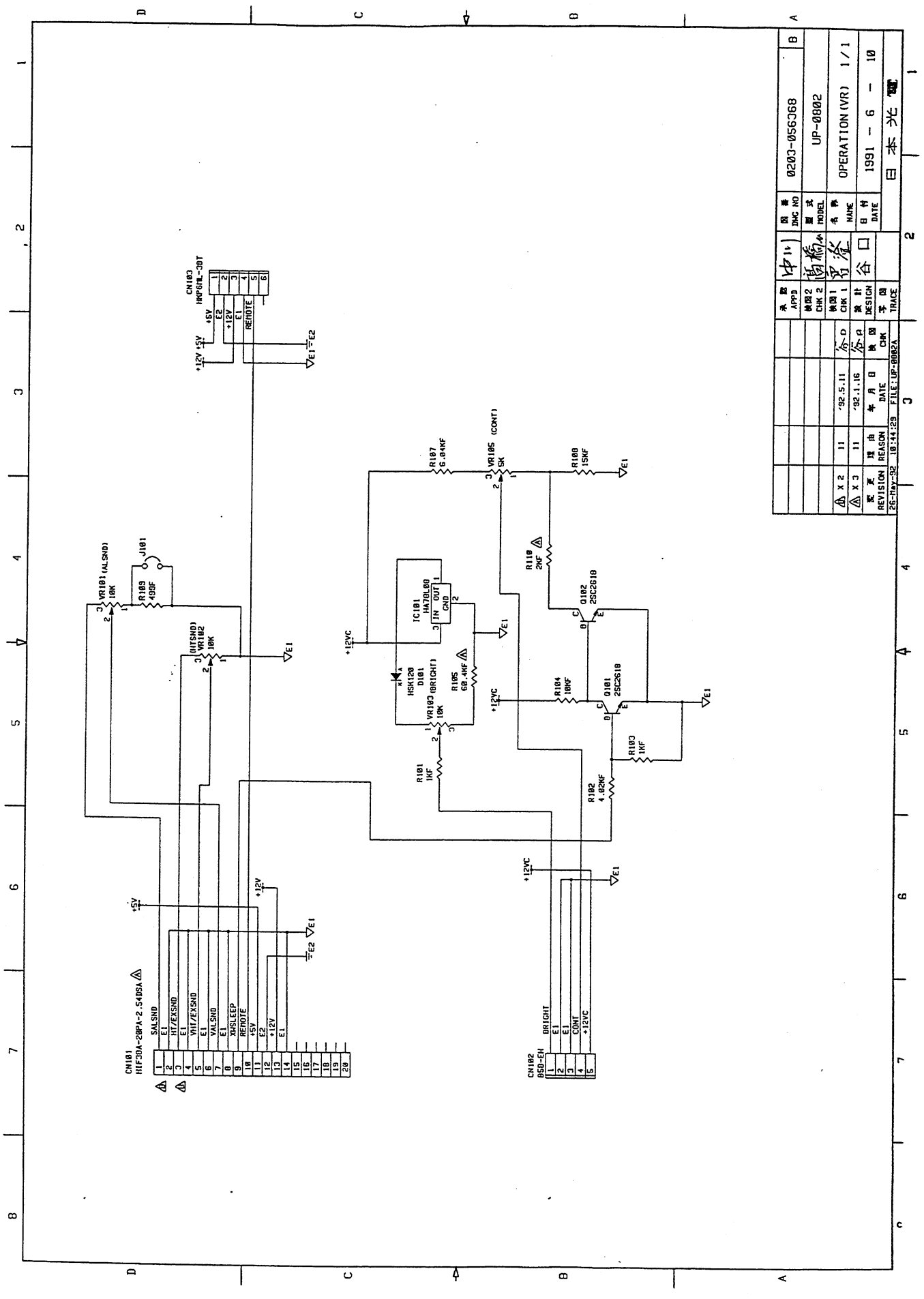
12. CIRCUIT DIAGRAM



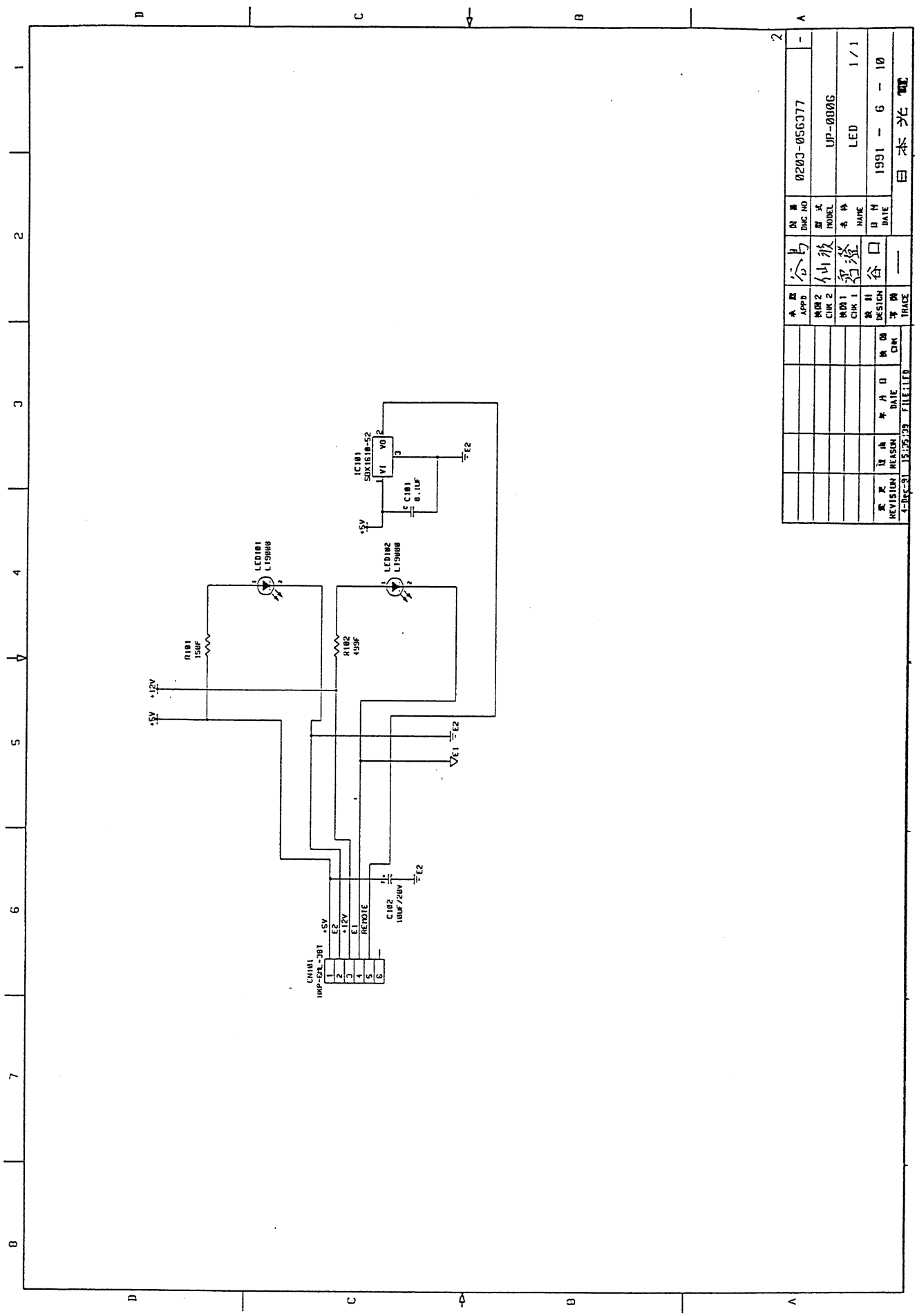

0203-05634 1
UP - 0001
OPERATION CONT 3/4
1991 - 5 - 27
IC302 μPC1310C
IC303A μPC812C
IC303B μPC812C
IC301A μPC812C
IC301B μPC812C
CN105 MS0-03-3M-114P
CN101 DX20M-26S
CN104 HIF3BA-20PA-2.54DSA
CN103 HIF3BA-20PA-2.54DSA
SPKR-
SPKR+
+12V
-12V
+5V
+8V
-8V
E1
E2
ALSNDGND
ALSND
HISNDGND
HISND
XHSLEEP
REMOTE
VALSND
VHIFXSND
CLICK
ALSND2
HISND2
LHXSND
SHXSND
XHSLEEP
R324 47
R321 20.0KF
R323 24.9KF
R313 6.04KF
R311 100F
R312 100F
R309 60.1KF
R310 499F
R303 20KF
R304 60.4KF
R305 562KF
R301 100KF
R302 100KF
R307 100KF
R308 100KF
R314 10F
R315 10F
R316 100F
R317 100F
R318 100F
R319 100F
C328 100pF
C307 0.1uF
C309 33pF
C311 33pF
C312 0.022uF
C313 0.022uF
C314 10uF/20V
C303 10uF/20V
C301 100pF
C302 47pF
C304 100uF/35V
C402 10uF/35V
C305 10uF/35V
C306 100uF/35V
C308 100uF/35V
C310 100uF/35V
C047J
C044C
C024H
C027A
C046D

12. CIRCUIT DIAGRAM



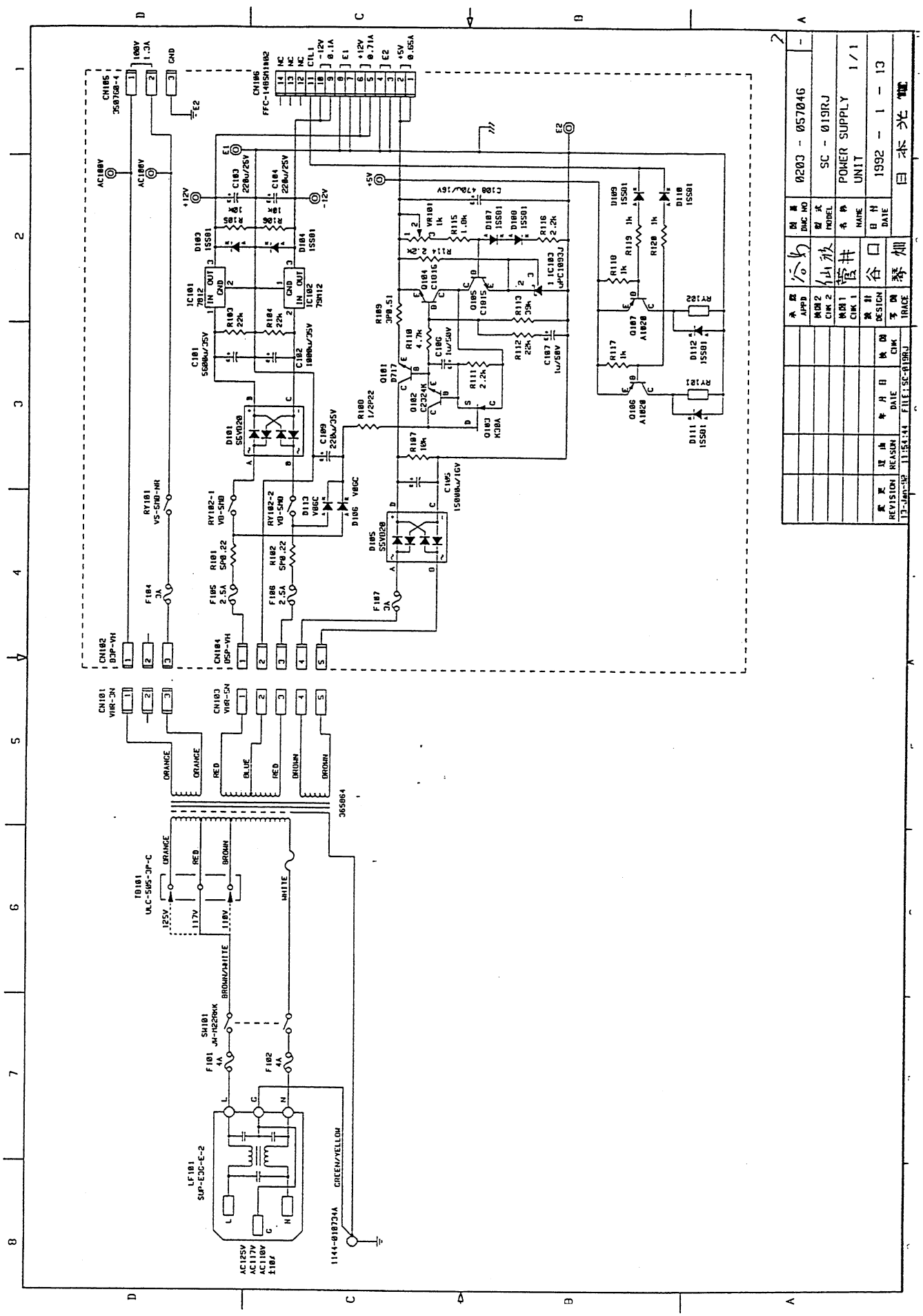

CN103
HDF6HL-30T
+5V
+12V
E2
E1
REMOTE
VR101 (VALSND)
10K
R109
430F
J101
VR102 (HTSND)
10K
IC101
HA7DL60
IN
OUT
GND
HSK120
D101
(BRIGHT)
VR103
10K
R105
60.4KF
R101
1KF
R107
6.04KF
VR105 (CONT)
5K
R108
15KF
R110
2KF
Q102
2SC2618
R104
10KF
Q101
2SC2618
R103
1KF
R102
4.02KF
+12VC
CN101
HIF3BA-20PA-2.54DSA
SALSND
HT/EXSND
VHT/EXSND
VALSND
XHSLEEP
REMOTE
CN102
05D-EH
BRIGHT
CONT
0203-05C368
UP-0002
OPERATION (VR)
1/1
1991 - 6 - 10
日本光電
26-May-92
FILE : UP-0002A

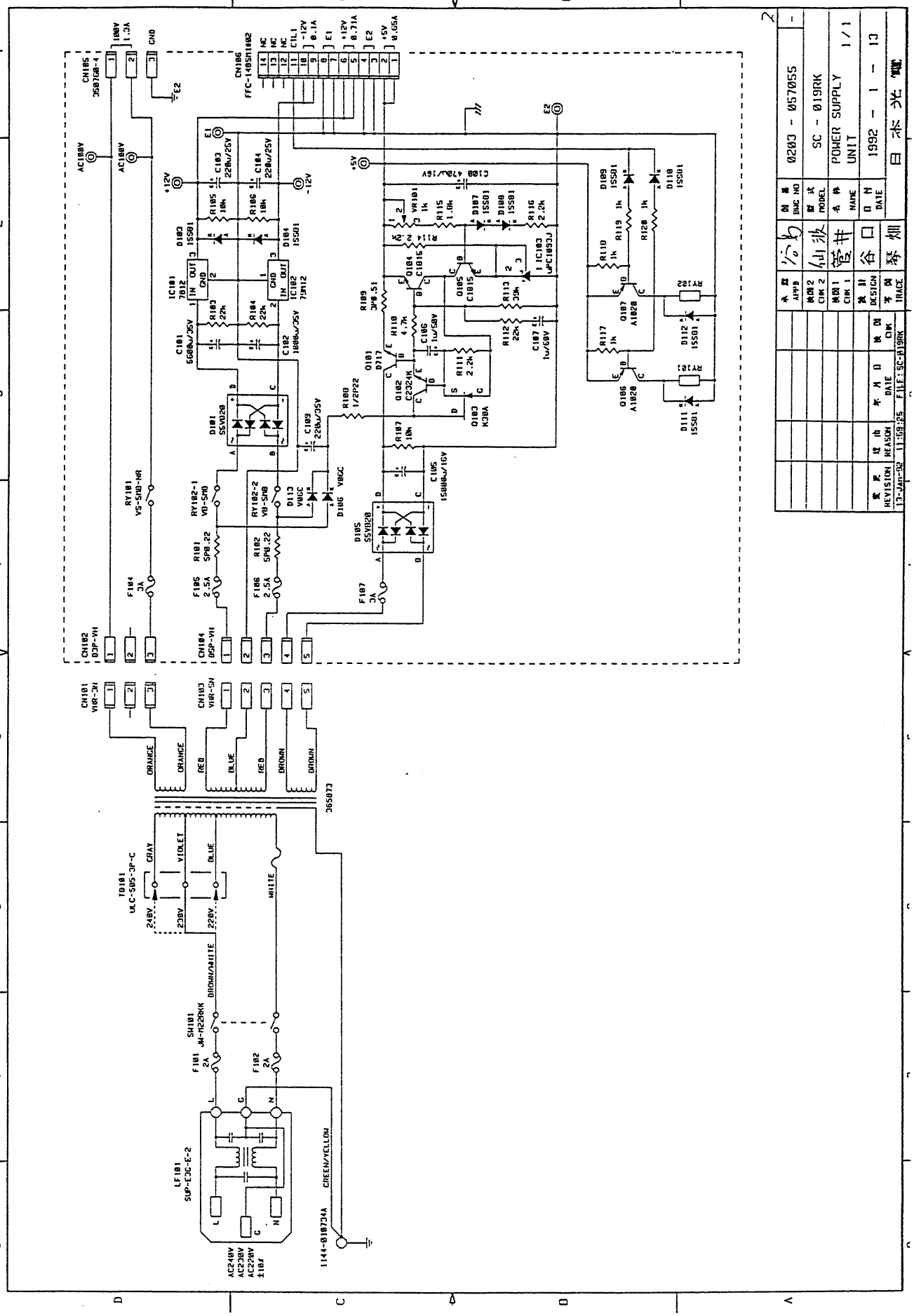
12. CIRCUIT DIAGRAM



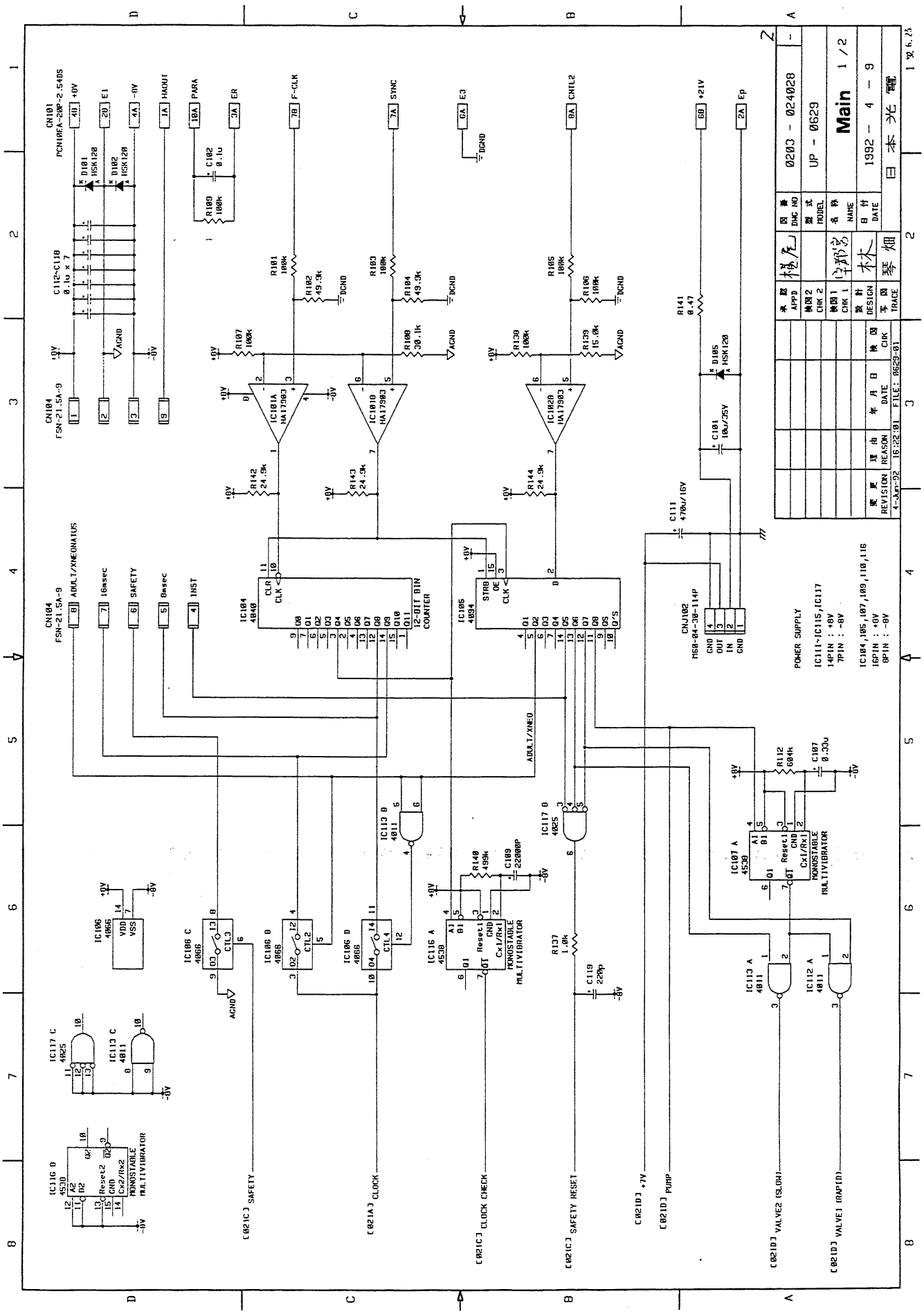
NO CONTENTS

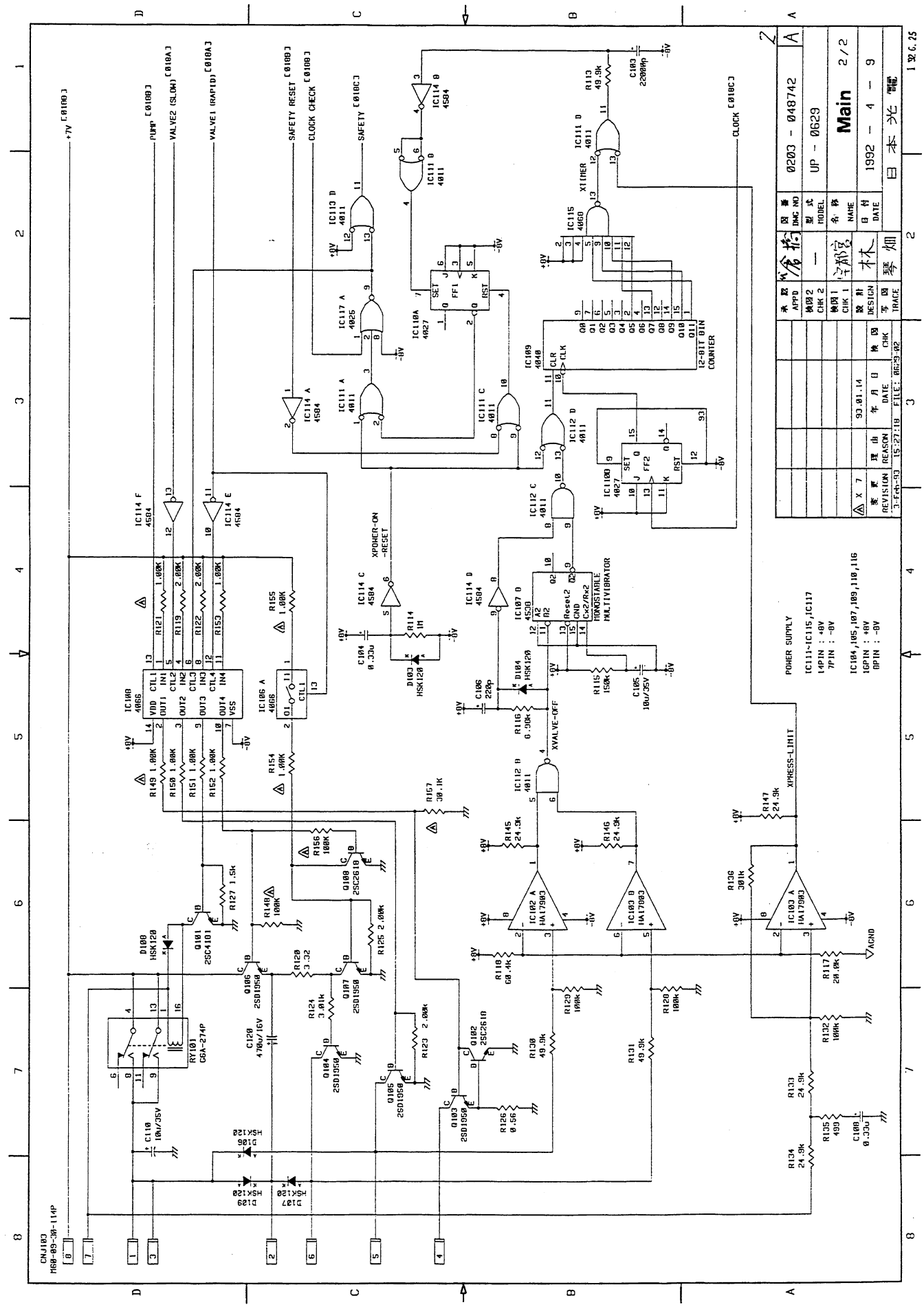
12. CIRCUIT DIAGRAM



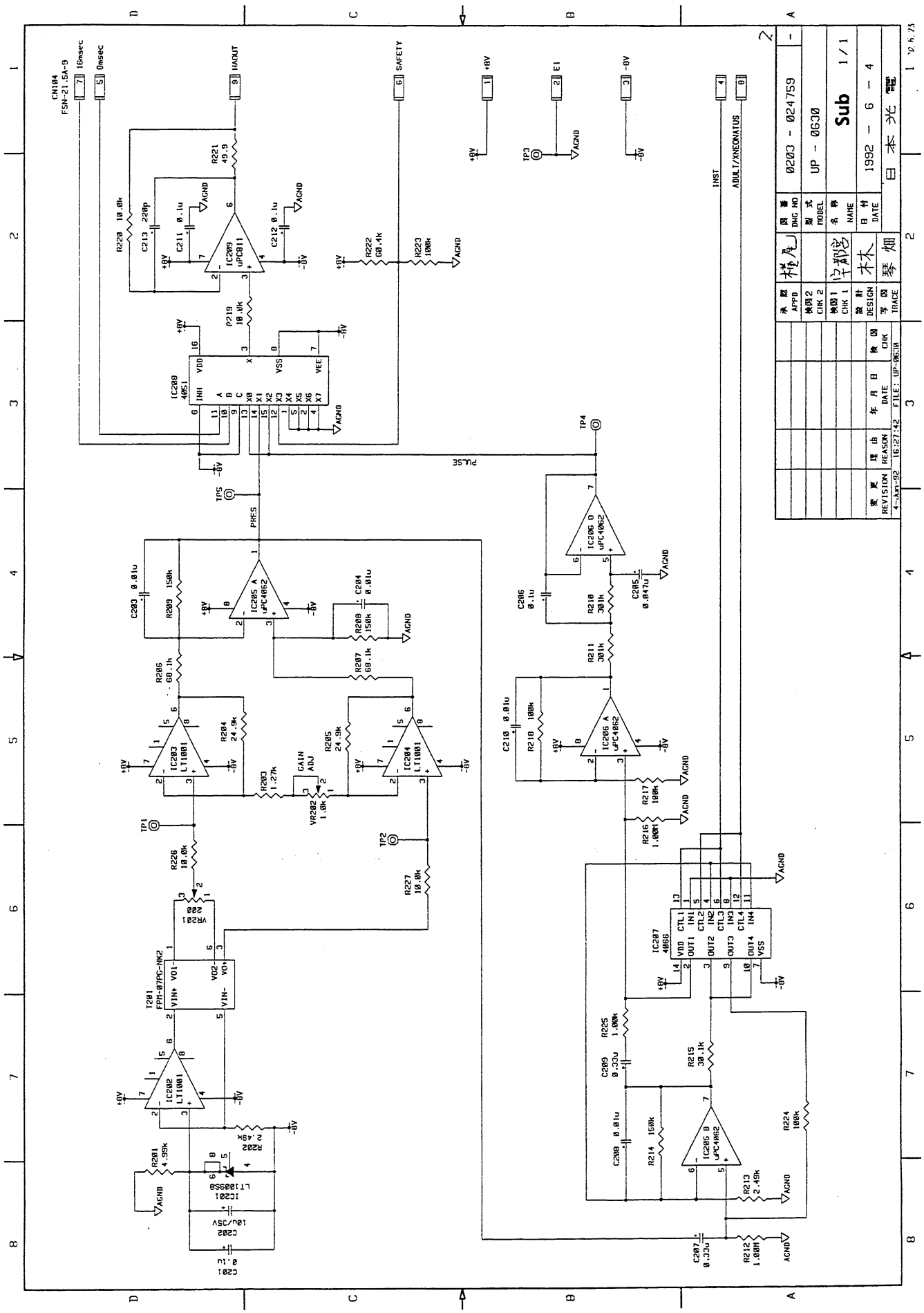

0203 - 057055
SC - 019RK
POWER SUPPLY UNIT
1 / 1
1992 - 1 - 13
日本光電
REVISION
13-Jan-92 11:59:25 FILE: SC-019RK

12. CIRCUIT DIAGRAM



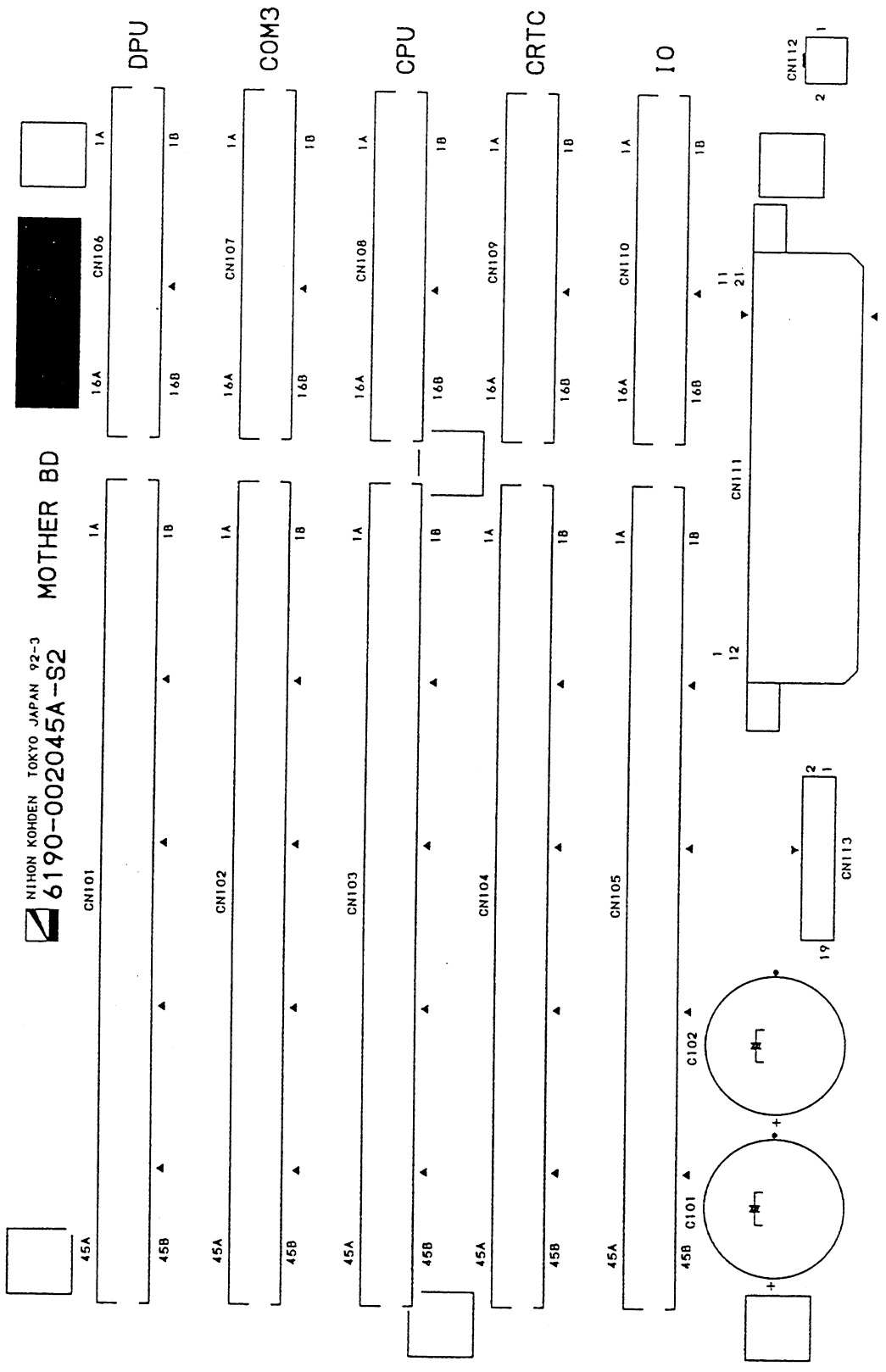

Main 2/2
0203 - 048742
UP - 0629
1992 - 4 - 9
日本光電
POWER SUPPLY
IC111~IC115,IC117
14PIN : +8V
7PIN : -8V
IC104,105,107,109,110,116
14PIN : +8V
7PIN : -8V
XPOWER-ON
-RESET
XVALVE-OFF
XPRESS-LIMIT
XTIMER
CLOCK
SAFETY RESET
CLOCK CHECK
SAFETY
PUMP
VALVE2 (SLOW)
VALVE1 (RAPID)
+7V
AGND
12-BIT BIN COUNTER
MONOSTABLE MULTIVIBRATOR
CNJ103
M68-09-30-114P

12. CIRCUIT DIAGRAM

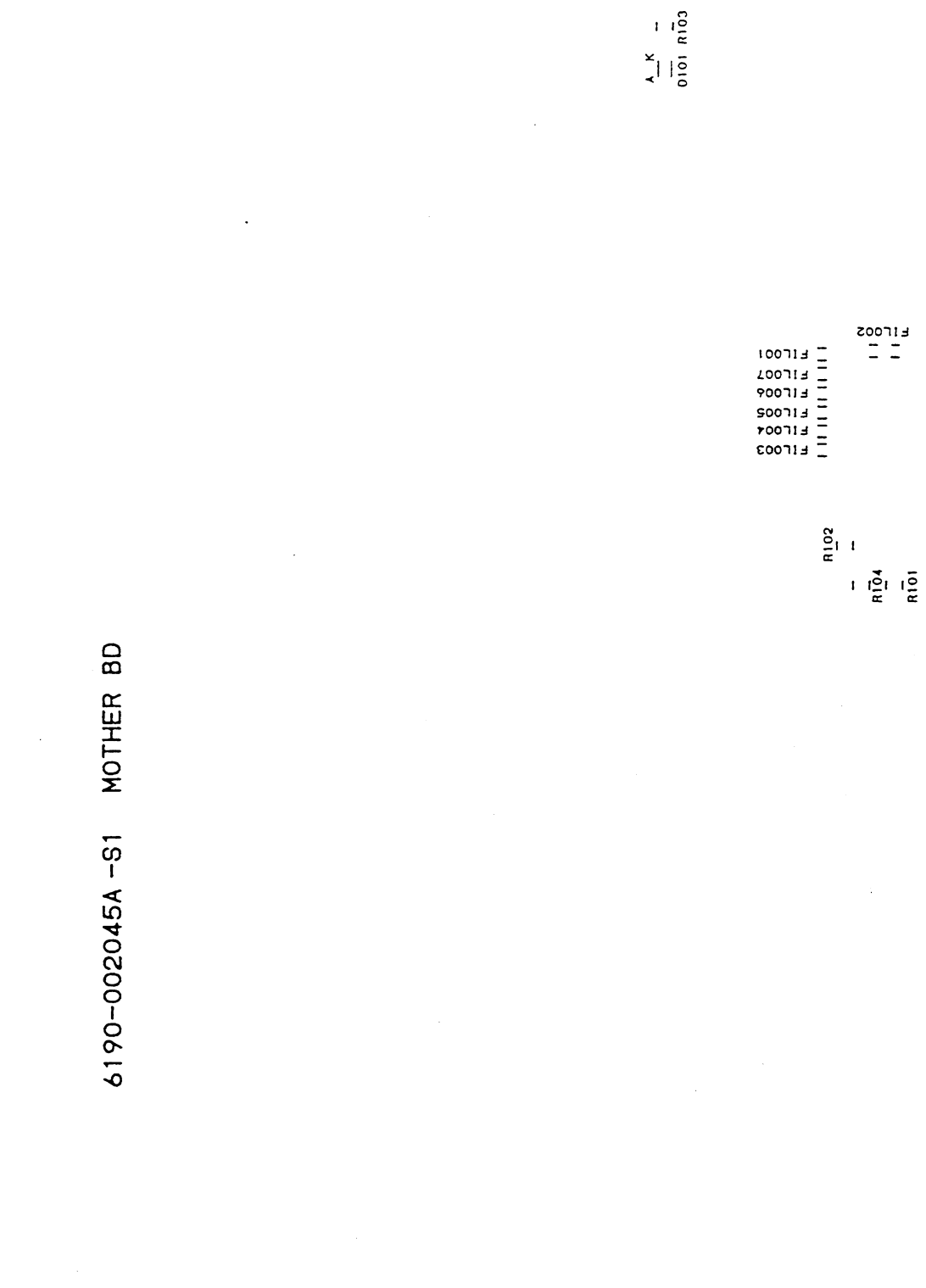


Section 13 PARTS LOCATION GUIDE

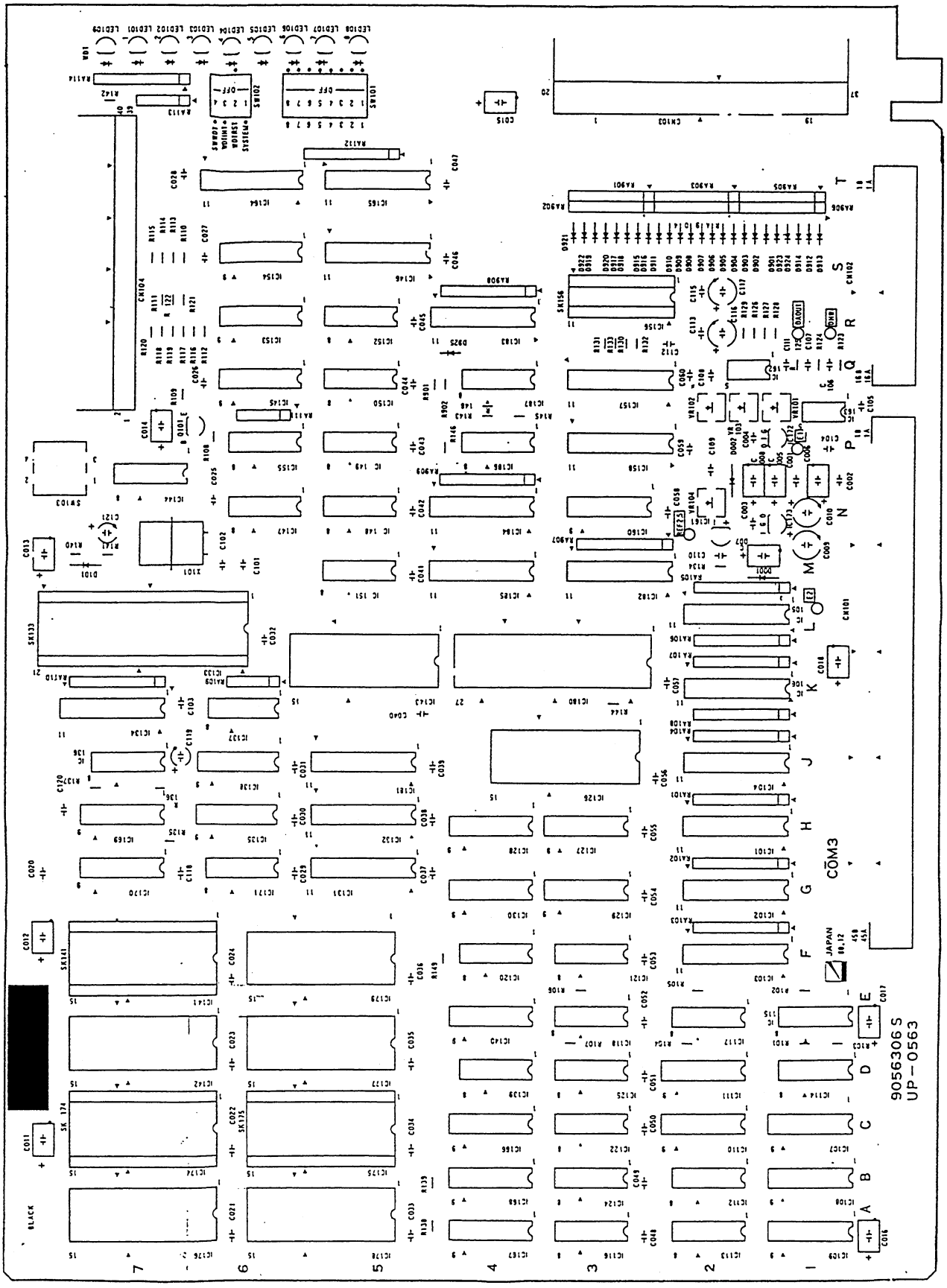
MOTHER Board, UP0798 (FRONT)



MOTHER Board, UP0798 (REAR)

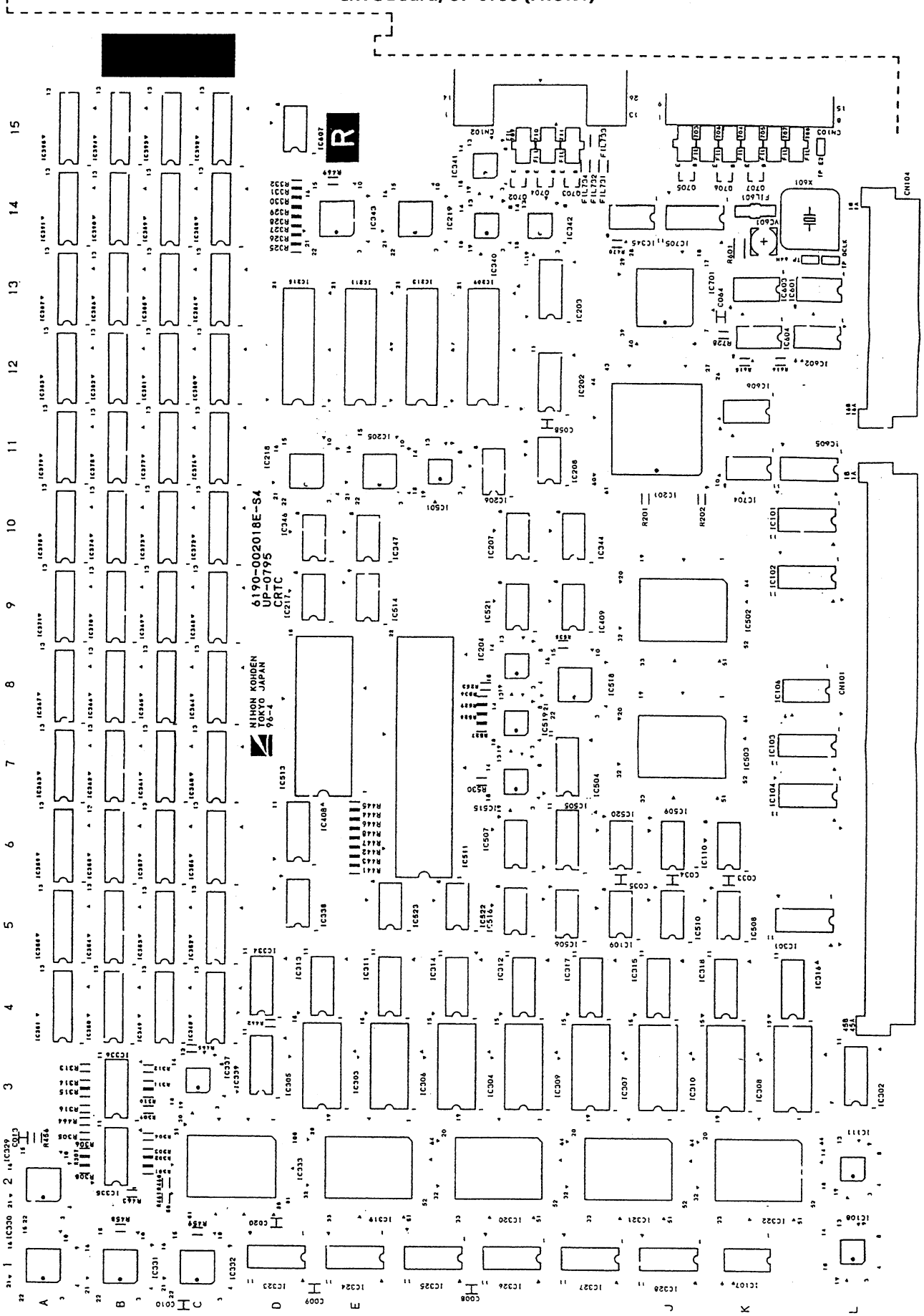


COM3 Board, UP-0563

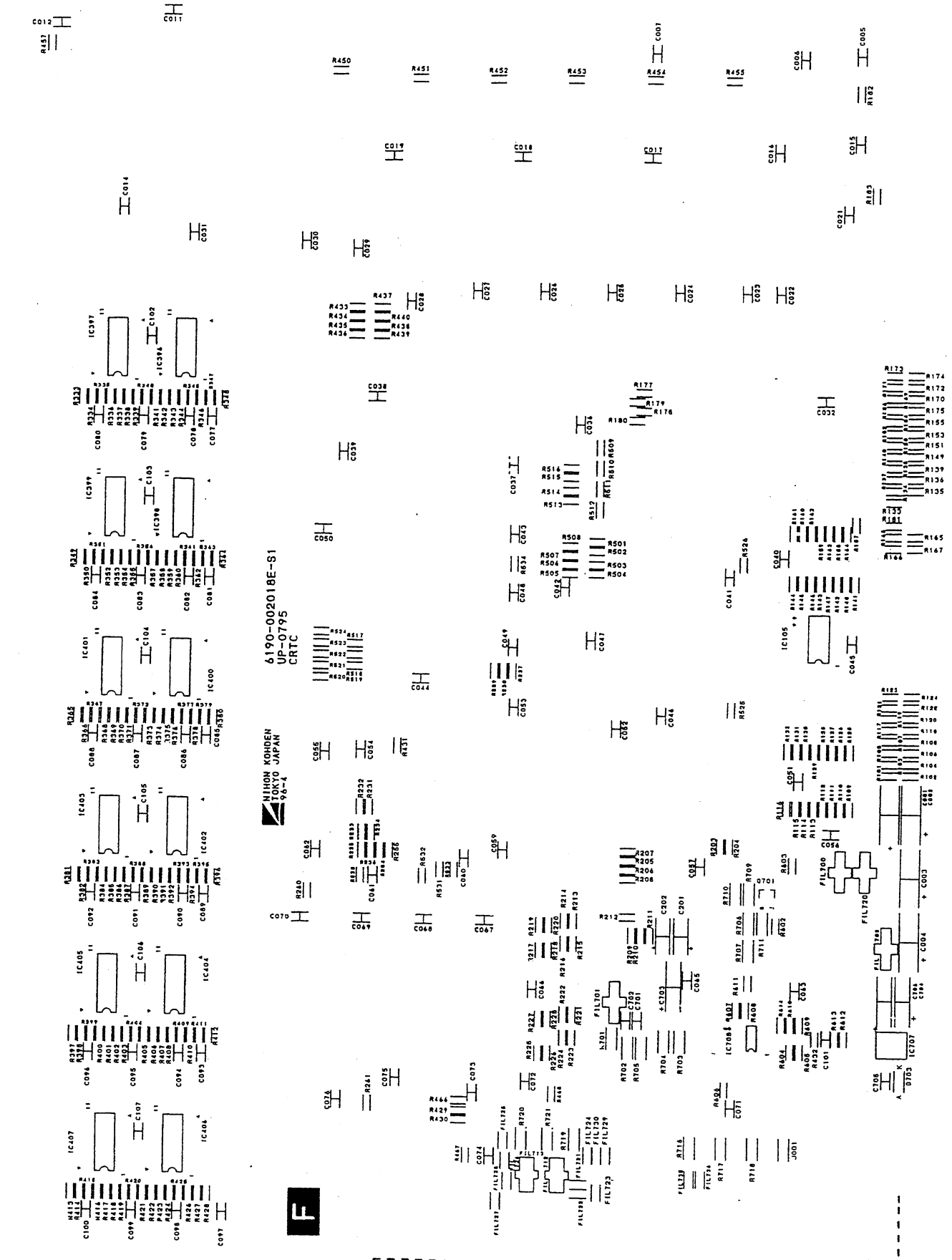


13. PARTS LOCATION GUIDE

CRTC Board, UP-0795 (FRONT)

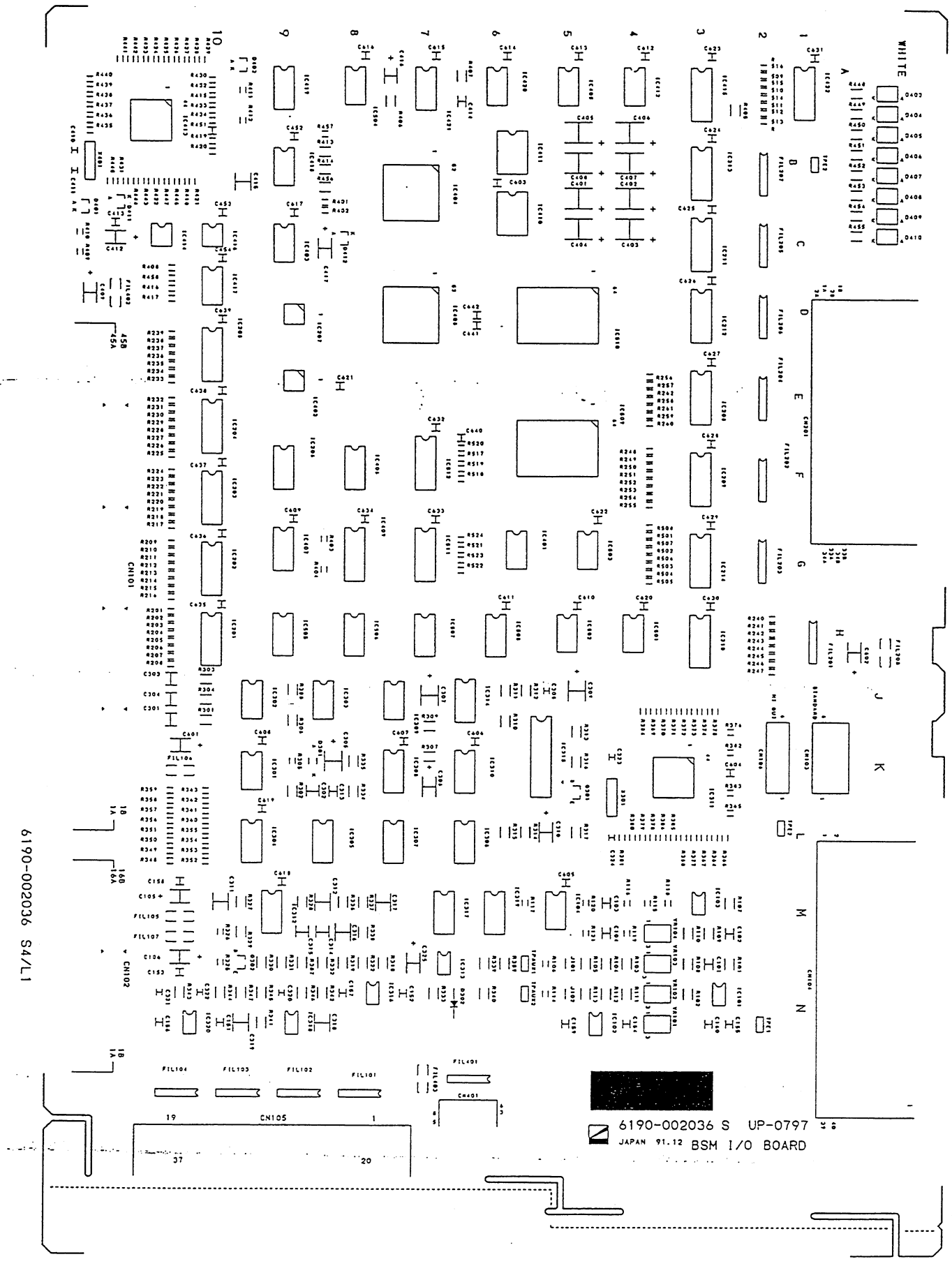


CRTC Board, UP-0795 (REAR)

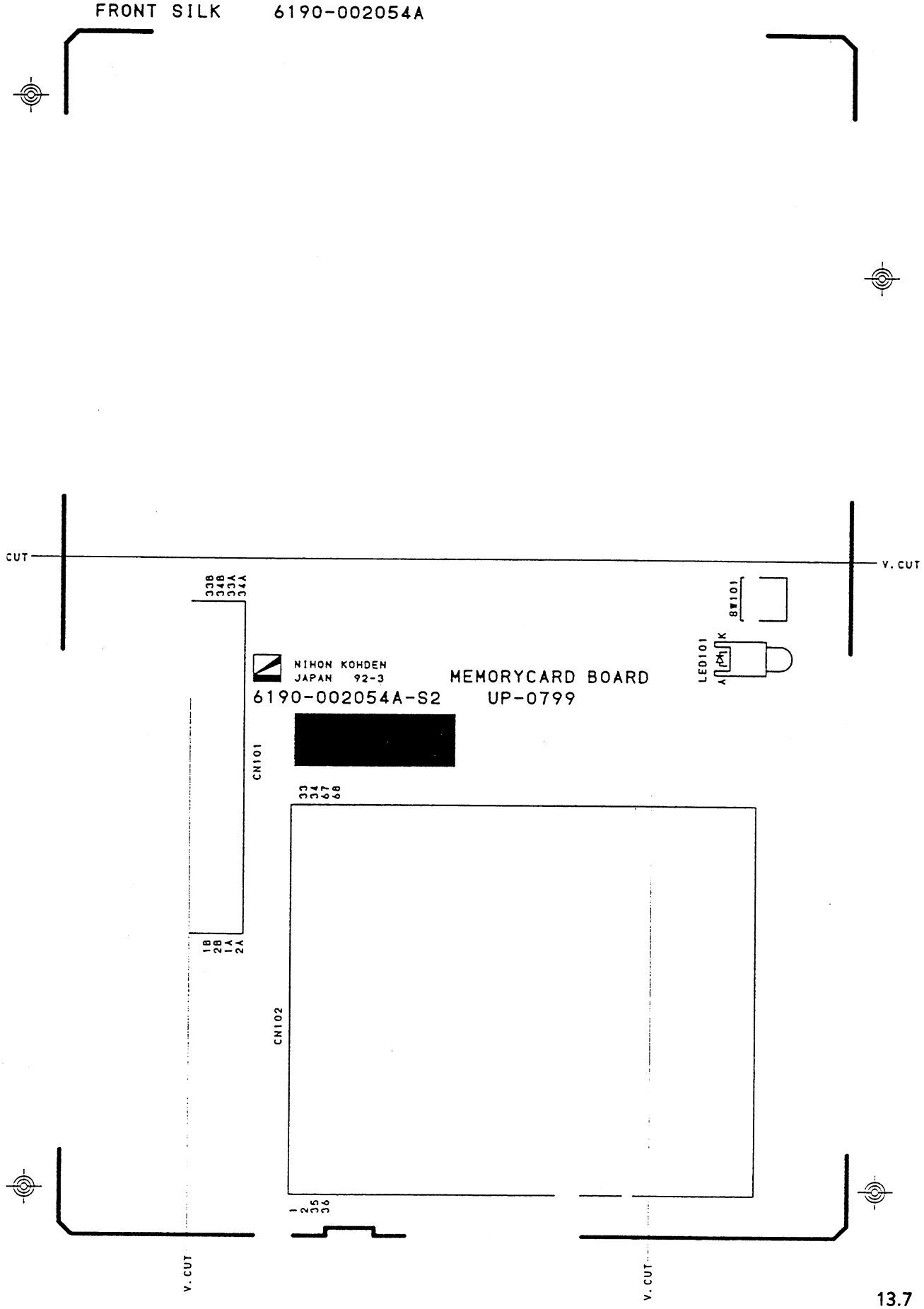


13. PARTS LOCATION GUIDE

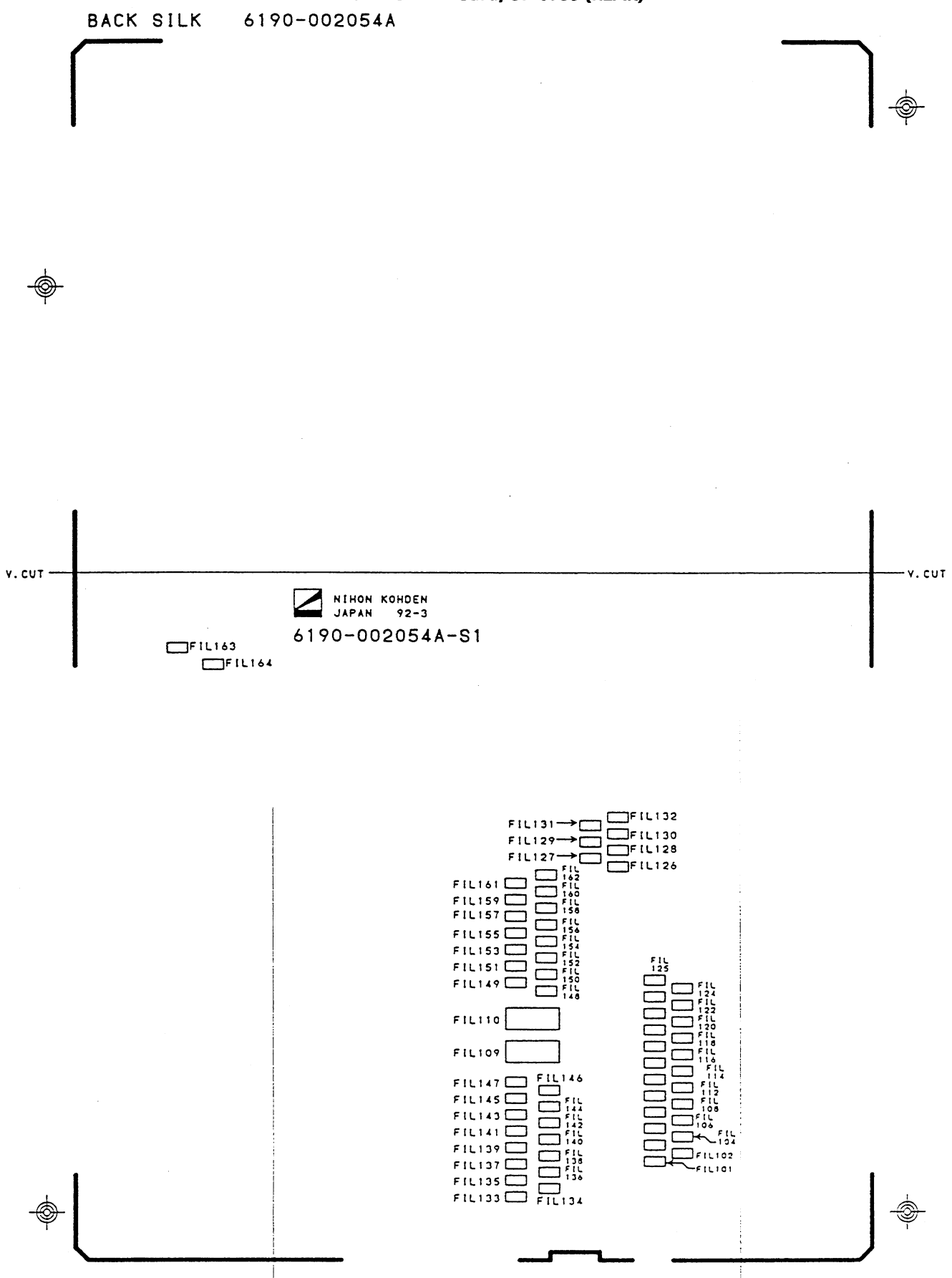
I/O Board, UP-0797



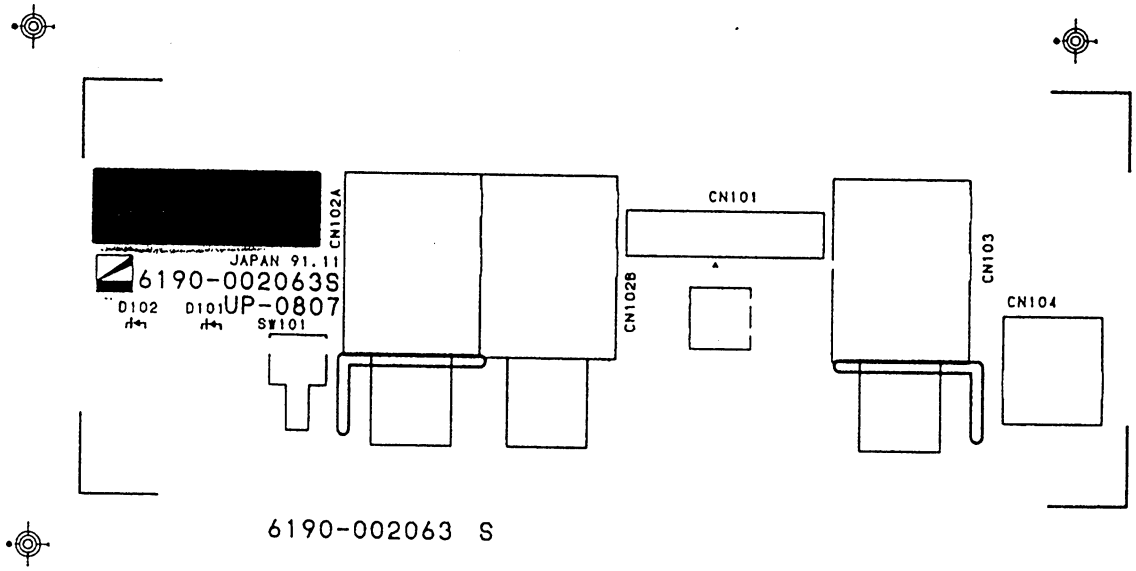
MEMORY CARD Board, UP-0799 (FRONT)



MEMORY CARD Board, UP-0799 (REAR)

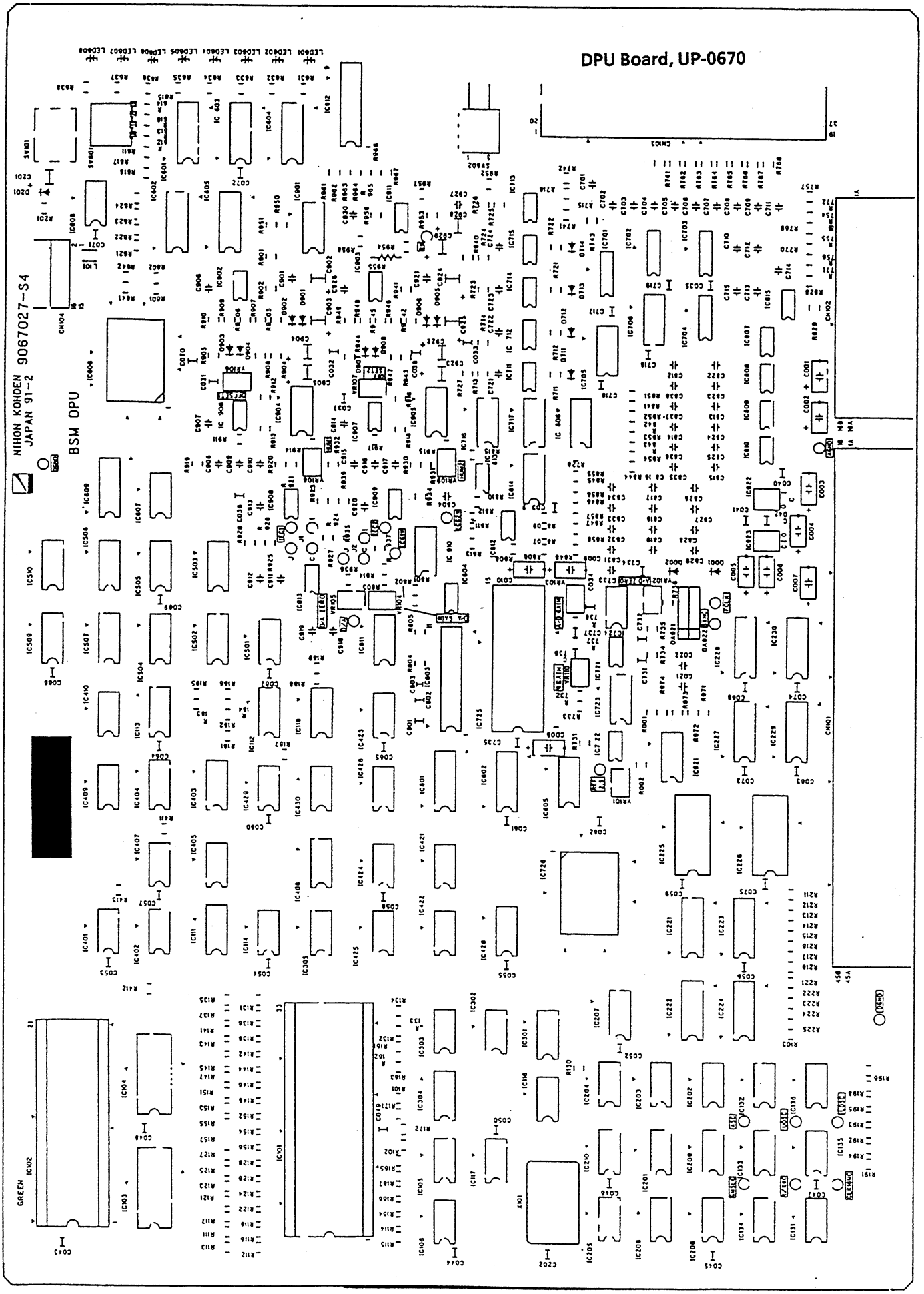


FRONT CONNECTOR Board, UP-0807

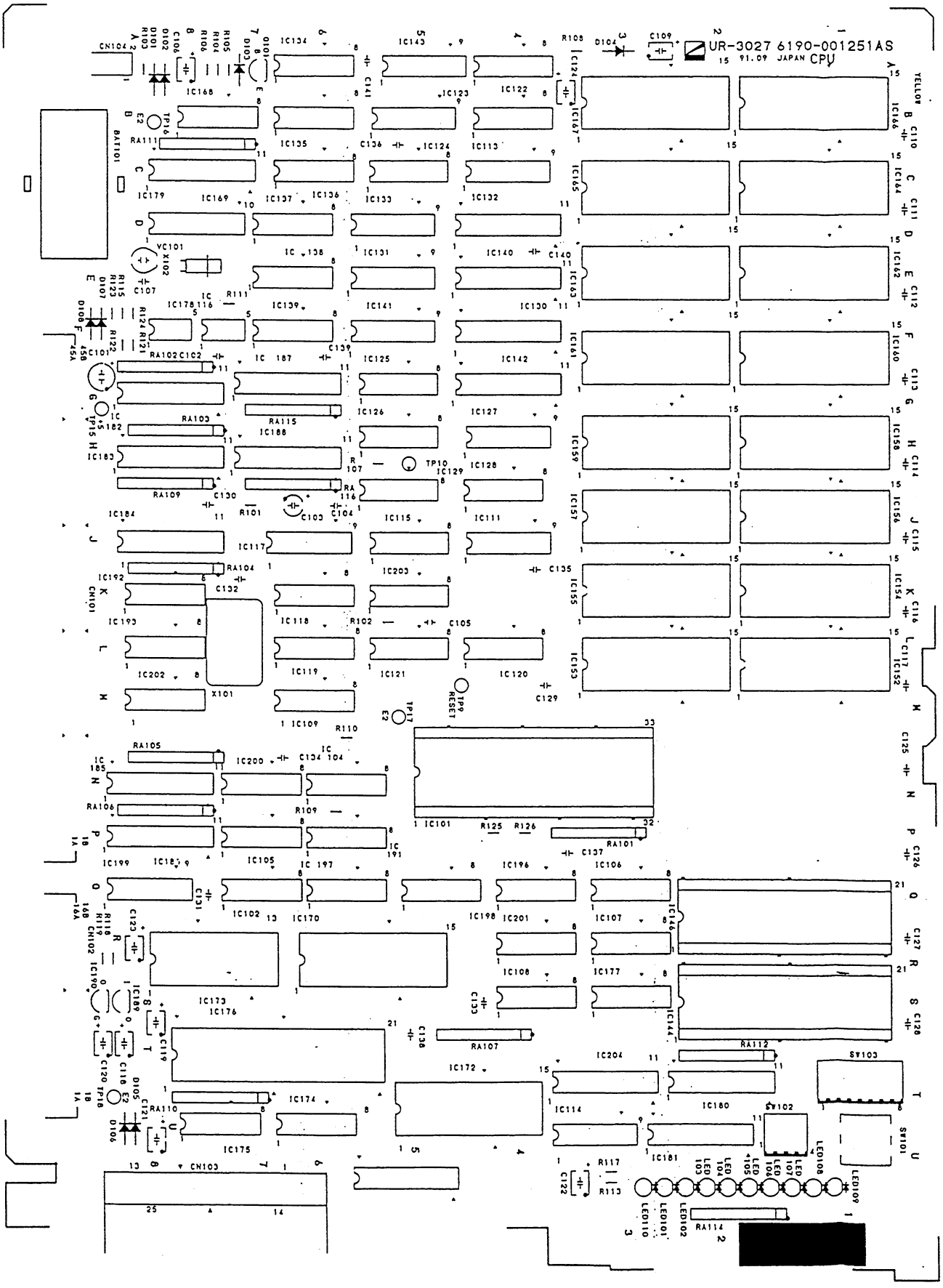


6190-002063 S

13. PARTS LOCATION GUIDE

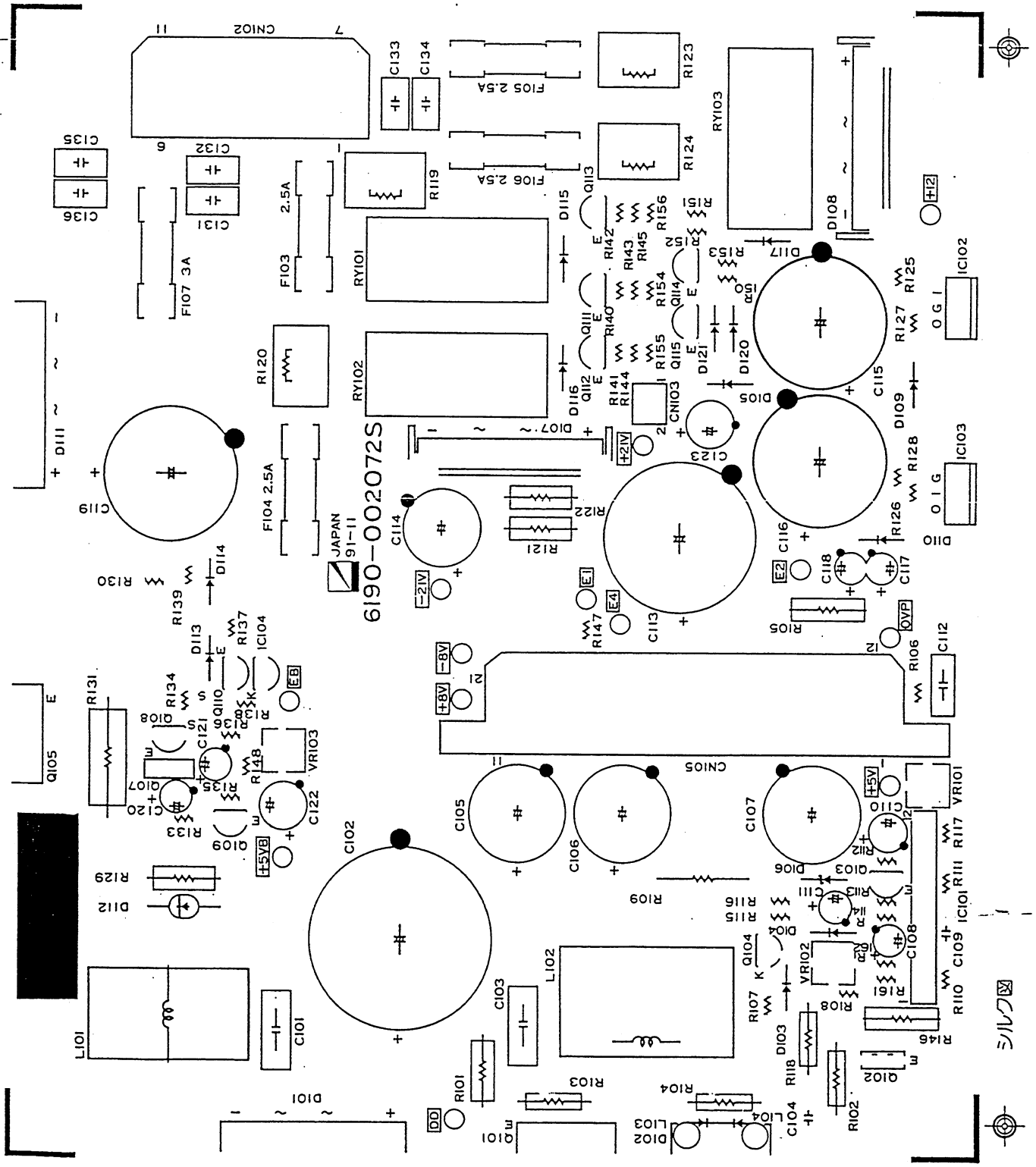


CPU Board, UR-3027

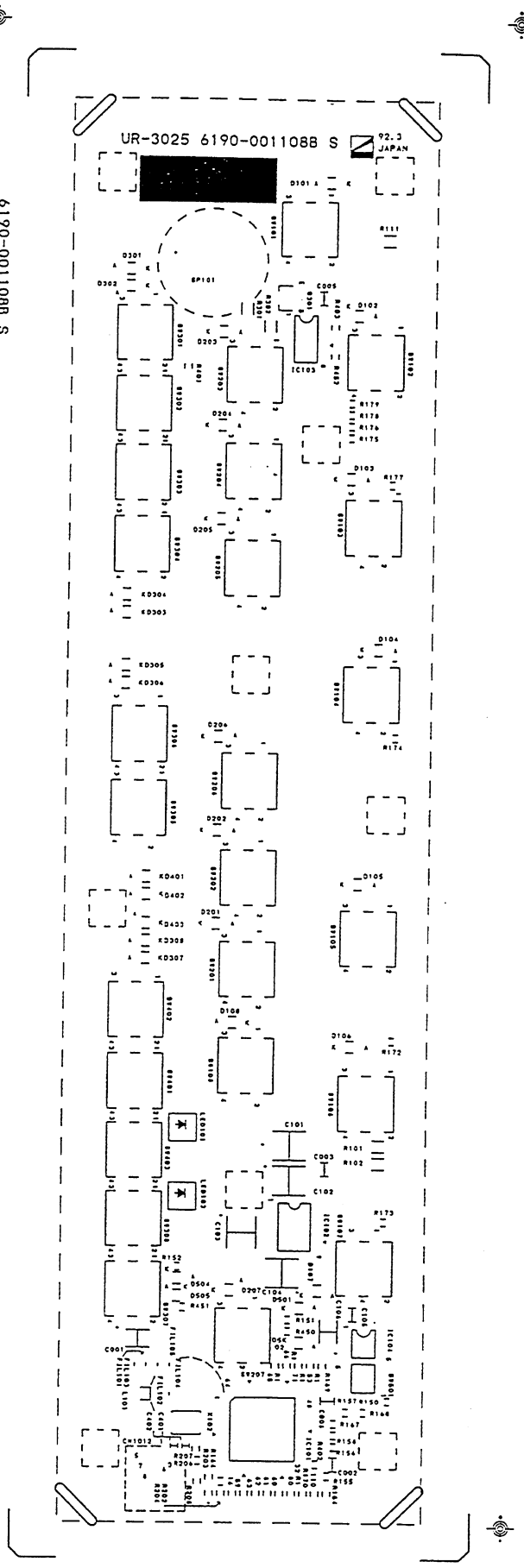


13. PARTS LOCATION GUIDE

Regulator Board, UP-0813

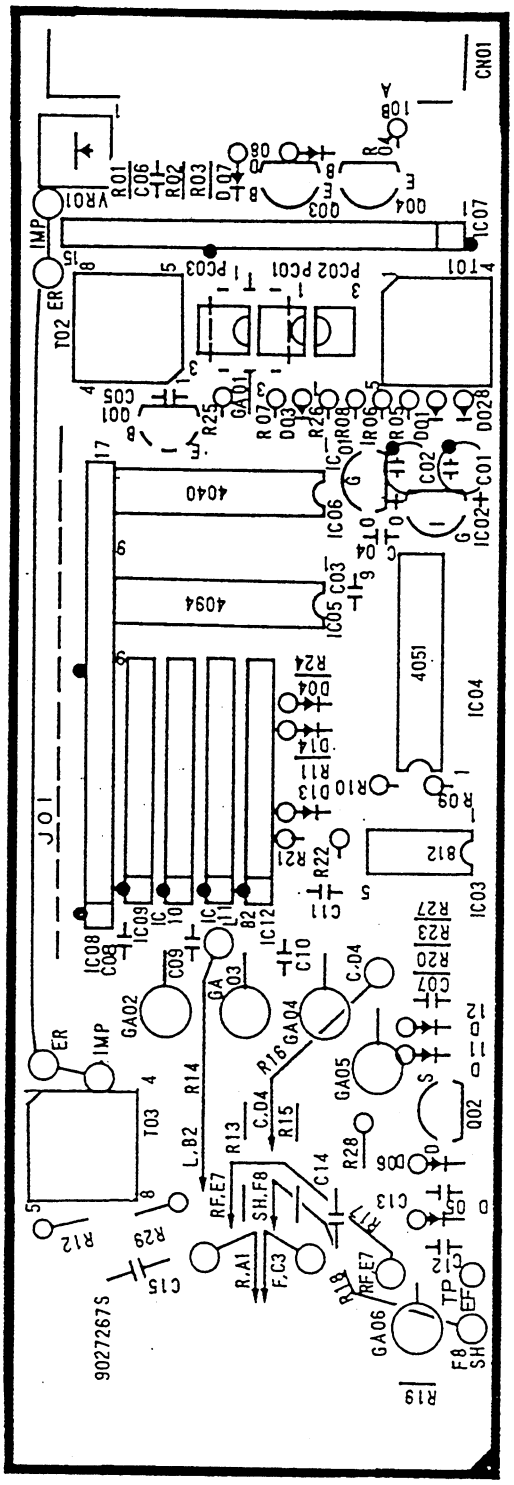


OPERATION Board, UR-3025

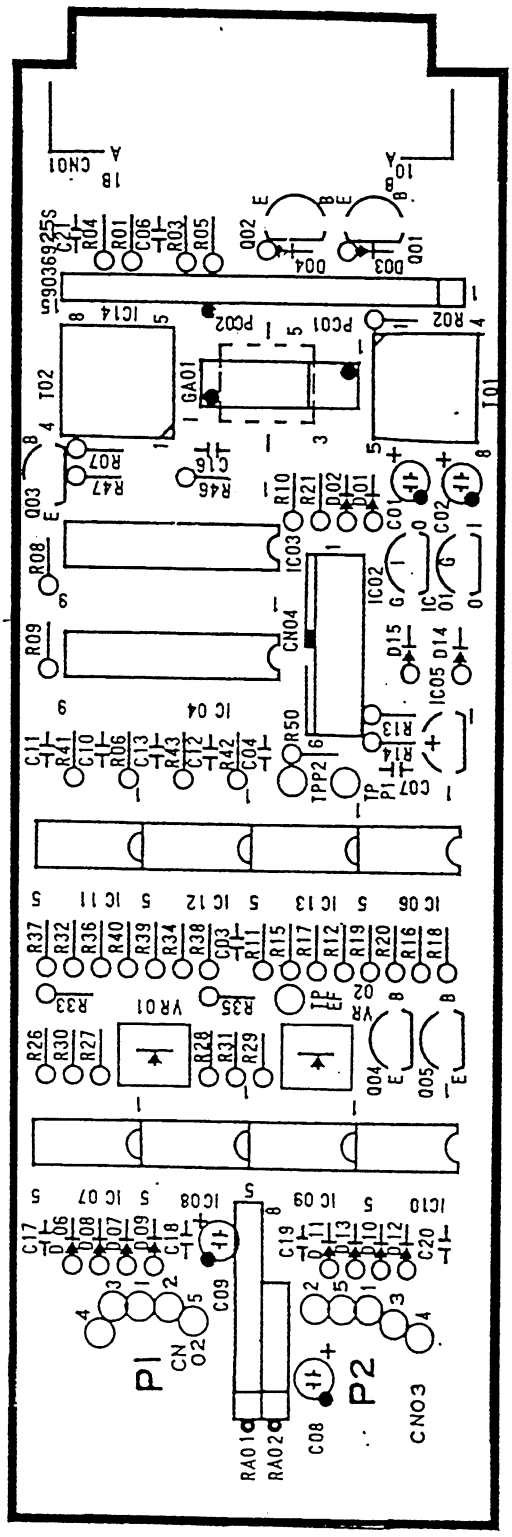


13. PARTS LOCATION GUIDE

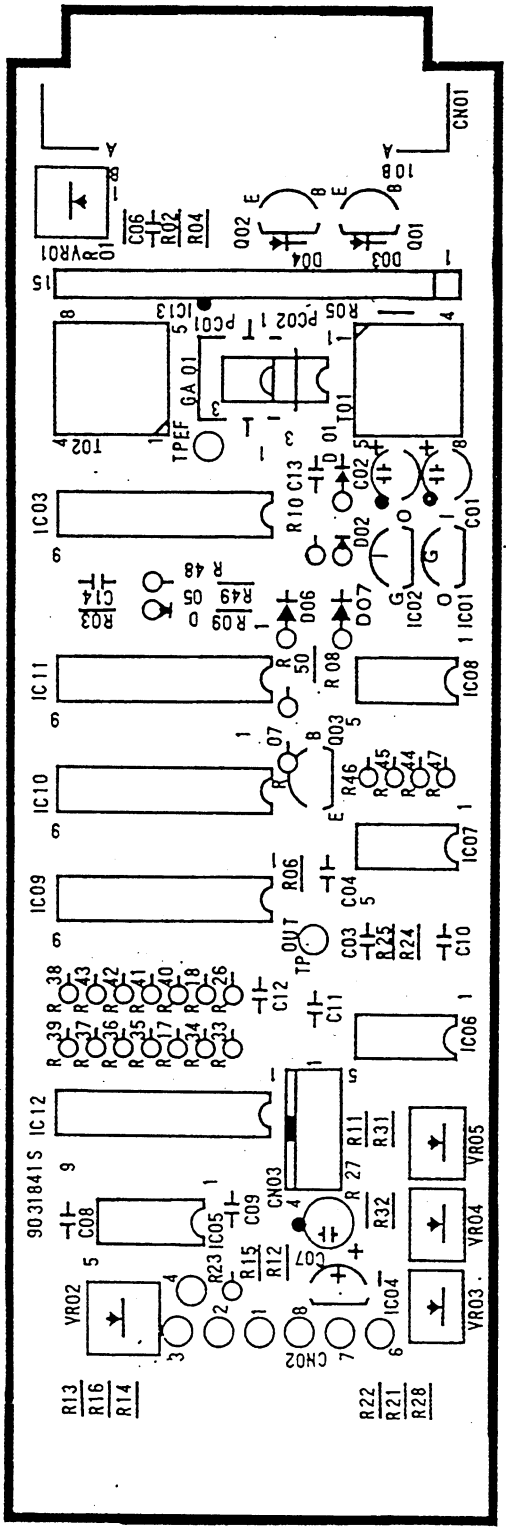
ECG Head Amp (AC-800P) Board, UP-0272



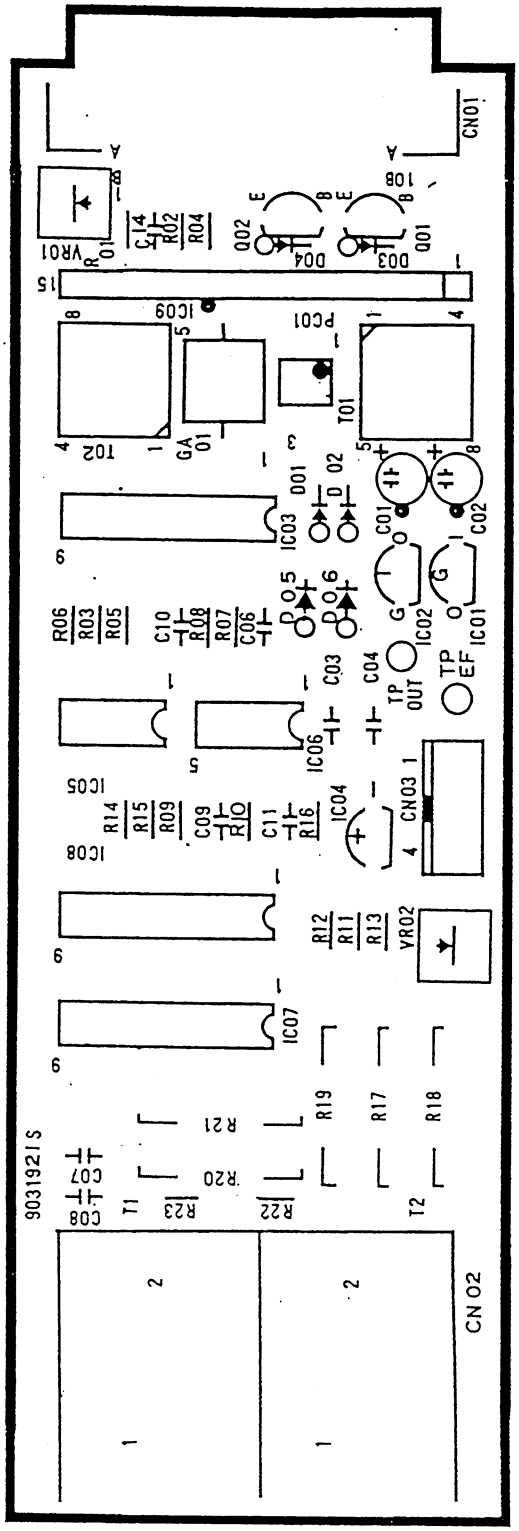
PRESS Head Amp (AP-800PA) Board, UP-0369



CO Head Amp (AH-800PA) Board, UP-0318

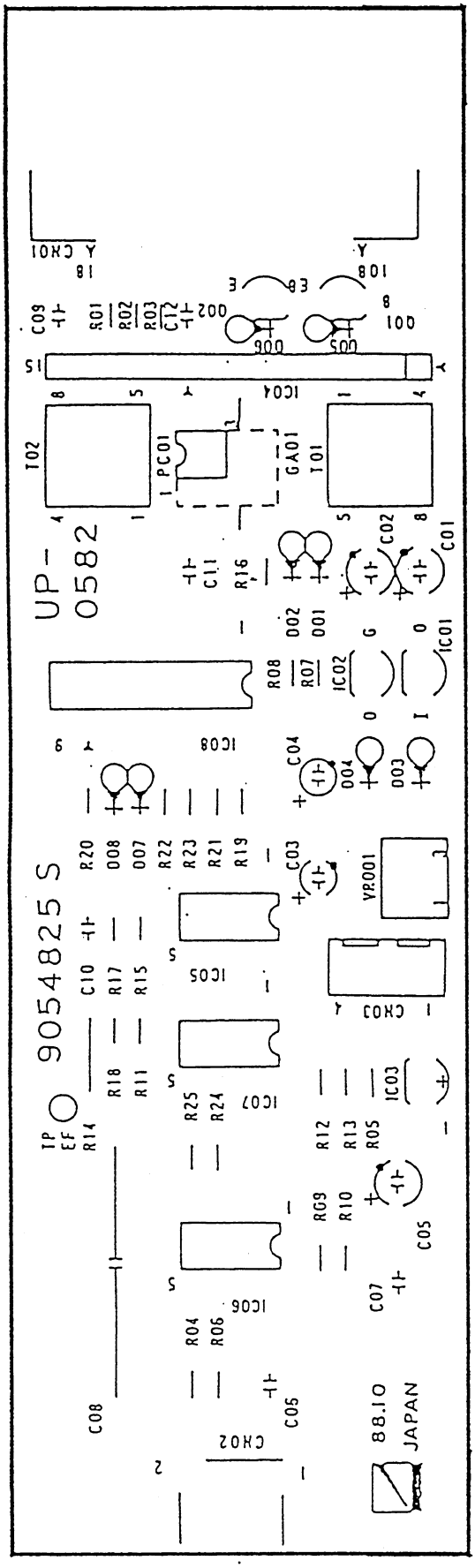


TEMP Head Amp (AW-800PA) Board, UP-0319

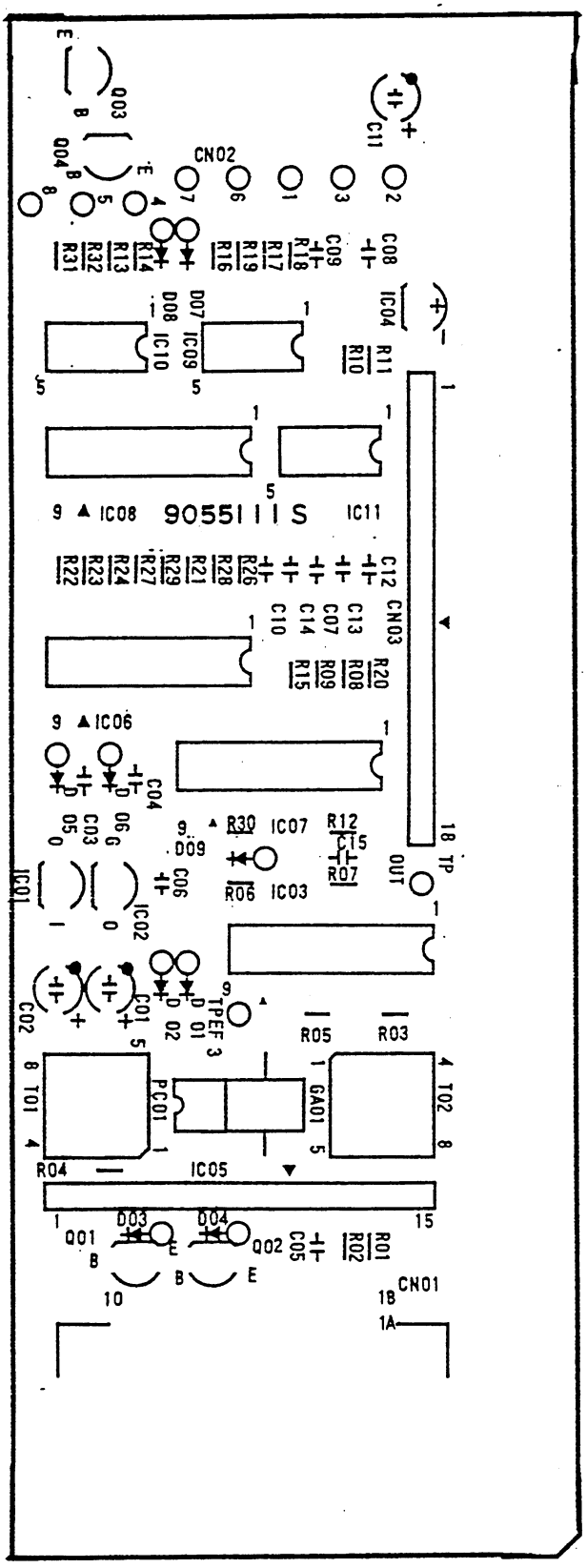


13. PARTS LOCATION GUIDE

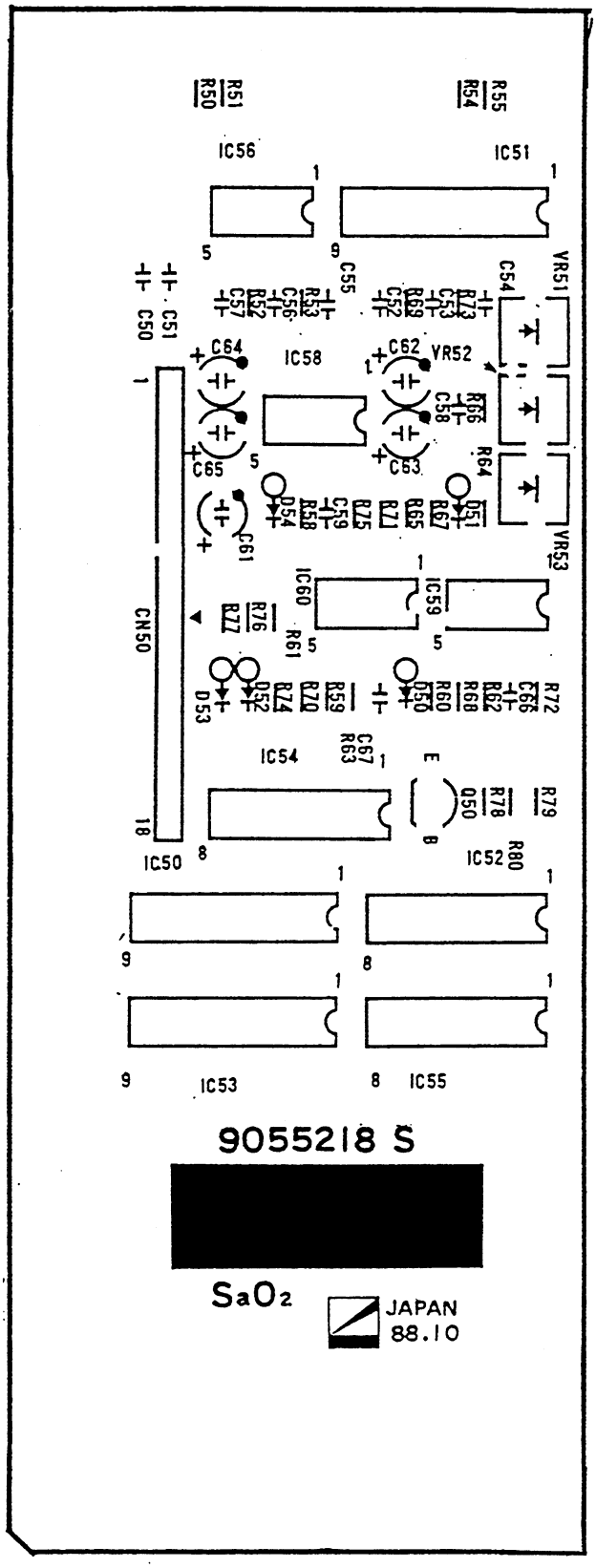
RESPIRATION Head Amp (AR-800PA) Board, UP-0548



SpO_2 Head Amp (AL-800PA) Main Board, UP-0551

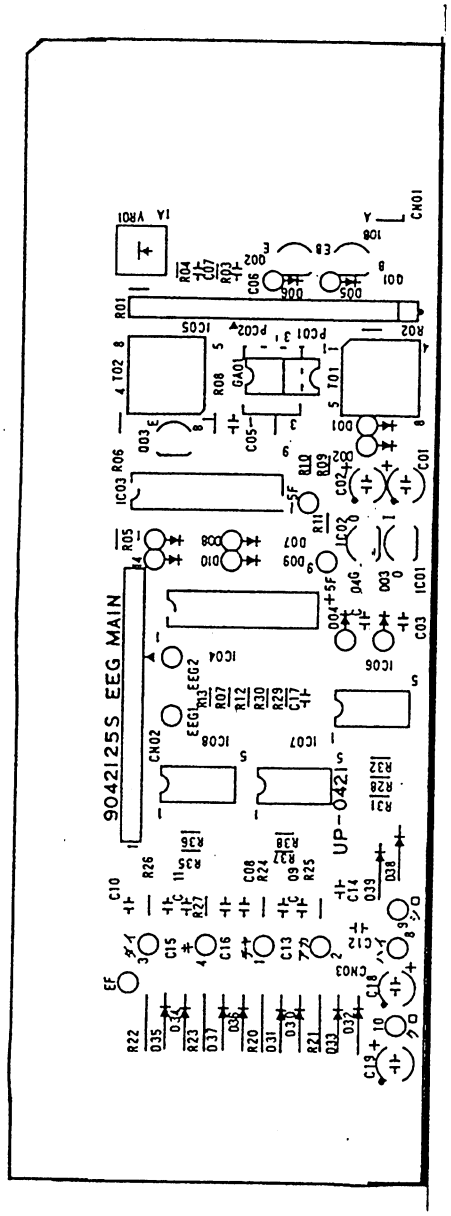


SpO_2 Head Amp (AL-800PA) Sub Board, UP-0552

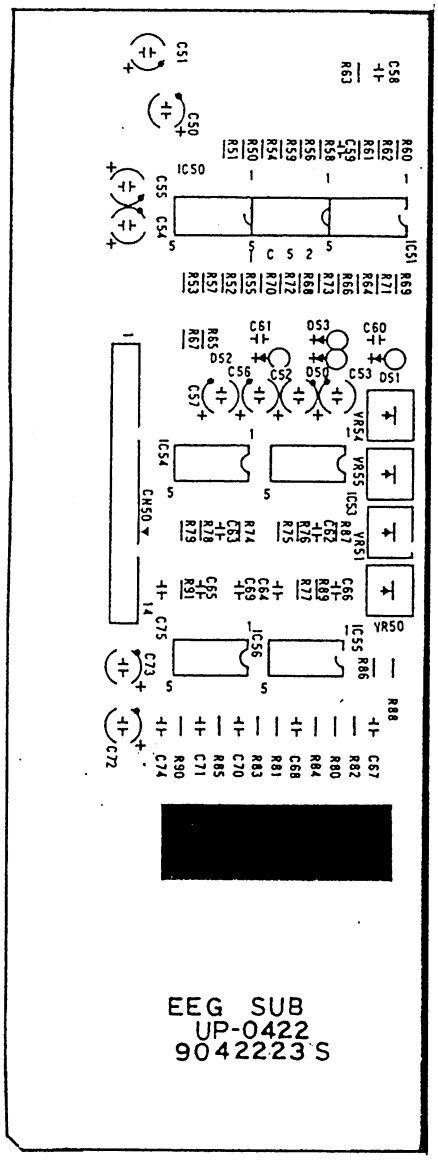


13. PARTS LOCATION GUIDE

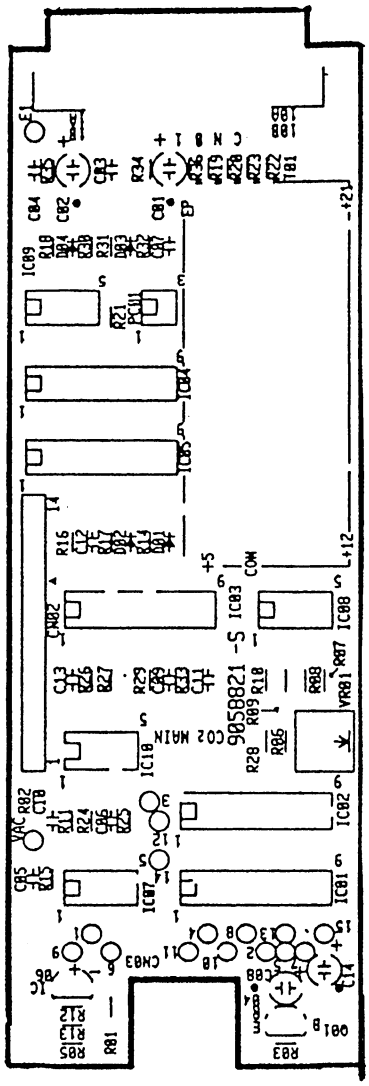
EEG Head Amp (AE-800PA) Main Board, UP0421



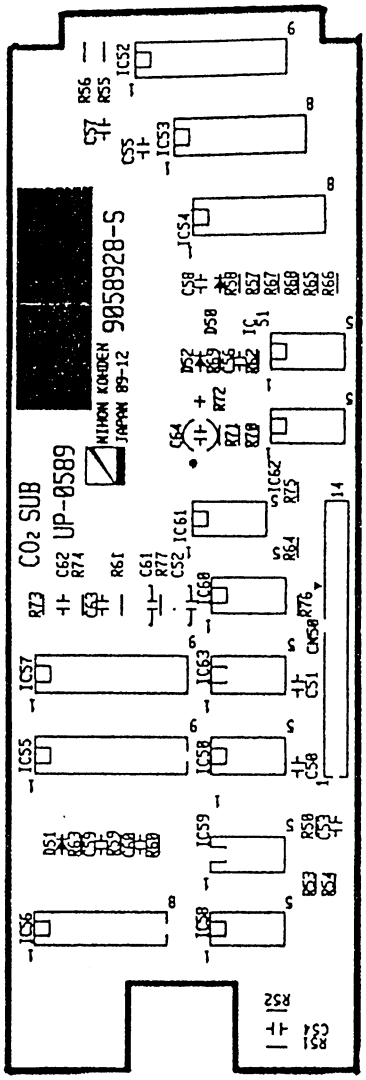
EEG Head Amp (AE-800PA) Sub Board, UP0422



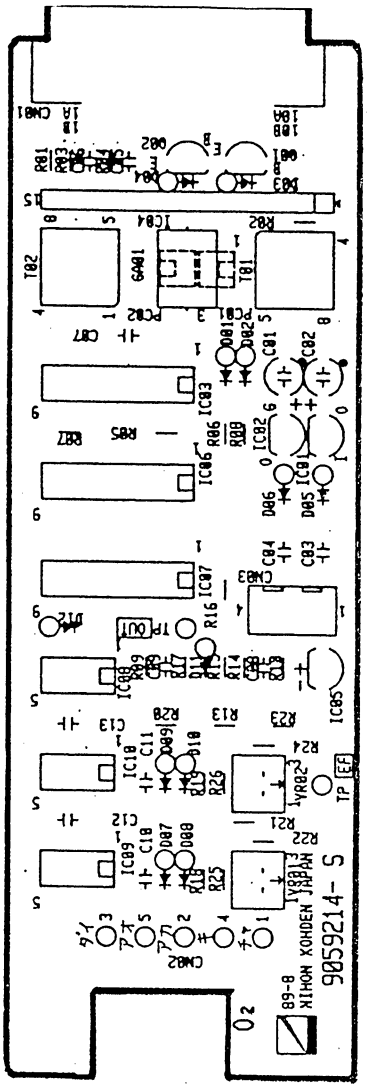
CO_2 Head Amp (AG-800PA) Main Board, UP-0588



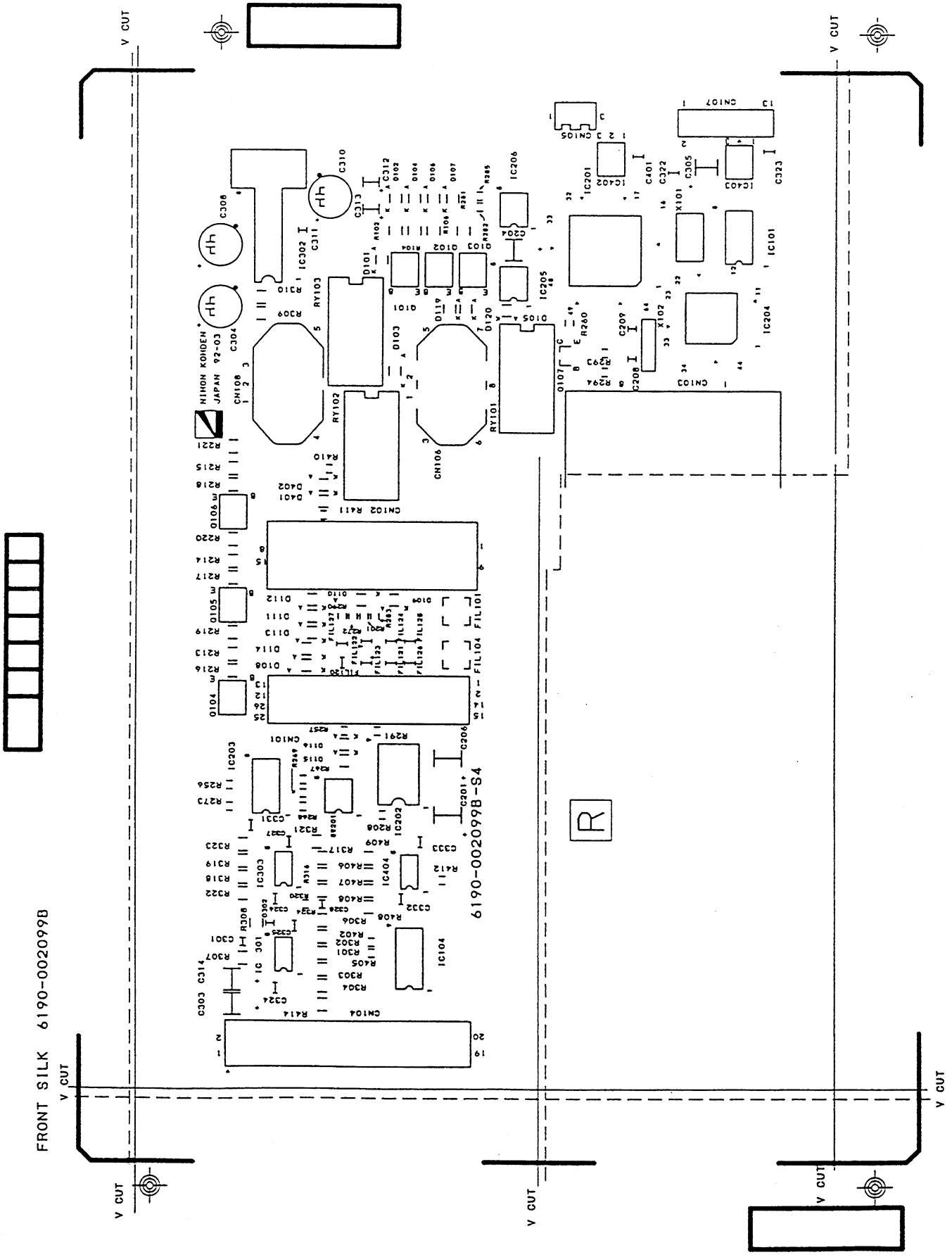
CO_2 Head Amp (AG-800PA) Sub Board, UP-0589



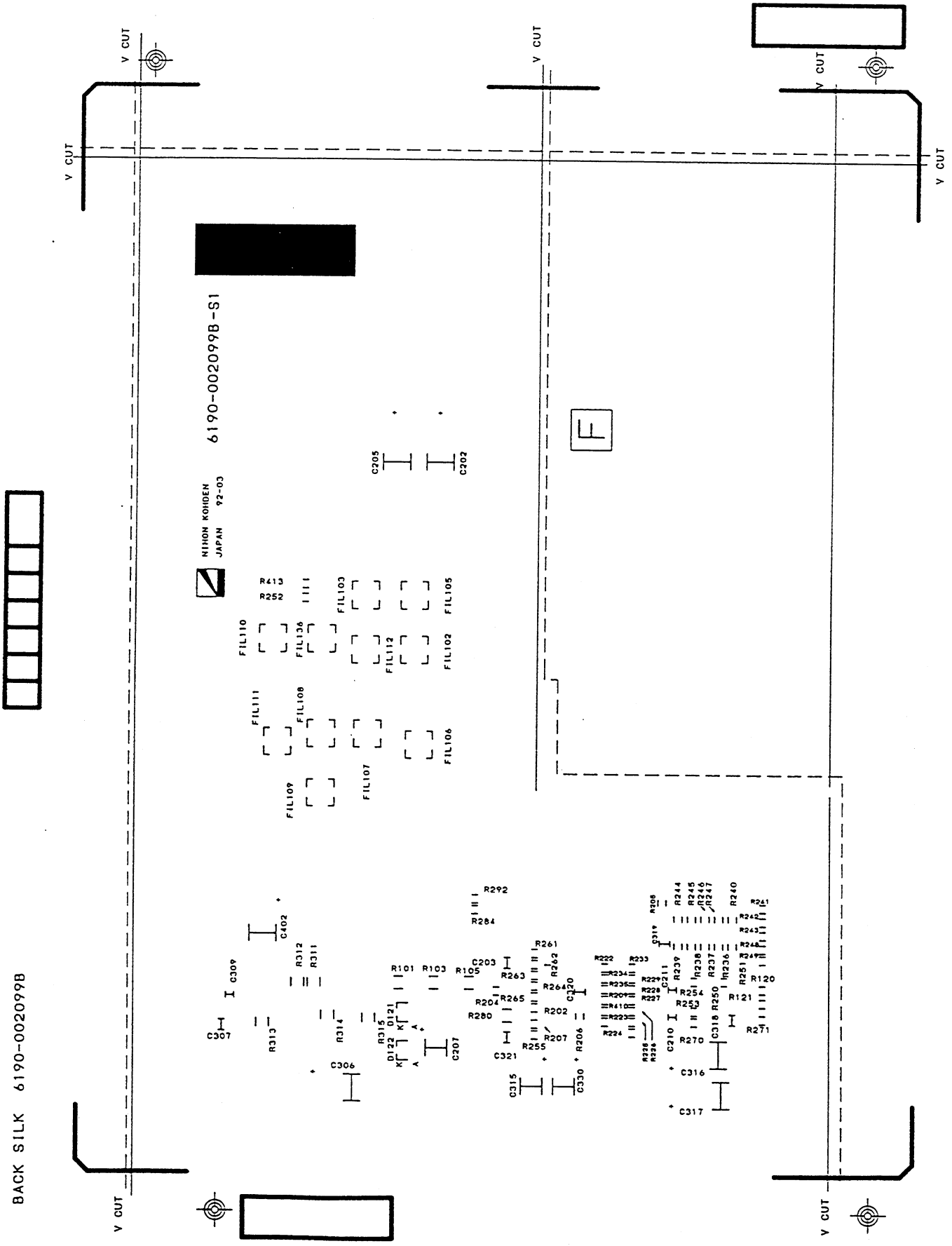
O_2 Head Amp (AG-820PA) Board, UP-0592



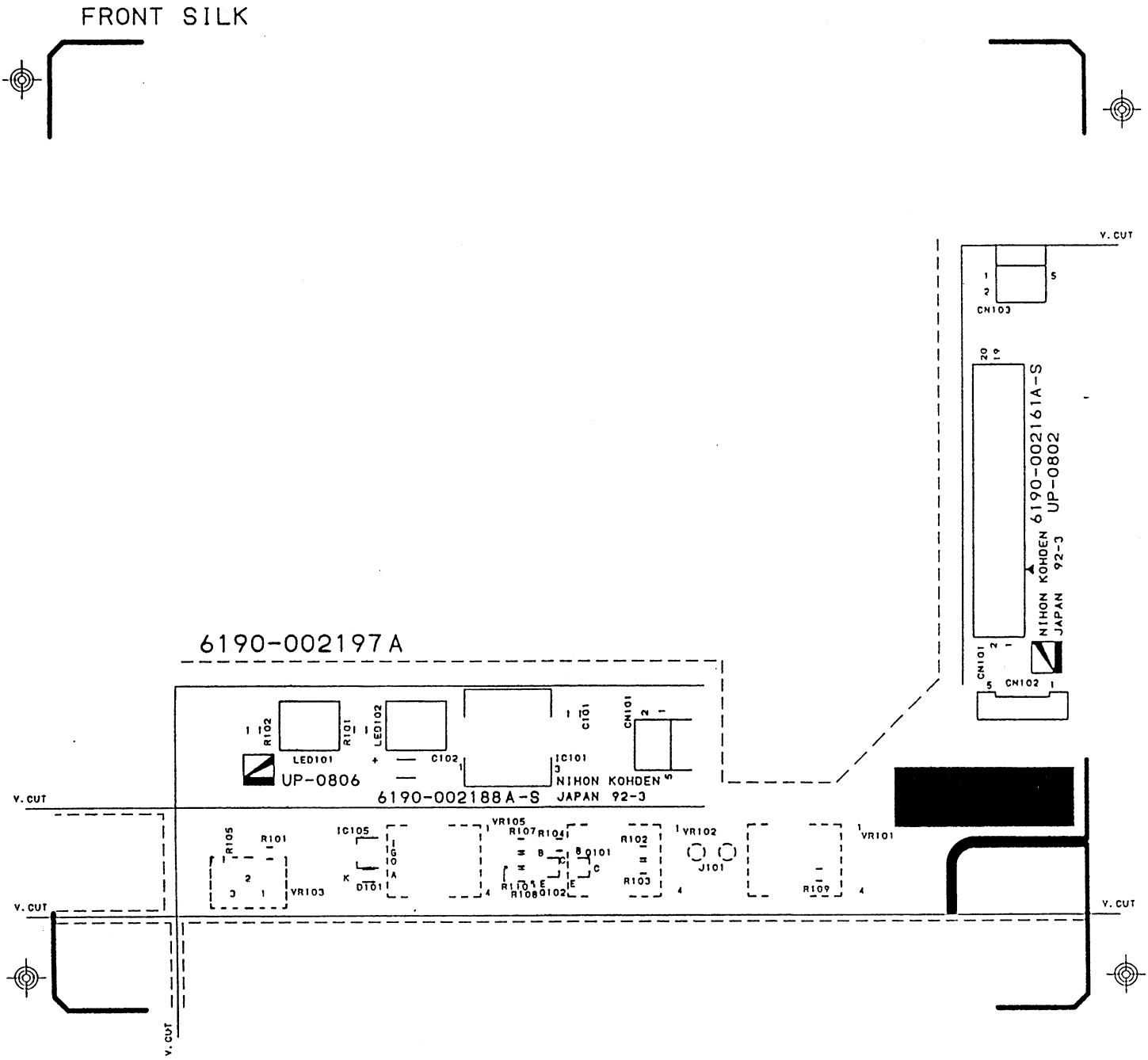
OPERATION CONTROL Board, UP-0801 (FRONT)



OPERATION CONTROL Board, UP-0801 (BACK)

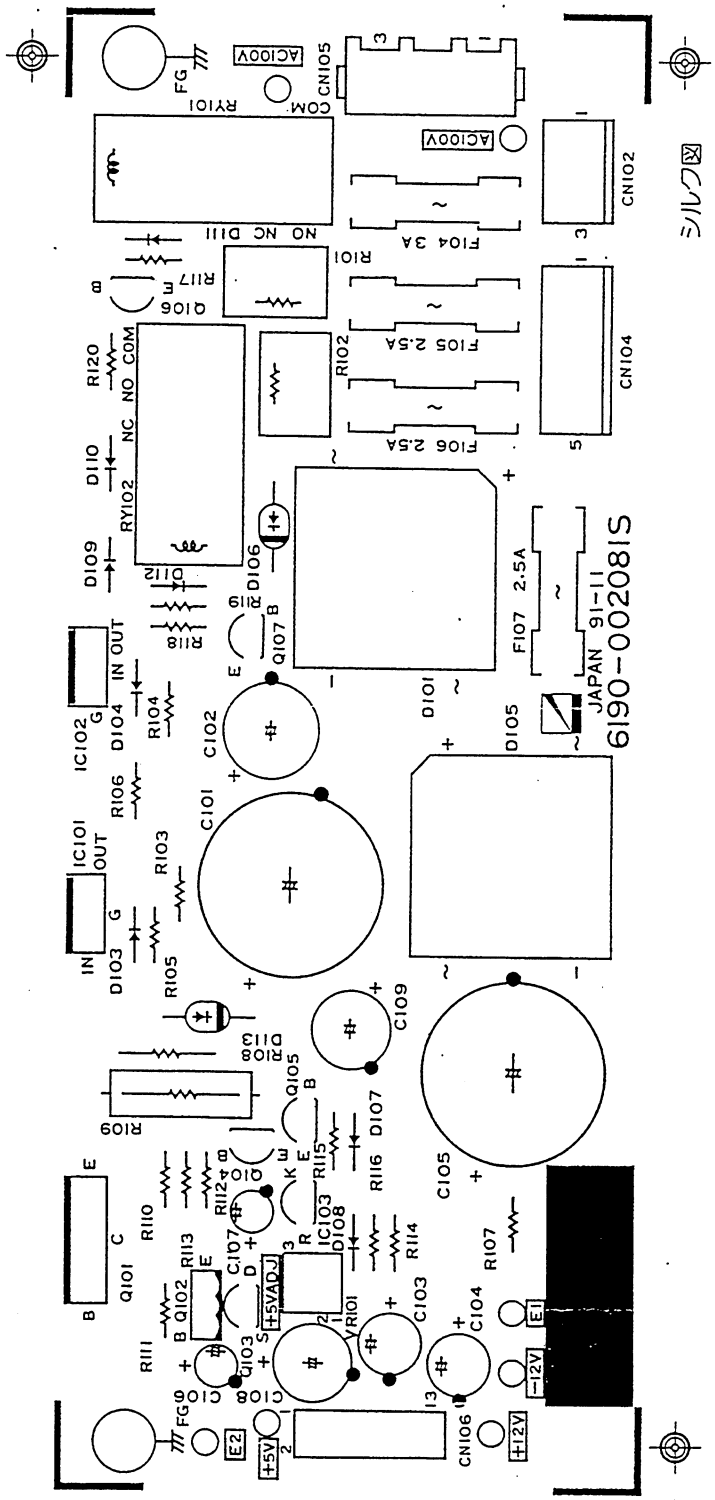


OPERATION CONTROL (VR) BOARD, UP-0802 and LED BOARD, UP-0806,

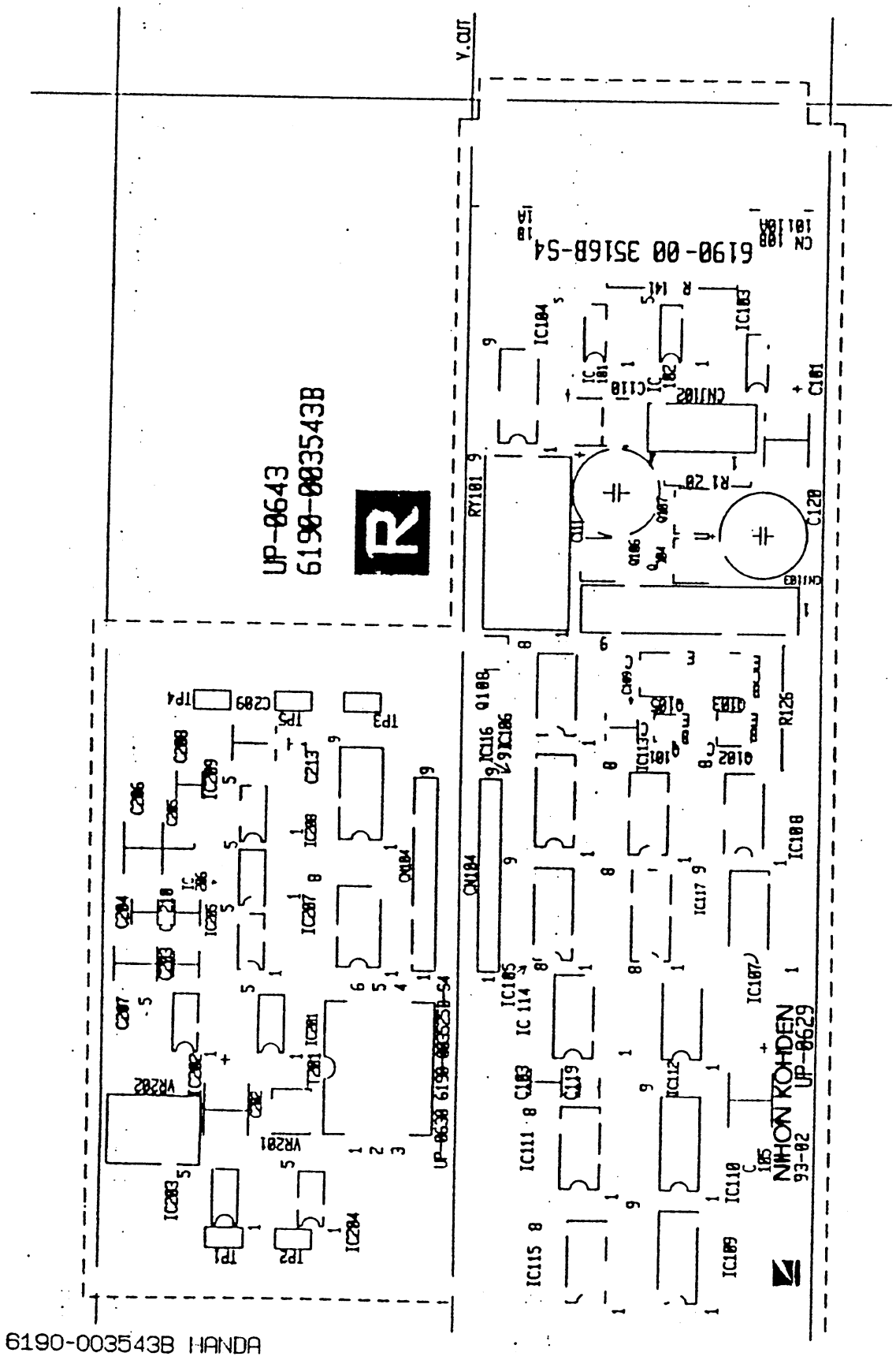


13. PARTS LOCATION GUIDE

Power Supply Unit, SC-019R



NIBP Head Amp (AP-860PA) Main board, UP-0629, and Sub Board, UP-0630



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