DIAGNOSTIC FUNCTION MANUAL
FOR
MODEL  SSA-340A
SERVICE TEST SYSTEM
(2D730-136E°C)

TOSHIBA CORPORATION

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<table>
<thead>
<tr>
<th>REV.</th>
<th>DATE (MM/YY)</th>
<th>REASON</th>
<th>AUTHOR</th>
<th>PAGE CHANGED</th>
<th>SER. No.</th>
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</thead>
<tbody>
<tr>
<td>INI.</td>
<td>02/‘95</td>
<td></td>
<td>Mr. Nakajima</td>
<td>-------</td>
<td>TM-WW</td>
<td></td>
</tr>
<tr>
<td>*A</td>
<td>11/‘95</td>
<td>12/’95 upgrade is supported.</td>
<td>Mr. Yamazaki</td>
<td>P. 4-113 to 115</td>
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<tr>
<td>*B</td>
<td>10/‘97</td>
<td>12/’96 upgrade is supported.</td>
<td>Mr. Okumoto</td>
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<tr>
<td>*C</td>
<td>07/‘98</td>
<td>10/‘98 upgrade is supported.</td>
<td>Mr. Okumoto</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
## CONTENTS

<table>
<thead>
<tr>
<th>Section</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. INTRODUCTION</td>
<td>1-1</td>
</tr>
<tr>
<td>2. OUTLINE OF THE TEST SYSTEM</td>
<td>2-1</td>
</tr>
<tr>
<td>2.1 Configuration of the Test System</td>
<td>2-1</td>
</tr>
<tr>
<td>2.2 Diagnostic Items and Nature of Tests in the Test System</td>
<td>2-1</td>
</tr>
<tr>
<td>2.3 Test Modes (ALL, SUB)</td>
<td>2-12</td>
</tr>
<tr>
<td>3. TROUBLESHOOTING</td>
<td>3-1</td>
</tr>
<tr>
<td>3.1 Preparatory Work</td>
<td>3-3</td>
</tr>
<tr>
<td>3.2 Operating Precautions for the Test Systems</td>
<td>3-3</td>
</tr>
<tr>
<td>3.3 Operating Procedure</td>
<td>3-4</td>
</tr>
<tr>
<td>3.3.1 Procedure until the menu message is displayed</td>
<td>3-4</td>
</tr>
<tr>
<td>3.3.2 Flowchart of the ALL mode</td>
<td>3-6</td>
</tr>
<tr>
<td>3.3.3 Flowchart of the SUB mode</td>
<td>3-6</td>
</tr>
<tr>
<td>3.3.4 Command</td>
<td>3-8</td>
</tr>
<tr>
<td>3.3.5 Changing the frequency of test execution</td>
<td>3-10</td>
</tr>
<tr>
<td>3.4 Error Code Table</td>
<td>3-13</td>
</tr>
<tr>
<td>4. FLOWCHARTS FOR IDENTIFYING MALFUNCTIONS</td>
<td>4-1</td>
</tr>
<tr>
<td>4.1 Identifying Faults in the CPU Unit</td>
<td>4-1</td>
</tr>
<tr>
<td>4.1.1 Preparatory work</td>
<td>4-1</td>
</tr>
<tr>
<td>4.1.2 Flowchart for identifying malfunctions</td>
<td>4-1</td>
</tr>
<tr>
<td>4.1.3 Decision criteria</td>
<td>4-3</td>
</tr>
<tr>
<td>4.1.4 Supplement</td>
<td>4-13</td>
</tr>
<tr>
<td>4.2 Identifying Faults in the PANEL Unit</td>
<td>4-13</td>
</tr>
<tr>
<td>4.2.1 Preparatory work</td>
<td>4-13</td>
</tr>
<tr>
<td>4.2.2 Flowchart for identifying faults</td>
<td>4-13</td>
</tr>
<tr>
<td>4.2.3 Criteria</td>
<td>4-14</td>
</tr>
<tr>
<td>4.2.4 Supplement</td>
<td>4-16</td>
</tr>
</tbody>
</table>
CONTENTS - continued

4.3 Identifying Faults in RPG ................................. 4-18
   4.3.1 Preparatory work ..................................... 4-18
   4.3.2 Troubleshooting flowchart .......................... 4-18
   4.3.3 Decision tree ........................................ 4-20
   4.3.4 Supplement ........................................... 4-21
4.4 Identifying Faults in the DSC Unit ......................... 4-23
   4.4.1 Preparations .......................................... 4-23
   4.4.2 Troubleshooting flowchart .......................... 4-23
   4.4.3 Criteria ............................................... 4-25
4.5 Identifying Faults in the T/R Unit ........................ 4-56
   4.5.1 Preparations .......................................... 4-56
   4.5.2 Fault diagnosis flow chart ......................... 4-56
   4.5.3 Criteria ............................................... 4-59
   4.5.4 Supplement ........................................... 4-71
4.6 Identifying Faults in the FFT Unit ......................... 4-76
   4.6.1 Preparatory work ..................................... 4-76
   4.6.2 Flowchart for identifying faults ................. 4-76
   4.6.3 Criteria ............................................... 4-79
   4.6.4 Supplement ........................................... 4-86
4.7 Identifying Faults in the CFM Unit ......................... 4-87
   4.7.1 Preparatory work ..................................... 4-87
   4.7.2 Flowchart for identifying faults ................. 4-87
   4.7.3 Criteria ............................................... 4-91
   4.7.4 Results of the diagnostic tests .................. 4-105
   4.7.5 Supplement ........................................... 4-111
4.8 Maintenance ................................................ 4-113
CONTENTS - continued

Page

5. APPENDIX ------------------------------------------------------------------------------------- 5-1

5.1 Error Codes for Self-diagnosis ---------------------------------------------- 5-1

5.2 Patch Menu Operation ----------------------------------------------------------- 5-5

5.2.1 Applicable equipment ---------------------------------------------------------- 5-5

5.2.2 Starting ----------------------------------------------------------------------- 5-5

5.2.3 Memory R/W & dump ------------------------------------------------------------- 5-6

5.2.4 Coordinate check (X,Y) -------------------------------------------------------- 5-7

5.2.5 Image cont external value set -------------------------------------------------- 5-7

5.2.6 Address & data value save ----------------------------------------------------- 5-9
1. INTRODUCTION

Test systems are service test units for the ultrasonic diagnostic equipment model SSA-340A.

This manual explains the diagnostic procedures.

Furthermore, since certain PWBs can be checked only if the system operates normally, it is necessary to perform testing in the following order.

(1) CPU unit
(2) RPG
(3) DSC unit
(4) T/R unit
(5) FFT unit
(6) CFM unit
(7) PANEL unit
2. OUTLINE OF THE TEST SYSTEM

If a malfunction occurs, the test system will indicate the test results with respect to PWBs and PWB blocks, identifying those which are responsible for the malfunction by displaying error codes. Alternately, the test system will indicate a pattern which permits assessment of the quality of each block.

Tests principally involve the CPU unit, PANEL unit, RPG, DSC unit, T/R unit, FFT unit, and CFM unit. Although not all units are included, it is possible to test the basic units required for generating an image. Therefore, troubleshooting is expedited if the test system succeeds in helping identify faulty units.

Furthermore, at the time of maintenance and checking it is possible to assess changes in ultrasonic wave transmission which are difficult to observe during the normal service period; degradation of system performance; and memory errors of any addresses caused by faulty reception.

In addition, there are guidelines for test performance frequency. This is useful for checking faults that occur infrequently, caused by RS-232C communication errors.

2.1 Configuration of the Test System

This test system is incorporated in the main unit of the diagnostic ultrasound system.

This manual describes the operating procedures for the test system.

2.2 Diagnostic Items and Nature of Tests in the Test System

PWBs which are tested by the test system are shown in figure 2-1 to figure 2-3. Details concerning each test item are given in Tables 2-1 and 2-2.
Figure 2-1 SSA-340A block diagram
Table 2-1 Table of equipment and corresponding test items

<table>
<thead>
<tr>
<th>Execution sequence</th>
<th>Unit under test</th>
<th>Check item</th>
<th>SSA-340A</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>CPU unit</td>
<td>CPU RAM R/W CHECK</td>
<td>o</td>
</tr>
<tr>
<td>2</td>
<td></td>
<td>CPU ROM CHECK</td>
<td>o</td>
</tr>
<tr>
<td>3</td>
<td></td>
<td>GRAPHIC MEMORY CHECK</td>
<td>o</td>
</tr>
<tr>
<td>4</td>
<td></td>
<td>RS-232C CH1 CHECK</td>
<td>o</td>
</tr>
<tr>
<td>5</td>
<td></td>
<td>RS-232C CH2 CHECK</td>
<td>x</td>
</tr>
<tr>
<td>6</td>
<td></td>
<td>CENTRONICS CHECK</td>
<td>x</td>
</tr>
<tr>
<td>7</td>
<td>PANEL unit</td>
<td>LED CHECK</td>
<td>o</td>
</tr>
<tr>
<td>8</td>
<td>RPG</td>
<td>RATE CHECK</td>
<td>o</td>
</tr>
<tr>
<td>9</td>
<td>USC unit</td>
<td>B/W FM CPU K/W</td>
<td>o</td>
</tr>
<tr>
<td>10</td>
<td></td>
<td>B/W TEST PATTERN (SYNC)</td>
<td>o</td>
</tr>
<tr>
<td>11</td>
<td></td>
<td>B/W TEST PATTERN (ASYNC)</td>
<td>o</td>
</tr>
<tr>
<td>12</td>
<td></td>
<td>B/W LIP TEST PATTERN</td>
<td>o</td>
</tr>
<tr>
<td>13</td>
<td></td>
<td>COLOR FM CPU R/W</td>
<td>o</td>
</tr>
<tr>
<td>14</td>
<td></td>
<td>CAL TEST PATTERN (R)</td>
<td>o</td>
</tr>
<tr>
<td>15</td>
<td></td>
<td>CAL TEST PATTERN (THETA)</td>
<td>o</td>
</tr>
<tr>
<td>16</td>
<td></td>
<td>COLOR RIP TEST PATTERN</td>
<td>o</td>
</tr>
<tr>
<td>17</td>
<td></td>
<td>COLOR LIP TEST PATTERN</td>
<td>o</td>
</tr>
<tr>
<td>18</td>
<td>T/R unit</td>
<td>T/R CONT RAM CHECK</td>
<td>o</td>
</tr>
<tr>
<td>19</td>
<td></td>
<td>DELAY CONT RAM CHECK</td>
<td>o</td>
</tr>
<tr>
<td>20</td>
<td></td>
<td>R-CHANNEL CHECK (SECTOR)</td>
<td>x</td>
</tr>
<tr>
<td>21</td>
<td></td>
<td>R-CHANNEL CHECK (CONVEX)</td>
<td>o</td>
</tr>
<tr>
<td>22</td>
<td></td>
<td>T-CHANNEL CHECK (CONVEX)</td>
<td>o</td>
</tr>
<tr>
<td>23</td>
<td></td>
<td>DELAY TIME CHECK (CONVEX)</td>
<td>o</td>
</tr>
<tr>
<td>24</td>
<td>FFT unit</td>
<td>PH.D OSC CHECK</td>
<td>o</td>
</tr>
<tr>
<td>25</td>
<td></td>
<td>FORWARD FLOW CHECK</td>
<td>o</td>
</tr>
<tr>
<td>26</td>
<td></td>
<td>REVERSE FLOW CHECK</td>
<td>o</td>
</tr>
<tr>
<td>27</td>
<td></td>
<td>BLANK CHECK</td>
<td>o</td>
</tr>
<tr>
<td>28</td>
<td>CFM unit</td>
<td>LB SELF TEST</td>
<td>o</td>
</tr>
<tr>
<td>29</td>
<td></td>
<td>LB/CAL SELF TEST</td>
<td>o</td>
</tr>
<tr>
<td>30</td>
<td></td>
<td>LB/CORR/CAL SELF TEST</td>
<td>o</td>
</tr>
<tr>
<td>31</td>
<td></td>
<td>LB/FIL/CORR/CAL SELF TEST</td>
<td>o</td>
</tr>
<tr>
<td>32</td>
<td></td>
<td>LB/CAL CHECK</td>
<td>o</td>
</tr>
<tr>
<td>33</td>
<td></td>
<td>LB/FIL/CORR/CAL CHECK</td>
<td>o</td>
</tr>
<tr>
<td>Execution sequence</td>
<td>Unit under test</td>
<td>Check item</td>
<td>Purpose of test (nature of check)</td>
</tr>
<tr>
<td>--------------------</td>
<td>-----------------</td>
<td>---------------------</td>
<td>---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------</td>
</tr>
<tr>
<td>1</td>
<td>CPU unit</td>
<td>CPU RAM R/W CHECK</td>
<td>Confirmation of RAM operation in the CPU program [The CPU writes data in RAM and then reads the same data. It then checks RAM function by comparing the two sets of data.]</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td></td>
<td>CPU ROM CHECK</td>
<td>Confirmation of ROM operation in the CPU program [ROM data are added and compared with data added and stored previously. The system checks ROM operation by comparing the two sets of data.]</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td></td>
<td>GRAPHIC MEMORY CHECK</td>
<td>Confirmation of memory operation for display of characters and graphics [The CPU fills the entire memory with alternating 1's and 0's, thus filling the screen with entirely white and entirely black areas.] (When color is used, blue and green are also displayed.)</td>
</tr>
<tr>
<td>4</td>
<td></td>
<td>RS-232C CH1 CHECK</td>
<td>Checking of RS-232C transmission and reception for CH1 [Transmitted data are received unchanged, and compared.]</td>
</tr>
<tr>
<td></td>
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<td></td>
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</tr>
<tr>
<td>Execution sequence</td>
<td>Unit under test</td>
<td>Check item</td>
<td>Purpose of test (nature of check)</td>
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<tr>
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</tr>
<tr>
<td>5</td>
<td>CPU unit</td>
<td>RS-232C CH2 CHECK</td>
<td>Checking of RS-232C transmission and reception for CH2 [Transmitted data are received unchanged, and compared.]</td>
</tr>
<tr>
<td>6</td>
<td></td>
<td>CENTRONICS CHECK</td>
<td>Checking of the printer [To output the test pattern]</td>
</tr>
<tr>
<td>7</td>
<td>RPG</td>
<td>RATE CHECK</td>
<td>Checking of various rate signals [Scan mode for test is set, and the CPU compares the changes in various rate signals with the correct values.]</td>
</tr>
<tr>
<td>8</td>
<td>DSC unit</td>
<td>B/W FM CPU R/W</td>
<td>To check FMA0 through FMA1 and FMB0 through FMB1 (frame memory 1 to 4) for B/W [CPU writes data into FMs and reads the same data, which is then compared.]</td>
</tr>
<tr>
<td>9</td>
<td></td>
<td>B/W TEST PATTERN (SYNC)</td>
<td>• To determine whether the abnormal section is in the DSC unit or in the T/R unit • To check the sampling address</td>
</tr>
<tr>
<td>Execution sequence</td>
<td>Unit under test</td>
<td>Check item</td>
<td>Purpose of test (nature of check)</td>
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<tr>
<td>10</td>
<td>DSC unit</td>
<td>B/W TEST PATTERN (ASYNC)</td>
<td>• To determine whether the abnormal section is in the DSC unit or in the T/R unit&lt;br&gt;• To check the multistage transmission</td>
</tr>
<tr>
<td>11</td>
<td></td>
<td>B/W LIP TEST PATTERN</td>
<td>To determine whether the abnormality is before the output section or after in the DSC unit&lt;br&gt;[The test pattern is input in the linear interpolation circuit.]</td>
</tr>
</tbody>
</table>
| 12                 |                 | COLOR FM CPU R/W | To check FMA0 through FM2 and FMBO through FMBo (frame memory 1 to 6) for COLOR<br>[CPU writes data into FMs and reads the same data, which is then compared.] | Normal: "OK"
Abnormal: Display of abnormal RAM address | CPU |         |
<p>| 13                 |                 | CAL TEST PATTERN (R) | • To check the interpolation function (RIP) in the DSC unit&lt;br&gt;• To determine whether the abnormality is in the MTI unit or in the DSC unit&lt;br&gt;[Interpolation check in the DSC r-direction and threshold check in the θ-direction] (RIP: Radius direction interpolation) | Normal: Display of an even pattern interpolated in the r-direction&lt;br&gt;Abnormal: Display of an abnormally interpolated pattern | Service engineer |         |</p>
<table>
<thead>
<tr>
<th>Execution sequence</th>
<th>Unit under test</th>
<th>Check item</th>
<th>Purpose of test (nature of check)</th>
<th>Message displayed (error code)</th>
<th>Judgement</th>
<th>Remarks</th>
</tr>
</thead>
</table>
| 14                 | DSC unit        | CAL TEST PATTERN (THETA) | - To check the interpolation function (WIP) in the DSC unit  
                   |                  |                         | - To determine whether the abnormal portion is the MTI unit or in the DSC unit  
                   |                  |                         | [Interpolation check in the DSC r-direction and threshold check in the θ-direction]  
                   |                  |                         | (WIP: Write interpolation) | Normal:  
                   |                  |                         | Display of an even pattern interpolated in the θ-direction  
                   |                  |                         | Abnormal:  
                   |                  |                         | Display of an abnormally interpolated pattern | Service engineer |
| 15                 | COLOR RIP TEST PATTERN | To determine whether the abnormal section is before or after the input system of the DSC system.  
                   |                  |                         | (Identifying the abnormality between the MTI unit and in the DSC unit)  
                   |                  |                         | [The test pattern is input in the RIP circuit.] | Normal:  
                   |                  |                         | Display of an interpolated pattern  
                   |                  |                         | Abnormal:  
                   |                  |                         | Display of an abnormally interpolated pattern | Service engineer |
| 16                 | COLOR LIP TEST PATTERN | To determine whether the abnormality is in the section before the output section of the DSC unit or after  
                   |                  |                         | [The test pattern is input to the linear interpolation circuit.] | Normal:  
                   |                  |                         | Display of a pattern of interpolated vertical lines  
                   |                  |                         | Abnormal:  
                   |                  |                         | Display of an abnormally interpolated pattern | Service engineer |
| 17                 | T/R unit        | T/R CONT RAM CHECK | To confirm COMMAND RAM operation  
                   |                  |                         | [The CPU writes data into COMMAND RAM, and reads the same data, then performs checking by comparing the two.] | Normal:  
                   |                  |                         | "OK"  
                   |                  |                         | Abnormal:  
<pre><code>               |                  |                         | Display of abnormal address in RAM | CPU |
</code></pre>
<table>
<thead>
<tr>
<th>Execution sequence</th>
<th>Unit under test</th>
<th>Check item</th>
<th>Purpose of test (nature of check)</th>
<th>Message displayed (error code)</th>
<th>Judgement</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>18</td>
<td>T/R unit</td>
<td>DELAY CONT RAM CHECK</td>
<td>To confirm BRI RAM operation [The CPU writes data into BRI RAM, and reads the same data, then performs checking by comparing the two.]</td>
<td>Normal: &quot;OK&quot; &lt;br&gt;Abnormal: Display of abnormal address in RAM</td>
<td>CPU</td>
<td></td>
</tr>
<tr>
<td>19</td>
<td></td>
<td>R-CHANNEL CHECK (RESERVE)</td>
<td>To confirm that each channel of R-DELAY in the CONVEX system is receiving correctly [Transmission is made by multiple channels, and is sequentially received by one channel at a time for each rate, thus constructing an image.]</td>
<td>Normal: No variations in brightness &lt;br&gt;Abnormal: Variations in brightness</td>
<td>Service engineer</td>
<td></td>
</tr>
<tr>
<td>20</td>
<td></td>
<td>R-CHANNEL CHECK (CONVEX)</td>
<td>To confirm that each channel of PULSER is transmitting correctly [Transmission is made sequentially by one channel at a time for each rate, thus constructing an image.]</td>
<td>Normal: No variation in brightness &lt;br&gt;Abnormal: Variations in brightness</td>
<td>Service engineer</td>
<td></td>
</tr>
<tr>
<td>21</td>
<td></td>
<td>T-CHANNEL CHECK (CONVEX)</td>
<td>To confirm that the delay time in transmission system is controlled correctly [Pattern resulting from the initial echo is to be continuous without any differences in level. (It should be checked comparing the pattern resulting from the CPU.)]</td>
<td>Normal: Delay time pattern of continuous type &lt;br&gt;Abnormal: Pattern of non-continuous type</td>
<td>Service engineer</td>
<td></td>
</tr>
<tr>
<td>22</td>
<td></td>
<td>DELAY TIME CHECK (CONVEX)</td>
<td>To confirm that the delay time in transmission system is controlled correctly [Pattern resulting from the initial echo is to be continuous without any differences in level. (It should be checked comparing the pattern resulting from the CPU.)]</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Execution sequence</td>
<td>Unit under test</td>
<td>Check item</td>
<td>Purpose of test (nature of check)</td>
<td>Message displayed (error code)</td>
<td>Judgment</td>
<td>Remarks</td>
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</tr>
<tr>
<td>23</td>
<td>FFT</td>
<td>PH.D OSC CHECK</td>
<td>Determining whether the abnormal portion is in the FFT or in the T/R system. [To send the test pattern to the PHASE DETECTION input]</td>
<td>Normal: Agree with the expected value pattern Abnormal: Does not agree with the expected value pattern</td>
<td>Service engineer</td>
<td></td>
</tr>
<tr>
<td>24</td>
<td></td>
<td>FORWARD FLOW CHECK</td>
<td>To test for abnormalities following FFT [To send the sequential test pattern to the FFT input]</td>
<td>Same as above</td>
<td>Service engineer</td>
<td></td>
</tr>
<tr>
<td>25</td>
<td></td>
<td>REVERSE FLOW CHECK</td>
<td>To test for abnormalities following FFT [To send the reverse test pattern to the FFT input]</td>
<td>Normal: Agree with the expected value pattern Abnormal: Does not agree with the expected value pattern</td>
<td>Service engineer</td>
<td></td>
</tr>
<tr>
<td>26</td>
<td></td>
<td>BLANK CHECK</td>
<td>Same as above [To send the non-signal test pattern to the FFT input]</td>
<td>Normal: No message Abnormal: Display of white points, etc.</td>
<td>Service engineer</td>
<td></td>
</tr>
<tr>
<td>27</td>
<td>CFM</td>
<td>LB SELF TEST</td>
<td>The test pattern is input, and the results of operation are compared with the correct value. [To test only the test RAM of the line buffer]</td>
<td>Normal: &quot;OK&quot; Abnormal: Display of error message</td>
<td>CPU</td>
<td></td>
</tr>
<tr>
<td>Execution sequence</td>
<td>Unit under test</td>
<td>Check item</td>
<td>Purpose of test (nature of check)</td>
<td>Message displayed (error code)</td>
<td>Judgement</td>
<td>Remarks</td>
</tr>
<tr>
<td>--------------------</td>
<td>----------------</td>
<td>------------</td>
<td>-----------------------------------</td>
<td>-------------------------------</td>
<td>-----------</td>
<td>---------</td>
</tr>
<tr>
<td>28</td>
<td>CFM</td>
<td>LB/CAL SELF TEST</td>
<td>Same as above [To test the line buffer and calculator]</td>
<td>Same as above</td>
<td>CPU</td>
<td></td>
</tr>
<tr>
<td>29</td>
<td></td>
<td>LB/CORR/CAL SELF TEST</td>
<td>Same as above [To test the line buffer, correlator and calculator]</td>
<td>Same as above</td>
<td>CPU</td>
<td></td>
</tr>
<tr>
<td>30</td>
<td></td>
<td>LB/FIL/CORR/CAL SELF TEST</td>
<td>Same as above [To test the line buffer, filter, correlator and calculator]</td>
<td>Same as above</td>
<td>CPU</td>
<td></td>
</tr>
<tr>
<td>31-36</td>
<td></td>
<td>LR/CAL CHECK</td>
<td>The test pattern is input, and the results are checked by visual inspection. [To test the line buffer and calculator]</td>
<td>Normal: A character pattern is displayed. The gradation curve becomes linear. Abnormal: Character pattern is not displayed sharply. The gradation curve does not become linear.</td>
<td>Service engineer</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>(BDF L)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>(BDF M)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>(BDF H)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>(BDF M)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>(MDF H)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>(BDF H)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>(BDF/MDF L)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>37-42</td>
<td></td>
<td>LB/FIL/CORR/CAL CHECK</td>
<td>The test pattern is input, and the results are checked by visual inspection. [To test the line buffer, filter, correlator and calculator]</td>
<td>Same as above</td>
<td>Service engineer</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>(BDF L)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>(BDF M)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>(BDF H)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>(MDF M)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>(MDF H)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>(BDF/MDF L)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Execution sequence</td>
<td>Unit under test</td>
<td>Check item</td>
<td>Purpose of test (nature of check)</td>
<td>Message displayed (error code)</td>
<td>Judgement</td>
<td>Remarks</td>
</tr>
<tr>
<td>--------------------</td>
<td>-----------------</td>
<td>--------------</td>
<td>-----------------------------------</td>
<td>----------------------------------------------------------</td>
<td>---------------</td>
<td>----------------</td>
</tr>
<tr>
<td>43</td>
<td>PANEL unit</td>
<td>LED CHECK</td>
<td>Turns the LEDs on PANEL ON/OFF</td>
<td>Normal: The SW LEDs light sequentially. Abnormal: The SW LEDs do not light.</td>
<td>Service engineer</td>
<td></td>
</tr>
</tbody>
</table>
2.3 Test Modes (ALL, SUB)

(1) ALL mode (general-purpose test mode for beginners)

All tests are conducted using this test mode. Use this mode if the faulty units are not identified.

This, however, takes a long time and requires several operations by the serviceman to get the final diagnostic results.

(2) SUB mode (test mode for experts)

Use this test mode to conduct a specific test if the faulty sections can be guessed from the symptoms.
3. **TROUBLESHOOTING**

Carry out tests to identify malfunctions according to the following procedure:

(1) Preliminary survey

(2) Preparatory work (with the power off)

(3) Setting of the service mode

(4) Setting of the test mode (ALL, SUB mode)

(5) Test

(6) Identification of malfunction based on the error code table

Figure 3-1 shows the flowchart for the above procedure.

**Preliminary survey**

Survey the stated problems not just by relying on information from the customer, but also by checking carefully the status of each mode and function. Problems that occur only occasionally cannot be identified by the test system when it is not actually occurring.

(For tests which are controlled by the CPU, such as the check of the RS-232C or the R/W of RAM, the test system can provide a means of reproducing the phenomenon by repeating the test sequence an unlimited number of times.)
**Preparatory work**

- Prepare tools, etc.
- Connect the specified probe (See section 3.2. (1)).
- Set the B-GAIN to MAX.
- Set the DEPTH to 10 cm.

**Setting of the service mode**

- Connect the specified probe (See section 3.2. (1)).
- Set the B-GAIN to MAX.
- Set the DEPTH to 10 cm.

**Turn on the power.**

- Press \( \text{SETTING} \) to display the SETTING menu

**Move the cursor to [SERVICE] in the SETTING menu and press \( \text{SERVICE} \).**

- Press \( \text{SERVICE} \) on the keyboard. At this time, the system enters the SERVICE menu.

**Move the cursor to [TEST] in the SERVICE menu and press \( \text{TEST} \).**

- Enter "ALPHA" from keyboard. At this time, the system enters the SERVICE menu.

**Enter numbers (for example, [0] \( \text{numbers} \) ) from the keyboard.**

- Carry out various tests.

**Error codes and messages will be displayed.**

- Identify faulty PWBs using the error code table.

---

*Reference manual for the test system (This manual)*
- Set of general service tools
- Jigs required for the test
3.1 Preparatory Work

Prepare the required tools/devices (such as a return connector) in accordance with the "Preparatory work" in section 4. (ex. LOOP BACK CNN)

3.2 Operating Precautions for the Test Systems

(1) Before carrying out tests, the transducer should be connected as specified below. Do not pull out or connect a probe during the test unless so instructed, otherwise a malfunction may occur.

<table>
<thead>
<tr>
<th>TRANSDUCER C</th>
<th>TRANSDUCER B</th>
<th>TRANSDUCER A</th>
</tr>
</thead>
<tbody>
<tr>
<td>SSA-340A</td>
<td>Linear or convex transducer, or no connection</td>
<td>PVF-375MT</td>
</tr>
</tbody>
</table>

(2) A transient phenomenon is displayed while the test is being carried out; however, this is not abnormal.

(3) The time, heart rate, PWR value, ID area and hospital name are not erased. The ID indication is erased.

(4) Pressing [button] at the graphic check of the CPU may cause a blank area on the upper right of the image; however, this is not abnormal (Photo 3.2-1).

(5) Although most switches are disabled during the serviceman test, do not press the following switches to avoid a malfunction:

- VCR SW (on the panel)
- Palm controller trackball
- Trackball (TRACK BALL FUNCTION)

(6) When the graphic check of the CPU is completed, either of the two lines for time display may not be displayed; however, this is not abnormal.

(7) Because peripheral devices may malfunction during testing, disconnect the control cables of all peripheral devices during testing. Alternatively, turn OFF the power of all peripheral devices.

(8) Be sure to execute New Patient after the test has been completed.
3.3 Operating Procedure

3.3.1 Procedure until the menu message is displayed

First perform the "Setting of the service mode" of the flowchart shown in figure 3-1.

The screen shown in figure 3.3-1-1 first appears in the serviceman test.
Then the caution screen shown in photo 3.3-1-2 appears, requesting that the following be checked.

(1) The probes specified in section 3.2 (1) have been connected.

After confirming the above, press \[ \] and the screen in photo 3.3-1-3 will appear.
Photo 3.3-1-1

Photo 3.3-1-2
Test items which cannot be executed are marked with X in place of a number.

3.3.2 Flowchart of the ALL mode

To select the ALL mode, press [0] and 4 in the screen in photo 3.3-1-3.

Test will be executed in accordance with the flowchart in figure 3.3-2-1.

(Press [9] and  to terminate the execution of the tests.)

3.3.3 Flowchart of the SUB mode

Press one of [1] to [8] and then  to start the test and execute the SUB mode.

(Press [9] and  to terminate the execution of the tests.)
Figure 3.3-2-1  Flow chart of the SUB mode

Note: Check items marked * cannot be performed in the 340A.
### Command

The basic operation commands are described below.

<table>
<thead>
<tr>
<th>No.</th>
<th>Purpose</th>
<th>Operation</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>To execute the ALL mode</td>
<td>Press the key of the number representing ALL TEST or ALL CHECK in the displayed menu and then press</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>To execute the SUB mode</td>
<td>Press the key of the number representing the item to be executed in the displayed menu and then press</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>To terminate the serviceman test</td>
<td>Four methods are available: (1) Press the NEW PATIENT SW (2) Press the PRESET A, B and C (3) While the menu of the above figure 3.3-1-3 is being displayed, press [9] and</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>To return to the preceding menu</td>
<td>Two methods are available: (1) When the menu displayed contains the END item, press the corresponding numeric key and then press</td>
<td>(2) press ← when so instructed.</td>
</tr>
<tr>
<td>5</td>
<td>To proceed to the next check</td>
<td>Three methods are available: (1) When so instructed, press ⇪. (2) Press the numeric key corresponding to the item in the displayed menu and then press</td>
<td>(3) When so instructed, press [F].</td>
</tr>
</tbody>
</table>

3-8
<table>
<thead>
<tr>
<th>No.</th>
<th>Purpose</th>
<th>Operation</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>To change the frequency of test execution</td>
<td>Refer to section 3.3.5.</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>To terminate the test when the test execution frequency is unlimited.</td>
<td>Press [DEL].</td>
<td>This can be performed even when the test frequency is not unlimited.</td>
</tr>
<tr>
<td>9</td>
<td>To correct a value entered incorrectly.</td>
<td>Press [DEL] and enter the correct value.</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>To stop the display of an error message at the time of memory check</td>
<td>Press [C] when so instructed.</td>
<td></td>
</tr>
</tbody>
</table>

Note: For the RS-232C Centronix check, the [DEL] key does not work immediately.
3.3.5 Changing the frequency of test execution

(1) The menu of each test includes the item CHECK COUNT SET just preceding the item of END.

Press the numeric key corresponding to CHECK COUNT SET and then press [7]. (See photo 3.3-5-1.)

Then the screen in photo 3.3-5-2 will appear.

Photo 3.3-5-1
(2) Press the numeric key corresponding to the desired text execution frequency and then press 

When [0] and \( \text{[key]} \) are pressed, the frequency will be an unlimited number of times.
(3) When is pressed at (2), the screen returns to the preceding screen with the new frequency displayed as "CHECK COUNT = XXX" (photo 3.3-5-3). If the wrong frequency is entered, perform the steps from (1) again.

![Photo 3.3-5-3](image-url)
### 3.4 Error Code Table

The error codes for visual check are described below.

<table>
<thead>
<tr>
<th>Error code</th>
<th>PWB error has occurred</th>
<th>Detail of the error</th>
<th>Reference</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU 00</td>
<td>CPU</td>
<td>Graphic memory abnormal</td>
<td>No. 3 of 4.1.3</td>
</tr>
<tr>
<td>CPU 01</td>
<td>CPU</td>
<td>Centronics abnormal</td>
<td>No. 6 of 4.1.3</td>
</tr>
<tr>
<td>PNL 00</td>
<td>PANEL CPU</td>
<td></td>
<td>4.2.3</td>
</tr>
<tr>
<td>DSC 01</td>
<td>PC DSC</td>
<td>Sampling address abnormal</td>
<td>No. 2 of 4.4.3</td>
</tr>
<tr>
<td>DSC 02</td>
<td>RPG/TR CONT B &amp; W DSC</td>
<td>Raster address abnormal</td>
<td>No. 3 of 4.4.3</td>
</tr>
<tr>
<td>DSC 03</td>
<td>B &amp; W DSC</td>
<td>FM-OUT GA abnormal or abnormal between FM-OUT GA and GAMMARAM</td>
<td>No. 4 of 4.4.3</td>
</tr>
<tr>
<td>DSC 04</td>
<td>ADC/LB/CAL CFM DSC RGB CONVERTER</td>
<td>RIP abnormal, etc.</td>
<td>No. 6 of 4.4.3</td>
</tr>
<tr>
<td>DSC 05</td>
<td>Ditto</td>
<td>WIP abnormal, etc.</td>
<td>No. 7 of 4.4.3</td>
</tr>
<tr>
<td>DSC 06</td>
<td>CFM DSC and the subsequent PWBs</td>
<td>FM-OUT SC abnormal, etc.</td>
<td>No. 8 of 4.4.3</td>
</tr>
<tr>
<td>DSC 07</td>
<td>ADC/LB/CAL CFM DSC RGB CONVERTER</td>
<td>FM-OUT GA abnormal, etc.</td>
<td>No. 9 of 4.4.3</td>
</tr>
<tr>
<td>T/R 00</td>
<td></td>
<td>Reception system abnormal</td>
<td>4.5</td>
</tr>
<tr>
<td>T/R 01</td>
<td></td>
<td>Reception system abnormal</td>
<td>4.5</td>
</tr>
<tr>
<td>T/R 02</td>
<td></td>
<td>Transmission system abnormal</td>
<td>4.5</td>
</tr>
<tr>
<td>T/R 03</td>
<td></td>
<td>Delay-line system abnormal</td>
<td>4.5</td>
</tr>
<tr>
<td>FFT 01</td>
<td>PHASE DETECTOR FFT UNIT</td>
<td>Analog system abnormal (PHASE DETECTOR FFT I/O)</td>
<td>4.6.2</td>
</tr>
<tr>
<td>FFT 02</td>
<td>FFT/CONT/AUDIO</td>
<td>Digital system abnormal FFT/CONT/AUDIO</td>
<td>4.6.2</td>
</tr>
<tr>
<td>FFT 03</td>
<td>FFT AUDIO &amp; L/M FFT CONT</td>
<td>Digital system abnormal (FFT)</td>
<td>4.6.2</td>
</tr>
<tr>
<td>FFT 04</td>
<td>FFT AUDIO &amp; L/M FFT CONT</td>
<td>Digital system abnormal (FFT)</td>
<td>4.6.2</td>
</tr>
<tr>
<td>Error code</td>
<td>PWB error has occurred</td>
<td>Detail of the error</td>
<td>Reference</td>
</tr>
<tr>
<td>------------</td>
<td>------------------------</td>
<td>---------------------</td>
<td>-----------</td>
</tr>
<tr>
<td>CFM01 to CFM03</td>
<td>CAL section on the ADC/LB/CAL PWB (BDF)</td>
<td>Abnormal ROM table and control system in the BDF channel system.</td>
<td>No. 5 to 7 of 4.7.3</td>
</tr>
<tr>
<td>CFM04 to CFM05</td>
<td>CAL section on the ADC/LB/CAL PWB (MDF)</td>
<td>Abnormal ROM table and control system in the MDF channel system.</td>
<td>No. 8 to 9 of 4.7.3</td>
</tr>
<tr>
<td>CFM06</td>
<td>CAL section on the ADC/LB/CAL PWB (BDF/MDF)</td>
<td>Abnormal ROM table and control system in the BDF/MDF channel system.</td>
<td>No. 10 of 4.7.3</td>
</tr>
<tr>
<td>CFM11 to CFM13</td>
<td>ADC/LB/PWB and FIL/CORR PWB (BDF)</td>
<td>Abnormal control system and memory channel in the BDF channel system.</td>
<td>No. 11 to 13 of 4.7.3</td>
</tr>
<tr>
<td>CFM14 to CFM15</td>
<td>ADC/LB/CAL PWB and FIL/CORR PWB (MDF)</td>
<td>Abnormal control system and memory channel in the MDF channel system.</td>
<td>No. 14 to 15 of 4.7.3</td>
</tr>
<tr>
<td>CFM16</td>
<td>ADC/LB/CAL PWB and FIL/CORR PWB (BDF/MDF)</td>
<td>Abnormal control system and memory channel in the BDF/MDF channel system.</td>
<td>No. 16 of 4.7.3</td>
</tr>
</tbody>
</table>
4. FLOWCHARTS FOR IDENTIFYING MALFUNCTIONS

4.1 Identifying Faults in the CPU Unit

4.1.1 Preparatory work

The following preparatory work is required before carrying out the tests for the CPU which are listed below:

1. When the RS-232C interface is checked
   a) The power to the ultrasonic diagnostic equipment is switched OFF.
   b) Connect the loopback connector to the PS-232C connector on the bottom of the main panel of the diagnostic ultrasound equipment.
      For the loopback connector, use the connector to which the following pins have been connected in the shell of the DSUB-25S connector.
      1) SD (pin 2) - RD (pin 3)
   c) The power to the ultrasonic diagnostic equipment is switched ON, and the CPU test is selected.

4.1.2 Flowchart for identifying malfunctions

The flow of processing of the CPU test system is shown as a flowchart. Figure 4.1-1 shows the processing flow of the entire CPU test system.

Since actual processing will proceed according to this flowchart when the test system is operated, it is recommended that the fault be diagnosed while confirming the processing currently being performed with respect to the entire test system by referring to this flowchart.
<CPU TEST>

START
Selection of test mode

0: ALL CHECK
Check of R/W in RAM
Check of checksum in ROM
Check of memory for character, graphic display (Plane: 1 to 4)
Transmission/reception check of RS-232C IF 1CH
Termination of CPU test and return to the main menu.

1: RAM CHECK
Check of R/W in RAM

RETURN

2: ROM CHECK
Check of checksum in ROM

RETURN

3: GRAPHIC MEMORY CHECK
Checking memory for character and graphic display (Plane 1: for character display)

RETURN

4: RS-232C 1CH CHECK
Confirmation of RS-232C IF 1CH operation

RETURN

5: RS-232C 2CH CHECK
Confirmation of RS-232C IF 2CH operation

RETURN

6: CENTRONICS CHECK
Confirmation of CENTRONICS IF operation

RETURN

7: CHECK COUNT
Setting of the test frequency

RETURN

Note: * Tests not performed in the 340A.

Figure 4.1-1
4.1.3 Decision criteria

This section shows decision criteria (normal or abnormal) for results of the tests performed according to the flowchart in section 4.1.2, depending on the messages resulting from images obtained.

Items which do not match the normal data shown here are faults as test results and faulty portions.
No. 2D730-136E

[No. 0] CPU test menu

Application:

Selection of CPU test menu
(Refer to photo 4.1-1)

Outline:

To perform selected CPU tests by function

0 ALL CHECK
  → To perform RAM CHECK, ROM CHECK, GRAPHIC MEMORY CHECK, RS-232C CH1 CHECK, RS-232C CH2 CHECK, CENTRONICS CHECK sequentially.

1 RAM CHECK
  → To check RAM operation.

2 ROM CHECK
  → To check ROM operation.

3 GRAPHIC MEMORY CHECK
  → To check graphic memory operation.

4 RS-232C CH1 CHECK (For the 160A/270A/250A and 140A CPUs)
  → To check RS-232C interface CH1 operation.

x RS-232C CH2 CHECK
  → To check RS-232C interface CH2 operation.

x CENTRONICS CHECK
  → To check CENTRONICS interface operation.
7 CHECK COUNT

→ To set the frequency of the CPU test. (This is preset at a frequency of one normally.)

8 END

→ To complete the CPU test and return to the main menu.

Procedure:

→ To input the No. of the test which is to be performed

Example..... ROM CHECK


Note:

Before performing a check, including the RS-232C CH1 CHECK, RS-232C CH2 CHECK, and CENTRONICS CHECK, refer to 4.1.1 Preparatory work.
No. 2D730-136E

[No. 1] CPU RAM CHECK

Application:

Operation check of RAM for the CPU program

Outline:

After data is written into RAM, data is read, then compared with the written data. If they do not match, non-matching addresses are indicated.

Procedure:

The CPU carries out the test automatically and displays the message in 1):

1) *** CPU RAM CHECK ***

2) Results are displayed sequentially in the RAM unit.

3) When test results are normal:

The displayed image is as shown in photo 4.1-2.

The system advances to the next CHECK (CPU ROM CHECK) when [ ] is pressed.

The CPU test menu is displayed when [ ] is pressed.
4) When test results are abnormal:

Based on the results of comparison, abnormal addresses are displayed.

Bits set to "1" indicate bits with abnormal RAM.

If [F] is pressed, advances to the next address.

If [C] is pressed, completes the present RAM check, and performs the next RAM check.

Operation upon completion of all addresses is the same as in 3) above.

RAM showing abnormal addresses in the above tests are faulty. Replace the CPU PWB.
[No. 2] CPU ROM CHECK

Application:

Operation check of ROM for the CPU program

Outline:

Checksum is performed by reading the contents of ROM, then comparison is made with the previous checksum results, and IC locations and checksum results (OK = normal) are indicated.

Procedure:

The CPU carries out the test automatically, and displays the message in 1):

1) *** CPU ROM CHECK ***

2) Results are displayed sequentially for each ROM unit.

3) When test results are normal:

The displayed image is as shown in photo 4.1-3.

With [ ] ON, the system advances to the next CHECK (GRAPHIC MEMORY).

With [ ] ON, the CPU test menu is displayed.

4) When test results are abnormal:

The location of abnormal ROM is displayed.

Operations upon completion of all ROM CHECKs are the same as those in 3) above.

Abnormal ROM is identified from the above results. Faulty ROM should be replaced.
[No. 3] GRAPHIC MEMORY CHECK

Application:

Operation check of CPU

GRAPHIC MEMORY

Outline:

"1" and "0" are written on 6 planes of GRAPHIC MEMORY.

The CRT screen will appear black and white.
(With the color display, the CRT screen will appear green and blue.)

Procedure:

Check visually that the CRT screen displays a normal black and white pattern.

1) *** GRAPHIC MEMORY CHECK ***
(Refer to photo 4.1-4)

2) The test starts when \( \text{[} \) is pressed.

3) When test results are normal:

The CRT screen becomes "white" as shown in photo 4.1-5. Then, when [F] is pressed, the CRT screen becomes "black" as shown in photo 4.1-6, permitting visual check.

If [F] is pressed, the next GRAPHIC MEMORY CHECK is performed.

After checking 6 planes of GRAPHIC MEMORY, the system advances to the next CHECK when \( \text{[} \) is pressed.

(RS-232C CH1 CHECK).

The CPU test menu is displayed when \( \text{[} \) is pressed.
4) When test results are abnormal:

The CRT screen becomes other than black and white (green and blue), as shown in photo 4.1-7.
(Refer to ERROR NO. CPU 00)

Operations upon completion of all GRAPHIC MEMORY CHECK are the same as those in 2) above.

If an abnormality is found, the CPU PWB should be replaced.

Reference:

The locations of GRAPHIC MEMORY

GRAPHIC MEMORY 1  8C
GRAPHIC MEMORY 2  8A
GRAPHIC MEMORY 3  10C
GRAPHIC MEMORY 4  10A
GRAPHIC MEMORY 5  12C
GRAPHIC MEMORY 6  12A
[No. 4] RS-232C (CH1) CHECK

Application:

Transmission and reception check for the CPU RS-232C interface CH1

Outline:

The contents of transmission from the equipment and reception from the return connector are compared, and if the two do not agree, an error is indicated.

Procedure:

The CPU carries out the test automatically and displays the message in 1):

1) *** RS-232C (CH1) CHECK ***

2) When test results are normal:

The displayed image is as shown in photo 4.1-8.

The system advances to the next CHECK when \(\text{\textgreater}\) is pressed.

(RS-232C CH2 CHECK).

The CPU test menu is displayed when \(\text{\textleft}\) is pressed.

3) When test results are abnormal:

An error message is displayed as shown in photo 4.1-9.

Types and meanings of error messages are given in table 4.1-1.

Operations after display of an error message are the same as in 2) above.
Note:
Before performing this CHECK, refer to 4.1.1 Preparatory work.
If the return connector is not connected, a NO ANSWER BACK occurs.

Table 4.1-1 Error messages

<table>
<thead>
<tr>
<th>No.</th>
<th>Error message</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>FRAMING ERROR</td>
<td>Format of 1 character received is not correct.</td>
</tr>
<tr>
<td>2</td>
<td>OVERRUN ERROR</td>
<td>Before 1 character received is processed, the next character is received.</td>
</tr>
<tr>
<td>3</td>
<td>PARITY ERROR</td>
<td>A parity error has occurred within 1 character received.</td>
</tr>
<tr>
<td>4</td>
<td>TIME OUT ERROR</td>
<td>Transmission could not be performed within one minute upon completion of preparation.</td>
</tr>
<tr>
<td>5</td>
<td>NO ANSWER BACK</td>
<td>Text could not be received.</td>
</tr>
<tr>
<td>6</td>
<td>COMPARE ERROR</td>
<td>Transmitted and received text do not agree.</td>
</tr>
</tbody>
</table>
4.1.4 Supplement

The checksum value must be registered prior to the CPU ROM check. Two different registration methods are available.

(1) Refer to subsection 4.8.

(2) This method clears the preset data, and requires resetting of the preset data.

(a) Turn on No. 3 of the DIP SW on the CPU PWB.

(b) Turn on the power.

(c) When the following message is displayed, key-in Y:

   INITIALIZE PRESET DATA
   ARE YOU SURE?

(d) After the initial screen displaying a B mode image appears, turn off No. 3 of the DIP SW.

Note: The above procedure has been already performed before shipment from the factory.

4.2 Identifying Faults in the PANEL Unit

4.2.1 Preparatory work

No preparatory work is required.

4.2.2 Flowchart for identifying faults

   START

   The LED on the panel blinks at intervals of approx. 1 second.

   RETURN

Figure 4.2-1
4.2.3 Criteria

(Purpose) To identify faults in the PANEL unit.

(Outline) Turns the LEDs of the switches indicated by _ in figure 4.2-2 ON/OFF at intervals of approximately one second.

Not all LEDs on the PANEL are turned OFF/ON at intervals of about 1 s (Some LEDs may be always on, always off, or going OFF/ON at intervals other than 1 s).

(1) Either the LEDs of switches not on the full keyboard are abnormal or
(2) The LEDs of switches on the keyboard are abnormal.

Both groups (1) and (2) are abnormal.

Yes

It is highly probable that the PANEL is faulty.

No

It is highly probable that the CPU PWB or the cable between the CPU and the PANEL is faulty. (If the panel data bus is faulty, LEDs in both groups (1) and (2) will be abnormal, regardless of the panel's condition.)

Note: The above is based on the assumption that the D & D MOTHER PWB is normal.
Figure 4.2-2 Panel of the SSA-340A
Figure 4.2-3 Peripheral control signal path
Figure 4.2-4 PANEL/CPU block diagram
4.3 Identifying Faults in RPG

4.3.1 Preparatory work

None

4.3.2 Troubleshooting flowchart

Troubleshooting procedures for RPG faults are shown in the flowchart.

<RPG CHECK>

START

Checking of various enable signals, raster addresses, OR, generated in the RPG

RETURN
Signal names and functions which can be checked using this test program and PWB names which utilize these signals are shown in the table below.

<table>
<thead>
<tr>
<th>Signal name (between boards)</th>
<th>Function</th>
<th>CPU</th>
<th>B &amp; W DSC</th>
<th>CFM DSC</th>
<th>IMAGE MEMORY</th>
<th>FFT/CONT/AUDIO</th>
<th>MIT CONT</th>
<th>ECG/NON FADE</th>
</tr>
</thead>
<tbody>
<tr>
<td>BSAEN0</td>
<td>Signal showing B mode echo sampling rate</td>
<td>o</td>
<td>o</td>
<td>o</td>
<td>o</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>M1SAENO</td>
<td>Signal showing M1 mode echo sampling rate</td>
<td>o</td>
<td>o</td>
<td>o</td>
<td>o</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>M2SAEN0</td>
<td>Signal showing M2 mode echo sampling rate</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DSAEN0</td>
<td>Signal showing D mode echo sampling rate</td>
<td>o</td>
<td></td>
<td>o</td>
<td>o</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FFTCMDO</td>
<td>Signal showing transfer rate for FFT operation data to DSC</td>
<td>o</td>
<td>o</td>
<td>o</td>
<td>o</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>BDFSAEN0</td>
<td>Signal showing DDF mode echo sampling rate</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>o</td>
<td></td>
</tr>
<tr>
<td>MDFSAEN0</td>
<td>Signal showing MDF mode echo sampling rate</td>
<td>o</td>
<td></td>
<td>o</td>
<td>o</td>
<td></td>
<td>o</td>
<td></td>
</tr>
<tr>
<td>DFINTU</td>
<td>Signal showing initial GFM operation sampling rate</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>o</td>
</tr>
<tr>
<td>DFA*0 (3 bit)</td>
<td>ID signal showing position of transmission focus</td>
<td>o</td>
<td>o</td>
<td>o</td>
<td>o</td>
<td></td>
<td>u</td>
<td></td>
</tr>
<tr>
<td>TRAST*0 (12 bit)</td>
<td>Raster address for transmission and reception</td>
<td>o</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DRAST*0 (12 bit)</td>
<td>Raster address for indication</td>
<td>o</td>
<td>o</td>
<td>o</td>
<td>o</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
4.3.3 Decision tree

From the test results, normal (OK) or abnormal (NG) is determined for each signal as shown below.

If NG is indicated, it is highly likely that the RPG PWB is faulty, and the PWB should be replaced.
4.3.4 Supplement

The RPG test program is activated when the host CPU sets test scan mode with respect to the RPG.

[Specification of test scan mode]

(1) Each enable signal is set to the enable condition sequentially for each rate, as shown in the attached timing chart.

(2) Focus

B : F0, F3, F4, F5, F6, F7 (6 step CF)
M1 : F1
M2 : F2

(3) Number of B mode raster lines : 240

The raster address ranges from 0 to 239 in the upper 8 bits.

(4) M-mode position

M1 : 55 (H)
M2 : AA (H)

[Functions of the Host CPU]

(1) Sets test scan mode in the I/O port of the RPG.

(2) By setting data 0 --> 1 --> 0 in the I/O port #70/19 TSTSYNCl bit, the leading edge of this signal serves as a trigger for generating the rate once.

(3) Each time the rate is generated once, data is read from I/O port #70/1C, lD, and it is checked whether such data agrees with the data shown in the attachment.

(4) For NG, the NG decision is made with respect to the signal in the specific bit, and the signal name is indicated.

(5) By generating the rate 8 x 240 = 1920 times, one frame is completed and DOFO is generated, thereby causing OF interruption with respect to the CPU. The CPU completes the test upon confirmation of this interruption.
Test scan timing chart

(Signals on the mother board are obtained by inverting the signals below)

<table>
<thead>
<tr>
<th>TRAST1</th>
<th>BSAEN1</th>
<th>M1SAEN1</th>
<th>M2SAEN1</th>
<th>DSAEN1</th>
<th>FFTCMD1</th>
<th>BDFSAEN1</th>
<th>MDFAEN1</th>
<th>DFINT1</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

DFA*1 (3 bits)

<table>
<thead>
<tr>
<th>TRAST*1 (12 bits)</th>
</tr>
</thead>
<tbody>
<tr>
<td>B0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>True values of port data</th>
</tr>
</thead>
<tbody>
<tr>
<td># 70/1C</td>
</tr>
<tr>
<td># 70/1D</td>
</tr>
<tr>
<td>000 (h)</td>
</tr>
<tr>
<td>000</td>
</tr>
<tr>
<td>010</td>
</tr>
<tr>
<td>020</td>
</tr>
<tr>
<td>550</td>
</tr>
<tr>
<td>550</td>
</tr>
<tr>
<td>550</td>
</tr>
<tr>
<td>550</td>
</tr>
<tr>
<td>550</td>
</tr>
<tr>
<td>550</td>
</tr>
<tr>
<td>550</td>
</tr>
<tr>
<td>550</td>
</tr>
<tr>
<td>550</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th># 70/1C</th>
</tr>
</thead>
<tbody>
<tr>
<td>001 (h)</td>
</tr>
<tr>
<td>010 (h)</td>
</tr>
<tr>
<td>020 (h)</td>
</tr>
<tr>
<td>030 (h)</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th># 70/1D</th>
</tr>
</thead>
<tbody>
<tr>
<td>000 (h)</td>
</tr>
<tr>
<td>010 (h)</td>
</tr>
<tr>
<td>020 (h)</td>
</tr>
<tr>
<td>030 (h)</td>
</tr>
</tbody>
</table>

Same as above
4.4 Identifying Faults in the DSC Unit

4.4.1 Preparations

No preparations are required to test the DSC.

4.4.2 Troubleshooting flowchart

Figure 4-11 shows a flowchart for DSC unit test system processing. This flowchart shows the actual processing flow.

When operating the test system, perform troubleshooting by checking the current processing on the flowchart.
<DSC TEST>

Selection of test mode:

0: ALL CHECK
1: B/W FM CPU R/W
2: B/W TEST PATTERN (SYNC)
3: B/W TEST PATTERN (ASYNC)
4: R/W LIP TEST PATTERN
5: COLOR FM RAM R/W
6: CAL TEST PATTERN (R)
7: CAL TEST PATTERN (THETA)
8: COLOR FRIP TEST PATTERN
9: COLOR LIP TEST PATTERN
10: END

B/W FMA0-1, FMBO-1 R/W check
B/W DSC test pattern check
B/W LIP test pattern check
Color FMA0 2, FMBO 2 R/W check
Color calculator test pattern check
RIP test pattern check
Color LIP test pattern check
RETURN

B/W FMA0 R/W check
RETURN

DSC input system rate synchronization test pattern check
DSC input system rate synchronization test pattern check
RETURN

RETURN

Color FMA0 R/W check
RETURN

Sampling address and r-direction and b-direction threshold check
RETURN

RIP GA test pattern check
RETURN

The DSC tests are completed, and the screen returns to the main menu.

Figure 4-11
4.4.3 Criteria

This section describes the criteria for normality or abnormality, based on the messages displayed on the screen, for the results of tests performed according to the flowchart.

If any test item does not meet the requirements, it is rejected.
START

Characters displayed

NO

YES

Faulty PWB: CPU B & W DSC

END

Frame memory error.
Faulty PWB: B & W DSC (CPU)

OK

1. B/W FM RAM R/W

NG

2. B/W TEST PATTERN (SYNC)

3. B/W TEST PATTERN (ASYNC)

NG

Sampling address error.
Faulty PWB: B & W DSC

OK

The DSC unit is normal. No signal is sent from the T/R unit.

NG

Raster address or transmission stage count error.
Faulty PWB: B & W DSC RPG/TR CONT

OK

4. B/W LIP TEST PATTERN

NG

An error in LIP or between LIP and gamma RAM.
Faulty PWB: B & W DSC

A

No error in LIP and subsequent units

END

Figure 4-12
No. 2D730-136E

A

Characters displayed

NO

YES

Faulty PWB: CPU B & W DSC

Faulty PWB: CFM DSC

NG

Frame memory error.
Faulty PWB: CFM DSC

OK

FM RAM R/W

Faulty PWB:

CPM (CPU)

5. COLOR

NG

Sampling address error.
Faulty PWB:

CFM DSC

OK

6. CAL

TEST PATTERN (R)

Minor error

NG

The DSC unit is normal,
No signal is sent from the CFM unit.

END

OK

7. CAL TEST

PATTERN

(THETA)

Raster address error
Faulty PWB:

CFM DSC

RPG/TR CONT
No error in RIP and SUBsequent units

Figure 4-13
Note: If the gradation is abnormal, proceed to the test of the next item. If the gradation becomes normal at item "n", it shows that the path of the signal at item "n-1" not included in the signal of item "n" is abnormal.

<table>
<thead>
<tr>
<th>Abnormal Item &quot;n&quot;</th>
<th>Normal Item &quot;n-1&quot;</th>
<th>Faulty PWB</th>
</tr>
</thead>
<tbody>
<tr>
<td>2 3</td>
<td>4</td>
<td>B &amp; W DSC</td>
</tr>
<tr>
<td>4</td>
<td>---</td>
<td>B &amp; W DSC</td>
</tr>
<tr>
<td>6 7</td>
<td>8</td>
<td>CFM unit, CFM DSC</td>
</tr>
<tr>
<td>8</td>
<td>9</td>
<td>CFM DSC</td>
</tr>
<tr>
<td>9</td>
<td>---</td>
<td>CFM DSC, RGB CONVERTER</td>
</tr>
</tbody>
</table>
## Image mode at the time of DSC test

<table>
<thead>
<tr>
<th>No.</th>
<th>Pattern</th>
<th>TV display</th>
<th>Display mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>B/W TEST PATTERN (SYNC)</td>
<td><img src="image1" alt="TV display" /></td>
<td>M + B</td>
</tr>
<tr>
<td>3</td>
<td>B/W TEST PATTERN (ASYNC)</td>
<td><img src="image2" alt="TV display" /></td>
<td>B-Dual</td>
</tr>
<tr>
<td>4</td>
<td>B/W LIP TEST PATTERN</td>
<td><img src="image3" alt="TV display" /></td>
<td>B-Dual</td>
</tr>
<tr>
<td>6</td>
<td>CAL TEST PATTERN (R)</td>
<td><img src="image4" alt="TV display" /></td>
<td>M + B</td>
</tr>
<tr>
<td>7</td>
<td>CAL TEST PATTERN (THETA)</td>
<td><img src="image5" alt="TV display" /></td>
<td>B-Dual</td>
</tr>
<tr>
<td>8</td>
<td>COLOR RIP TEST PATTERN</td>
<td><img src="image6" alt="TV display" /></td>
<td>B-Dual</td>
</tr>
<tr>
<td>9</td>
<td>COLOR LIP TEST PATTERN</td>
<td><img src="image7" alt="TV display" /></td>
<td>B-Dual</td>
</tr>
</tbody>
</table>
[No. 0] CPU test menu

Application:

The DSC test mode is selected.
(See photo 4.4-1)

Outline:

The DSC function test is selected.

0 ALL CHECK

→ The following checks are sequentially performed:
B/W FM CPU R/W, B/W TEST PATTERN (SYNC), B/W TEST PATTERN (ASYNC), B/W LIP TEST PATTERN, COLOR FM CPU R/W, CAL TEST PATTERN (R), CAL TEST PATTERN (THETA), COLOR RIP TEST PATTERN, COLOR LIP TEST PATTERN

1 B/W FM CPU R/W

→ B/W FMA, FMB are checked.

2 B/W TEST PATTERN (SYNC)

→ The sampling address is checked by the rate synchronization test pattern.

3 B/W TEST PATTERN (ASYNC)

→ The raster address is checked by the rate asynchronization test pattern.

4 B/W LIP TEST PATTERN

→ Determining whether the error position is in the system preceding the B/W DSC unit or in the system following the B/W DSC unit.

5 COLOR FM CPU R/W

→ COLOR FMAO to 2, FMBO to 2 R/W is checked.
6 CAL TEST PATTERN (R)

→ The sampling address and r-direction thresholds are checked.

7 CAL TEST PATTERN (THETA)

→ The raster address and r-direction and θ-direction thresholds are checked.

8 COLOR RIP TEST PATTERN

→ The RTP test pattern is checked.

9 COLOR LIP TEST PATTERN

→ Determining whether the error position is in the system preceding the color DSC unit or in the system following the color DSC unit.

11 END

→ The DSC tests are completed, and the screen returns to the main menu.

Procedure:

Enter the test number.

Example ...

B/W TEST PATTERN (SYNC)


Caution:

Characters should be displayed on the screen. If no characters are displayed, either the CPU, B&W DSC, or CFM DSC PCB is abnormal.
Application:

FM memory IC operation is checked.

Outline:

Data is written into RAM, then read. If the read data does not match the written data, the address is displayed.

Procedure:

The CPU carries out the test automatically, and displays the message in 1):

1) **** B/W FM RAM CHECK ****

2) The result is displayed sequentially for each RAM.

3) When FMA0 is completed, FMA1 and FMB0 are checked in that order.

4) When the test results are normal, the image shown in photo 4.4-2 is displayed.

When \( \square \) is pressed, it proceeds to the next check (B/W TEST PATTERN (SYNC)).

When \( \rightarrow \) is pressed, the DSC test menu is displayed.

The error address and the comparison result are displayed. A bit which is set to 1 is an error bit in the RAM.
If the [F] key is pressed, the next address is tested.

When [C] is pressed, this check is terminated.

The operations when all addresses have been tested are the same as the operations described in 4).
[No. 2] B/W TEST PATTERN (SYNC)

Application:

The sampling address is checked, and an error position in the DSC unit is discriminated from one in the T/R unit.

Outline:

Generate the rate synchronization test pattern in the FM-IN SC, and visually check whether the sampling address is normal.

Procedure:

The visual check procedures are as follows:

1) When the image shown in photo 4.4-3 is displayed, the sampling address is normal.

2) When the test results are abnormal:

3) When \[ 	ext{[button]} \] is pressed, the operation proceeds to the next check (B/W TEST PATTERN (ASYNC)).

When \[ 	ext{[button]} \] is pressed, the DSC test menu is displayed.

Note:

When both check results, B/W TEST PATTERN (SYNC) and B/W TEST PATTERN (ASYNC), are normal, the DSC unit is normal. No signal is sent from the Receiver.
Flow chart of B/W TEST PATTERN (SYNC) signal
[No. 3] B/W TEST PATTERN (ASYNC)

Application:

The raster address and the transmission stage count are checked, and an error position in the DSC unit is discriminated from one in the T/R unit.

Outline:

Generate a test pattern asynchronous with the rate in the FM-IN SC to check visually whether the raster address is normal.

Procedure:

The visual check procedures are as follows:

1) The image shown in photo 4.4-4 is displayed.

   If no raster displacement occurs, the raster address is normal.

2) When the test results are abnormal:

   • If an image different from that shown in photo 4.4-4 is displayed, PRG/TR CONT and B&W DSC are abnormal.

   • When nothing is displayed, the error is in the B & W DSC.
3) When is pressed, the operation proceeds to the next check (B/W LIP TEST PATTERN).

When is pressed, the DSC test menu is displayed.

Note:

When both check results, B/W TEST PATTERN (ASYNC) and B/W TEST PATTERN (SYNC), are normal, the DSC unit is normal. No signal is sent from the Receiver.
Flow chart of B/W TEST PATTERN (ASYNC) signal
[No. 4] B/W LIP TEST PATTERN

Application:

The B/W LIP interpolation operation is checked, and an error position in the DSC unit is discriminated from one in subsequent units.

Outline:

Enter the test pattern in the LIP of the FM-OUT GA, and visually check whether interpolation is performed normally.

Procedure:

The visual check procedures are as follows:

1) The image shown in photo 4.4-5 is displayed.

2) When the test result is normal, the FM-OUT GA and subsequent systems are normal.

3) When the test result is abnormal:
   - When interpolation is not performed normally, the error is in the FM-OUT GA
   - When no pattern is displayed or the gradation is incorrect, the error is in the system from the FM-OUT GA to the gamma RAM.

4) When \( \rightarrow \) is pressed, the operation proceeds to the next check (COLOR FM RAM R/W).

When \( \rightarrow \) is pressed, the DSC test menu is displayed.
Note:

If the check result is normal and no pattern is displayed when B/W TEST PATTERN (SYNC) or B/W TEST PATTERN (ASYNC) is checked, the error is in the system from the FM-IN SC to the FM-OUT.
Flow chart of B/W LIP TEST PATTERN signal
[No. 5] COLOR FM CPU R/W

Application:

FM memory IC operation is checked.

Outline:

Data is written into RAM, then read. If the read data does not match the written data, the address at which the discrepancy has occurred is displayed.

Procedure:

The CPU carries out the test automatically, and displays the message in 1):

1) **** CFM FM RAM CHECK ****
2) The result is displayed sequentially for each RAM.
3) When FMA0 is completed, FMA1 and FMA3 are checked in that order.
4) When the test result is normal, the image shown in photo 4.4-6 is displayed.

When is pressed, the operation proceeds to the next check (CAL TEST PATTERN (R)).

When is pressed, the DSC test menu is displayed.

If COLOR FM CPU R/W is selected, the DSC test menu is displayed when the key is pressed.

5) The error address and the comparison result are displayed. A bit which is set to 1 is an error bit in the RAM.
• If the [F] key is pressed, the next address is tested.

When [C] is pressed, this check is terminated.

The operations when all the addresses have been tested are the same as the operations in 4).
[No. 6] CAL TEST PATTERN (R)

Application:
To check the sampling address, and to distinguish an error position in the DSC unit from one in the CFM unit.

Outline:
Enter the test pattern from the CALCULATOR, and visually check whether the sampling address and the threshold of the interpolation circuit to prevent r-direction return (RIP) are normal.

Procedure:
The visual check procedures are as follows:

1) If the image shown in photo 4.4-7 is displayed, they are normal.

   r-direction

   θ-direction

2) If the test results are abnormal:
   - If an image different from that shown in figure 4.4-7 is displayed, the CFM DSC is abnormal.
- If the pattern is otherwise abnormal, the error is in the CALCULATOR PWB or CPM DSC PWB.

- If no pattern is displayed, the error is in the CALCULATOR PWB, CPM DSC PWB, or RGB CONV PWB.

3) When \([\text{[}\text{]}\) is pressed, the system proceeds to the next check (CAL TEST PATTERN (THETA)).

When \([\text{[}\text{]}\) is pressed, the DSC test menu is displayed.

Note:

If both check results, CAL TEST PATTERN (R) and CAL TEST PATTERN (THETA), are normal, the DSC unit is normal. No signal is sent from the CPM unit.
Flow chart of CAL TEST PATTERN (R) signal
[No. 7] CAL TEST PATTERN (THETA)

Application:

To check the raster address, and to distinguish an error position in the DSC unit from one in the CFM unit.

Outline:

Enter the test pattern from the CALCULATOR, and visually check whether the raster address and the thresholds of the interpolation circuit to prevent r-direction return (RIP) and the interpolation circuit to prevent θ-direction return (WIP) are normal.

Procedure:

The visual check procedures are as follows:

1) If the image shown in photo 4.4-8 is displayed, they are normal.

```
  r-direction
  \_\_/\
  \  / \n \  /  
\_\_/\_
  θ-direction
```

2) If the test results are abnormal:

- If an image different from that shown in figure 4.4-8 is displayed, the CFM DSC and RPG/TR CONT are abnormal.
If the pattern is otherwise abnormal the error is in the CALCULATOR PWB or CFM DSC PWB.

If no pattern is displayed, the error is in the CALCULATOR PWB, CFM DSC PWB or RGB CONV.

3) When is pressed, the
proceeds to the next check (COLOR RIP TEST PATTERN).
When is pressed, the DSC test menu is displayed.

Note:
If both check results, CAL TEST PATTERN (THETA) and CAL TEST PATTERN (R) are normal, the DSC unit is normal. No signal is sent from the CFM unit.
Flow chart of CAL TEST PATTERN (THETA) signal
[No. 8] COLOR RIP TEST PATTERN

Application:

The test checks whether the error position is in the system preceding the CFM DSC FWB or in the system following the CFM-I/O FWB.

Outline:

Enter the test pattern in the RIP of the FM-IN SC to visually check whether the pattern is displayed.

Procedure:

The visual check procedures are as follows:

1) The image shown in photo 4.4-9 is displayed. When the pattern is displayed, the system is normal.

2) When the test results are normal, the FM-IN SC and subsequent systems are normal.

3) When the test results are abnormal, the CFM DSC FWB or subsequent systems are faulty.

4) When \( \square \) is pressed, the operation proceeds to the next check (COLOR RIP TEST PATTERN).

When \( \square \) is pressed, the DSC test menu is displayed.
Signal chart of COLOR RIP TEST PATTERN signal
[No. 9] COLOR LIP TEST PATTERN

Application:

Enter the test pattern in the LIP of the FM-OUT GA, and an error position in the DSC unit is discriminated from one in subsequent systems.

Outline:

Enter the test pattern in the COLOR LIP G.A, and visually check whether the interpolation is performed normally.

Procedure:

The visual check procedures are as follows:

1) The image shown photo 4.4-10 is displayed.

2) When the test result is normal:

- When no test pattern from the CALCULATOR PWB is displayed, the error is in the DSC unit from the CALCULATOR PWB to the FM-OUT GA

- When no test pattern from the FM-IN SC is displayed, the error is in the DSC unit from the FM-IN SC PWB to the FM-OUT GA
3) When the test results are abnormal:

- When interpolation is not performed normally, the error is in the FM-OUT GA.

- When no pattern is displayed or the color tone is incorrect, the error is in the CPM DSC PWB or RGB CONVERTER PWB subsequent to the FM-OUT GA.

4) If ALL CHECK or COLOR LIP TEST PATTERN is selected, the DSC test menu is displayed when the key is pressed.
Flow chart of COLOR LIP TEST PATTERN signal
4.5 Identifying Faults in the T/R Unit

4.5.1 Preparations

Ultrasonic jelly is required in the items listed below:

(1) T/R test item No. 4 R-channel check (CONVEX)

(2) T/R test item No. 5 T-channel check (CONVEX)

4.5.2 Fault diagnosis flow chart

Figure 4.5-1 shows the processing for the T/R test.
<T/R TEST>

![Diagram of test mode selection]

Figure 4.5-1
Troubleshooting procedure

START

R/W check of command RAM

OK → R/W check of BRI RAM

OK → R-CHANNEL check

OK → T-CHANNEL check

OK → DELAY TIME check

END

[Suspected PWB]

NG → RPG/TR CONT PWB

NG → RPG/TR CONT PWB

NG → PROBE SELECTOR PWB PULSER PWB

NG → R-DELAY PWB

NG → PROBE SELECTOR PULSER PWB

NG → R-DELAY PWB

If more than one PWB, identify the defective PWB by checking the patterns of test results.

* The RAM check function (command RAM, BRI RAM) does not check whole of RPG/TR CONT PWB.
There is a slight chance that RPG/TR CONT is defective, in addition to the PWBs with *.

Notes:
1. Prior to replacing PWBs, check that cables are connected correctly and are not cut off.
2. The DVAF/RECEIVER cannot be checked using the test program. These PWBs must be checked separately.
4.5.3 Criteria

[No. 1] T&R TEST MENU

Purpose:
T&R test menu selection

Outline:
Select the test for each block.

0 ALL CHECK
The following tests are executed sequentially.

1 T&R CONT RAM CHECK
The RAM for T/R CONT1 and 2 delay time data is checked for read and write.

2 DELAY CONT RAM CHECK
The RAM for DELAY CONT delay time data is checked for read and write.

x R-CHANNEL CHECK (RESERVE)

4 R-CHANNEL CHECK (CONVEX)
Each channel of the convex reception system is checked.

5 T-CHANNEL CHECK (CONVEX)
Each channel of the sector transmission system is checked.

6 DELAY TIME CHECK (CONVEX)
The sector transmission - reception delay time is checked.

7 CHECK COUNT SET
The T&R test is completed. The [No. 1] menu is displayed.

Procedure:

Enter the number of the test to be executed.

Example: R-CHANNEL CHECK (CONVEX)

Press the [4] and keys in that order.
No. 2D730-136E

[No. 2] T/R CONT RAM CHECK

Purpose:

Operation check for T/R delay time RAM

Outline:

Data is written into the RAM. The data is read and compared with the written data. If they do not match each other, the address and data are displayed.

Procedure:

The CPU executes the test automatically and displays the message below:

1) "***T/R CONT RAM CHECK***" is displayed.

2) The result is displayed for each RAM.

3) When the test result is normal, the message in photo 4.5-2 is displayed.

   When the key is pressed, the next check is executed.

   When the key is pressed, menu [No. 1] is displayed.

4) When the test result is abnormal, the abnormal address and the results of comparison are displayed.
When the [F] key is pressed, the next address is checked.

When the [C] key is pressed, the current RAM check is terminated.

After all the addresses are checked:

When the \[\rightarrow\] key is pressed, the next check is executed.

When the \[\leftarrow\] key is pressed, the [No. 1] menu is displayed.

The RAM containing the error address is faulty. Replace the RPG/TR CONT PWB.
[No. 3] DELAY CONT RAM CHECK

Purpose:
BRI RAM operation check

Outline:
Data is written into the RAM, then the data is read and compared with the written data. If they do not match each other, the address and data are displayed.

Procedure:
The CPU automatically executes the test and displays the message below:

1) "***DL CONT RAM CHECK***" is displayed.

2) The result is displayed for each RAM.

3) When the test result is normal:
   a) The message in photo 4.5-3 is displayed

   When the key is pressed, the next check is executed.

   When the key is pressed, menu [No. 1] is displayed.
4) When the test result is abnormal, the abnormal address and the result of comparison are displayed.

When the [F] key is pressed, the next address is checked.

When the [C] key is pressed, the current RAM check is terminated.

After all the addresses are checked:

When the (→) key is pressed, the next check is executed.

When the (←) key is pressed, the menu [No. 1] is displayed.

The RAM containing the error address is faulty. Replace the RPG/TR CONT PWB.
[No. 5] R-CHANNEL CHECK
(CONVEX)

Purpose:

Each channel of the reception system is checked by linear operation.

Outline:

The system sends an ultrasound beam from multiple channels near the specified channel of the reception system, and displays the reflected signals as a line on the monitor.

Procedure:

Visually check the display.

1) Connect the sector probe to the probe CNN.

SSA-340A ...... PVF-375MT
(CNN A)

2) Apply a sufficient amount of acoustic coupler to the probe in an even layer.

3) Acoustic power: 16

4) Check whether any channel of the reception system is faulty by watching the monitor display.

When the key is pressed, the next check is executed.
When the \( \rightarrow \) key is pressed, menu [No. 1] is displayed.

When the [SPACE] key is pressed, the first half and the second half of the channels are switched. (See the figure below.)

If the values of the STC controls are set too high, the brightness of the line of a faulty channel increases, making it difficult to detect faulty channels.

\[
\begin{array}{|c|c|}
\hline
\text{CH64} & \text{CH5} \\
\text{(CH124)} & \text{(CH65)} \\
\hline
\end{array}
\]

Examples:

Photo 4.5-4 shows an example of a normal result for channels 5 to 64.
Photo 4.5-5 shows an example of a normal result for channels 65 to 124.

For abnormal results, the defective ch is black.
[No. 6] T-CHANNEL CHECK  
(CONVEX)

Purpose:
The operation of each channel of the transmission system is checked.

Outline:
Sends channels one by one, receives the reflected signals with multiple elements, and displays the signals as a raster.

Procedure:
Visually check the monitor display.

1) Apply a sufficient amount of acoustic coupler to the probe.

2) Acoustic power: 16

3) Observe the monitor display to determine whether each channel for transmission is defective.

When is turned ON, the system proceeds to the next check.

When is turned ON, it enters the [No. 1] menu display.

When (SPACE) is turned ON, the first-half and second-half CHs are switched.
Example

Photo 4.5.6 shows an example of normal 5 to 64 ch and photo 4.5.7 shows an example of normal 64 to 124 ch.

The marker on the raster is displayed every 10 channels.

If the channel for the transmission system is defective, the raster corresponding to the channel is black.

The gain dial has no effect, so adjust the STC to clarify the black area.
[No. 7] DELAY TIME CHECK (CONVEX)

Purpose:
Checking the total transmission and reception delay time of all the channels.

Outline:
The delay data is generally the scan delay data. Only the channel which is specified for transmission and reception is turned ON, and the pattern generated by the initial echo is compared with the graphic pattern calculated by the CPU.

Procedure:
Visually check the monitor display.

1) Connect the convex probe to the probe CNN.

2) Check whether any channel of the transmission system is faulty by watching the monitor display.

Pressing [SPACE] alternates the delay-time display of the DVAF steps between the even-numbered and odd-numbered steps.
3) Press the [DEL] key to terminate the delay time check. Figure 4.5.19 is displayed.

When the \( \leftarrow \) key is pressed, the next menu is displayed.

When the \( \rightarrow \) key is pressed, the menu No. 1 is displayed.

4) Adjust the STC controls so that a narrowest echo pattern is generated.

Photo 4.5-10
4.5.4 Supplement

(1) COMMAND RAM CHECK

Write data onto the command RAM on the RPG/TR CONT and read the data. The read data must be identical to the written data.

Figure 4.5-1
(2) DL CONT RAM CHECK

Write data onto BRI RAM on the DL CONT and read the data. The read data must be identical to the written data.

Figure 4.5-2
(3) T/R R channel check (convex)

For the R channel check (convex), a reception check is performed during convex operation. It is possible to identify possible defective PWBs if the R channel check and reception check interpolate each other. This check is based on transmission from multiple elements and reception by a single element. The figure below outlines this operation. Probe channels 1 to 4 and 125 to 128 cannot be checked due to limitations.

Note: The number of transmission channels changes from 9 to 47 depending on the raster.

Figure 4.5-3

If one of the reception channels is defective, the corresponding raster is cut off. Display is as follows:

Figure 4.5-4
(4) T/R T channel check (convex)

For the T channel check (convex), a transmission check is performed during convex operation. In combination with the R channel check (convex), follow the flowchart of figure 4.5.2-3. This check is based on transmission from a single element and reception by multiple elements. The figure below outlines this operation. Probe channels 1 to 4 and 125 to 128 cannot be checked due to limitations.

Note: The number of transmission channels changes from 9 to 47 depending on the raster.

If one of the reception channels is defective, the corresponding raster is cut off. Display is as follows:

Figure 4.5-5

Figure 4.5-6
(5) T/R DELAY TIME CHECK (CONVEX)

In this check, only one channel is turned ON for transmission and reception, and the initial echo pattern is displayed. This pattern is a delay track for the specified channel when scanning is performed for lines 0 to 239.

Check whether the initial echo pattern matches the graphic pattern. If they do not match each other, there is a fault in the system.

(Example of convex)

Figure 4.5-7
4.6 Identifying Faults in the FFT Unit

4.6.1 Preparatory work

Set the audio VR (L,R) to MIN.

4.6.2 Flowchart for identifying faults

(1) Operating procedure

Perform visual comparison check between the expected value pattern displayed on the monitor screen and the Doppler image resulting from the FFT of test signals.

<FFT TEST>

START

Test mode selection

[0]

[1] PH.D OSC CHECK

A test signal is input to the PHASE DETECTOR

[2] FORWARD FLOW CHECK

A forward flow test signal is input to the FFT (digital section).

[3] REVERSE FLOW CHECK

A reverse flow test signal is input to the FFT (digital section).

[4] BLANK CHECK

A no flow test signal is input to the FFT (digital section).

[6]

It returns to the test system menu.

It proceeds to the next step (CFM).

Figure 4.6-1
(2) Troubleshooting expected failures of PWRs

Figure 4.6-2
Failure of the PHASE DETECTOR, FFT I/O or FFT/CONT/AUDIO

Figure 4.6-3
4.6.3 Criteria

Expected value pattern
FFT spectrum

(Normal)
Figure 4.6-4

[No. 1] PH.D OSC CHECK

Application:

To check whether the PHASE DETECTOR PWB and the subsequent PWBs operate normally and to distinguish error position from one in the prestige (T/R unit).

Outline:

The input stage of the PHASE DETECTOR is connected to the test signal generating circuit. The FFT spectrum for this signal is displayed on the TV monitor and at the same time the expected value pattern is displayed graphically.

Perform visual check to judge whether it is normal or abnormal. Check if changing the GAIN to three different levels causes the signal to change to three sizes, large, middle and small, changing the brightness of the spectrum, mirror image, and degree of noise. (Note 2)

Procedure:

Check if the FFT spectrum to the test signal and the expected value pattern are displayed as shown in the figure 4.6-4.

Photo 4.6-1 HIGH GAIN

Photo 4.6-2 MIDDLE GAIN
[1] --- HIGH GAIN

[2] --- MIDDLE GAIN
(Initial state)

[3] --- LOW GAIN

To terminate visual check, press [4] and .

The PWB judged to be defective at the time of abnormality will be displayed.

Press to proceed to the next test.

Note 2:

The FFT spectrum does not match the expected value pattern exactly because the accuracy of the oscillator on the PHASE DETECTOR PWB differs from that of the oscillator on the RPG PWB. (Refer to the figure on the left.)

The FFT spectrum must be displayed within the range indicated by dotted lines in the figure above.
[No. 2] FORWARD FLOW CHECK

Application:

To check whether the FFT (digital signal processing) PWB and the subsequent PWBs operate normally, and to distinguish an error position from one in the prestage (analog unit).

Outline:

The test CAL signal is connected to the input of FFT. The FFT spectrum to this signal is displayed on the TV monitor and at the same time the expected value pattern is graphic-displayed. Perform visual check to judge whether it is normal or abnormal.

Check if changing the GAIN to three different levels causes the signal to change to three sizes, large, middle and small, changing the brightness of the spectrum and amount of harmonic noise.

Procedure:

Check that the FFT spectrum to the test signal and the expected value pattern are displayed as shown in the figure 4.6-5 and Photos 4.6-4, 4.6-5 and 4.6-6.

Note: Even if the FFT spectrum and the expected value pattern do not match, be sure to switch the GAIN to carry out the check again.

- If nothing is displayed, the operation system is not working.
- If they are displayed symmetrically, the RE/IM will not be separated.
- If many of them are displayed, the digital unit is malfunctioning.
• If there are white spots or noise, the digital unit is malfunctioning.

Perform the same check with a different GAIN level.

[1] [ ] --- HIGH GAIN
[2] [ ] --- MIDDLE GAIN (Initial state)
[3] [ ] --- LOW GAIN

To terminate visual check, press [4] and [ ].

The PWB judged to be defective at the time of abnormality will be displayed.

Press [ ] to proceed to the next test.
[No. 3] REVERSE FLOW CHECK

The application and outline of this are the same as those for [No. 2] FORWARD FLOW CHECK. Check if the FFT spectrum and the expected value pattern are displayed in the reverse flow direction.

(Normal)
Figure 4.6-6

Photo 4.6-7 HIGH GAIN

Photo 4.6-8 MIDDLE GAIN
Photo 4.6-9 LOW GAIN

[No. 4] BLANK CHECK

Same as No. 2 FORWARD FLOW CHECK. The test signal does not have velocity components. Confirm that nothing is displayed.

(Normal)
Figure 4.6-7

Photo 4.6-10 HIGH GAIN
Photo 4.6-11  MIDDLE GAIN

Photo 4.6-12  LOW GAIN
When starting this test system, the normal PANEL SW does not operate, and quantitative evaluation is performed with the conditions limited to the three GAIN levels.

The changes of the FFT spectrum display can be checked by operating the PANEL SW as required as described below.

(1) PH.D OSC signal check (with the probe of 3.75MHZ and REFERENCE = M)

Turn off the test. Place it in the PATCH input mode. Write the following data.

R204000  W 1
R224000  W 80
R224044  W 9  (To release, write W 0.)
R204000  W 0

Now, the PANEL SW can be operated so changes in the image can be checked with the SW functioning. (To release it, turn off the power or write R224044 W 0.)

Notes: 1. This check can be applied to the COLOR (BDF, MDF) as well as the PW Doppler.

2. The setting can be changed as required with the PANEL SW. Saturation and too much narrowing prevent changing some combinations.

(2) FFT CAL signal check

Turn [ON] FFT CAL using the service function.

Now, the PANEL SW can be operated to permit checking the operation of the switch. (However, the analog unit control SW = FFT GAIN is not working.)
4.7 Identifying Faults in the CFM Unit

4.7.1 Preparatory work

To check the system using the test pattern, set the STC-volume to the minimum.

4.7.2 Flowchart for identifying faults

2-1 Procedure

Perform self-diagnosis and visual check of the Z80 of the CFM unit by the commands of the HOST CPU (68000) by the following procedure.
2-2 Faults-identifying path

(1) Self-diagnostic path

(a) LB test RAM, test

ADC/LB/CAL → FIL/CORR

The shaded part (B) is to be checked.

(b) LB/CAL test

ADC/LB/CAL → FIL/CORR

The shaded parts (C) are to be checked.
(c) LB/CORR/CAL test

The shaded parts (□) are to be checked.

(d) LB/FIL/CORR/CAL test

The shaded parts (□) are to be checked.
(2) Visual check path

(a) CAL test patterns 1, 2 and 3

(b) LB test pattern 1 and 2

The shaded parts ( ) are to be checked.
4.7.3 Criteria

This subsection describes the criteria for determining whether the results of tests carried out according to the flowchart in 4.7.2 are abnormal based on messages displayed on the screen.

Items which do not match the normal data shown here are faults and faulty portions.
[No. 0] CFM test menu

Purpose:

Selecting the test mode for CFM
(Refer to figure 4.7-1.)

Outline:

Select tests by function of CFM.

0 ALL CHECK

-> Carry out test items 1 to 16 sequentially.

1 LB SELF TEST

-> Carry out self diagnosis of the LB test RAM.

2 LB/CAL SELF TEST

-> Carry out self diagnosis of LB/CAL.

3 LB/CORR/CAL SELF TEST

-> Carry out self diagnoses of LB/CORR/CAL.

4 LB/FIL/CORR/CAL SELF TEST

-> Carry out self diagnoses of LB/FIL/CORR/CAL.

5 to 10 LB/CAL CHECK

-> Display the test pattern for the LB/CAL path and visually check it.

11 to 16 LB/FIL/CORR/CAL

-> Display the test pattern for the LB/FIL/CORR/CAL path and visually check it.
[No.1] LB SELF TEST

Purpose:

Self diagnosis of the LB test RAM is carried out.

Outline:

R/W is performed from/to the LB test RAM to diagnose the LB test RAM by comparing written data with read data.

Procedure:

The CPU automatically performs the test and displays the results on the monitor.

<1> When the test is normal

The screen appears as shown in photo 4.7-2 after a transit image has been displayed.

When ▼ is entered, the system proceeds to the next check.

When ▼ is entered, the menu is displayed.

<2> If the test result is abnormal

An error code is displayed.

Refer to 4.7.4 "Results of the diagnostic tests" to identify the defective section.
[No.2]  LB/CAL SELF TEST

Purpose:

Self diagnosis of LB/CAL is performed.

Outline:

Enter data into CAL via the path that has passed through the FIL/CORR and compare the CAL output buffer value with the expected value obtained by simulation.

Procedure:

The CPU automatically performs the test and displays the results on the monitor.

<1> When the test is normal

The screen appears as shown in photo 4.7-3 and then displays the test results as shown in photo 4.7-4.

When $\square$ is entered, the system proceeds to the next check.

When $\Rightarrow$ is entered, the menu is displayed.

<2> If the test result is abnormal

An error code is displayed. Refer to 4.7.4 "Results of the diagnostic tests" to identify the defective section.
[No. 3] LB/CORR/CAL SELF TEST

Purpose:
Self diagnoses of the LB/CORR/CAL is performed.

Outline:
Enter data into CAL via the path that has passed through the FILTER and compare the CAL output buffer value with the expected value obtained by simulation.

Procedure:
The CPU automatically performs the test and displays the results on the monitor.

<1> When the test is normal

The screen appears as shown in photo 4.7-5 and displays the test result as shown in photo 4.7-6.

When \[ \text{[ Enter]} \] is entered, the system proceeds to the next check.

When \[ \text{[ Previous Menu]} \] is entered, the menu is displayed.

<2> If the test result is abnormal

An error code is displayed. Refer to 4.7.4 "Results of the diagnostic tests" to identify the defective section.
[No. 4] LB/FILL/CORR/CAL SELF TEST

Purpose:
Self diagnosis of the LB/FILL/CORR/CAL is performed.

Outline:
Enter the data that has passed through the path of the LB/FILL/CORR/CAL into CAL and compare the CAL output buffer value with the expected value obtained by simulation.

Procedure:
The CPU automatically performs the test and displays the result on the monitor.

<1> When the test is normal
The screen appears as shown in photo 4.7-7 and displays the test result as shown in photo 4.7-8.
When is entered, the system proceeds to the next check.
When is entered, the menu is displayed.

<2> If the test result is abnormal
An error code is displayed. Refer to 4.7.4 "Results of the diagnostic tests" to identify the defective section.
[No. 5] LB/CAL visual check

Purpose:

The defective section on the ADC/LB/CAL PWB is identified.

Outline:

The test pattern that has passed through the FIL/CORR is displayed on the monitor to diagnose the LB/CAL section.

Procedure:

Visually check the test pattern displayed on the monitor.

<1> When the test is normal

The screen appears as shown in photo 4.7-9 for the LB/CAL CHECK (BDF L).

When ☑ is turned ON, the system proceeds to LB/CAL CHECK (BDF M).

When ☐ is turned ON, the menu is displayed.

<2> If the test is abnormal

Refer to 4.7.4 "Results of the diagnostic tests" to identify the defective section.
[No 6] LB/CAL CHECK (BDF M)  
(Normal example: photo 4.7-10)

[No 7] LB/CAL CHECK (BDF H)  
(Normal example: photo 4.7-11)

[No 8] LB/CAL CHECK (MDF M)  
(Normal example: photo 4.7-12)

[No 9] LB/CAL CHECK (MDF H)  
(Normal example: photo 4.7-13)

[No 10] LB/CAL CHECK  
(BDF/MDF L)  
(Normal example: photo 4.7-14)

The checks above are the same.
Photo 4.7-11

Photo 4.7-12
[No. 11] LB/FILL/CORR/CAL CHECK

Purpose:

The defective section on the FILL/CORR PWB is diagnosed.

Outline:

The test pattern that has passed through the LB/FILL/CORR/CAL is displayed on the monitor. The defective section is diagnosed taking into consideration the results of LB/CAL CHECK.

Procedure:

Visually check the test pattern displayed on the monitor.

<1> When the test is normal

The screen appears as shown in photo 4.7-15 for the LB/FILL/CORR/CAL (BDFL).

When \( \Box \) is turned ON, the system proceeds to LB/FILL/CORR/CAL (BDFM).

When \( \Box \) is turned ON, the menu is displays.

<2> If the test is abnormal

Refer to 4.7.4 "Results of the diagnostic tests" to identify the defective section.
[No. 12] LB/FILL/CORR/CAL CHECK (BDFM)
(Normal example: photo 4.7-16)

[No. 13] LB/FILL/CORR/CAL CHECK (BDFH)
(Normal example: photo 4.7-17)

[No. 14] LB/FILL/CORR/CAL CHECK (MDF)
(Normal example: photo 4.7-18)

[No. 15] LB/FILL/CORR/CAL CHECK (MDF)
(Normal example: photo 4.7-19)

[No. 16] LB/FILL/CORR/CAL CHECK (BDF/MDF)
(Normal example: photo 4.7-20)

The operation for the above is the same.
### 4.7.4 Results of the diagnostic tests

#### (1) Definition of error codes of self-diagnosis

<table>
<thead>
<tr>
<th>Description of error</th>
<th>Error code</th>
</tr>
</thead>
<tbody>
<tr>
<td>Normal</td>
<td>00</td>
</tr>
<tr>
<td>LB test RAM abnormal</td>
<td>01</td>
</tr>
<tr>
<td>LB/CAL v abnormal</td>
<td>41</td>
</tr>
<tr>
<td>LB/CAL P abnormal</td>
<td>42</td>
</tr>
<tr>
<td>LB/CAL σ abnormal</td>
<td>44</td>
</tr>
<tr>
<td>LB/FIL/CORR/CAL v abnormal</td>
<td>88</td>
</tr>
<tr>
<td>LB/FIL/CORR/CAL P abnormal</td>
<td>90</td>
</tr>
<tr>
<td>LB/FIL/CORR/CAL σ abnormal</td>
<td>A0</td>
</tr>
<tr>
<td>LB/CORR/CAL v abnormal</td>
<td>48</td>
</tr>
<tr>
<td>LB/CORR/CAL P abnormal</td>
<td>50</td>
</tr>
<tr>
<td>LB/CORR/CAL σ abnormal</td>
<td>60</td>
</tr>
</tbody>
</table>
### (2) Example

<table>
<thead>
<tr>
<th>Error code</th>
<th>PWB name</th>
<th>Details of fault</th>
<th>Name of the self-diagnostic test applied</th>
</tr>
</thead>
<tbody>
<tr>
<td>01</td>
<td>MTI-CONT</td>
<td>(1) Z80 I/F section with LB/CAL abnormal (Location: 0S, 0R, 0T, 0Q)</td>
<td>LB test RAM test</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(2) Z80 and Z80 peripheral (ROM, RAM) abnormal (Location: 7T, 3S, 5T etc.)</td>
<td></td>
</tr>
<tr>
<td>ADC/LB/CAL</td>
<td></td>
<td>(1) Test RAM abnormal (Location: 12G, 12F and 12E)</td>
<td></td>
</tr>
<tr>
<td>41 (Note 1)</td>
<td>MTI-CONT</td>
<td>(1) Control unit abnormal (Location: 3J, 2L, 2M, 2J, 2H, 1L, 1J, 1H, 2C, 1D, 0D etc.)</td>
<td>LB/CAL test</td>
</tr>
<tr>
<td></td>
<td>ADC/LB/CAL</td>
<td>(1) Operation ROM table section (circuit diagram page 10/14) abnormal</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>(2) CAL output buffer section Z80 I/F defective (Location: B6K, 7G, 6J, 8G, 6H, B5F, B5E)</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>(3) CAL output buffer RAM abnormal (Location: 6G and 6F)</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>(4) CAL output buffer memory read/write control section abnormal (Circuit diagram page 13/14)</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>(5) Data number encode section (location B3P and 3N) and gradation cut control code (location B1R) abnormal</td>
<td></td>
</tr>
<tr>
<td></td>
<td>D &amp; D MOTHER</td>
<td>(1) MTI-CONT PWB, ADC/LB/CAL PWB mother board contact defective</td>
<td></td>
</tr>
<tr>
<td>42 (Note 1)</td>
<td>MTI-CONT</td>
<td>(1) MTI-CONT PWB, LB/CAL PWB mother board contact defective</td>
<td>LB/CAL test</td>
</tr>
<tr>
<td></td>
<td>ADC/LB/CAL</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>D &amp; D MOTHER</td>
<td></td>
<td></td>
</tr>
<tr>
<td>44 (Note 1)</td>
<td>MTI-CONT</td>
<td>Same as above</td>
<td>LB/CAL test</td>
</tr>
<tr>
<td></td>
<td>ADC/LB/CAL</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>D &amp; D MOTHER</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Error code</td>
<td>FWB name</td>
<td>Details of fault</td>
<td>Name of the self-diagnostic test applied</td>
</tr>
<tr>
<td>------------</td>
<td>----------</td>
<td>-----------------</td>
<td>----------------------------------------</td>
</tr>
<tr>
<td>48 (Note 2)</td>
<td>MTI-CONT</td>
<td>(1) Control unit abnormal (Location: 1Y, 1BB, 1AA, OCC, 3DD, ODD, 2DD, 2CC, 7D, 5B, OBB etc.)</td>
<td>LB/CORR/CAL test</td>
</tr>
<tr>
<td></td>
<td>FIL/CORR</td>
<td>(1) CORR section control PAL abnormal (Location: 4G, 4J, 4L, 5J, 5F, 3K, 3L) (2) Discrete logic around the above control PAL is abnormal (3) CORR Z-1 memory (location 8D and 7D) and Σ memory (location 7A to 7C and 8C) abnormal (4) Gate array (location 7K) abnormal (5) FILTER through gate (location 2W, 3V, 3W) operation defective</td>
<td></td>
</tr>
<tr>
<td></td>
<td>D &amp; D MOTHER</td>
<td>(1) Contact of the MTI CONT FWB, ADC/LB/CAL FWB FIL/CORR FWB with the mother board defective</td>
<td></td>
</tr>
<tr>
<td>50 (Note 2)</td>
<td>MTI-CONT</td>
<td>Same as above</td>
<td>LB/CORR/CAL test</td>
</tr>
<tr>
<td></td>
<td>FIL/CORR</td>
<td>Same as above</td>
<td></td>
</tr>
<tr>
<td></td>
<td>D &amp; D MOTHER</td>
<td>Same as above</td>
<td></td>
</tr>
<tr>
<td>60 (Note 2)</td>
<td>MTI-CONT</td>
<td>Same as above</td>
<td>LB/CORR/CAL test</td>
</tr>
<tr>
<td></td>
<td>FIL/CORR</td>
<td>Same as above</td>
<td></td>
</tr>
<tr>
<td></td>
<td>D &amp; D MOTHER</td>
<td>Same as above</td>
<td></td>
</tr>
<tr>
<td>88 (Note 3)</td>
<td>MTI-CONT</td>
<td>(1) Control unit defective (Location: 1Y. 1BB. 1AA. OCC. 3DD. ODD. 2DD. 2CC. 7D. 5B. OBB etc.)</td>
<td>LB/FIL/CORR/CAL test</td>
</tr>
<tr>
<td></td>
<td>FIL/CORR</td>
<td>(1) Control PAL abnormal (Location 4M, 4H, 4K, 4G, 4J, 4L, 3K, 3L, 5H, 5L, 5K, 5G, 5J, 5F, 6H) (2) Discrete logic around the above control PAL is abnormal (3) Z-1, Z-2 memory (location 8S, 8D, 8V and 8U) abnormal or coefficient memory (location 6S and 6R) abnormal (4) Gate array (location 5U) abnormal</td>
<td></td>
</tr>
<tr>
<td></td>
<td>D &amp; D MOTHER</td>
<td>(1) Contact of the MTI-CONT FWB, ADC/LB/CAL FWB, FIL/CORR FWB with the mother board defective</td>
<td></td>
</tr>
<tr>
<td>Error code</td>
<td>PWB name</td>
<td>Details of fault</td>
<td>Name of the self-diagnostic test applied</td>
</tr>
<tr>
<td>------------</td>
<td>----------</td>
<td>------------------</td>
<td>------------------------------------------</td>
</tr>
<tr>
<td>90 (Note 3)</td>
<td>MTI-CONT</td>
<td>Same as above</td>
<td>LB/FIL/ CORR/ CAL test</td>
</tr>
<tr>
<td></td>
<td>FIL/CORR</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>D &amp; D MOTHER</td>
<td></td>
<td></td>
</tr>
<tr>
<td>A0 (Note 3)</td>
<td>MTI-CONT</td>
<td>Same as above</td>
<td>LB/FIL/ CORR/ CAL test</td>
</tr>
<tr>
<td></td>
<td>FIL/CORR</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>D &amp; D MOTHER</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(Note 1): First, complete normally the LB test RAM test.
(Note 2): First, complete normally the LB test RAM test and LB/CAL test.
(Note 3): First, complete normally the LB test RAM test, LB/CAL test and LB/CORR/CAL test.
### (3) CAL test pattern

#### (a) CAL test pattern

<table>
<thead>
<tr>
<th>No.</th>
<th>Phenomenon</th>
<th>Faulty units</th>
<th>Relevant PWB</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>The character S is not displayed.</td>
<td>(1) CAL operation ROM table speed operation unit (Location: 1G, 1F, B2E, B1G, B1F, B5H, 6H, 5H, B6B, B5C, 10D, B8C, B6C, 8D, B8B, 8B)</td>
<td>LB/CAL</td>
<td>If the phenomena mentioned at the left occur together, the cause may be one of the following:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(2) CAL operation power ROM unit (Location: 6D, B6C, B11C, B12B) abnormal</td>
<td></td>
<td>• Pipe line lock is out of order.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>• The CAL output buffer read/write is out of order.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>• The MTI CONT control system is out of order.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>• No control signal has come from the PRG.</td>
</tr>
<tr>
<td>2</td>
<td>The dispersion display has no gradation.</td>
<td>(1) CAL operation ROM table speed operation unit (Location: 5B, 5D, BSC, B5D, 10E, B10B, B10C, 10B, B10E, 11E, 11D) abnormal</td>
<td>LB/CAL</td>
<td>MTI-CONT ADC/LB/CAL D &amp; D MOTHER</td>
</tr>
<tr>
<td>3</td>
<td>The character P is not displayed.</td>
<td>(1) CAL operation ROM table speed operation unit abnormal</td>
<td>LB/CAL</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>(2) CAL operation power ROM unit abnormal</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>The power display has no gradation.</td>
<td>(1) CAL operation power ROM unit abnormal</td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>The character V is not displayed.</td>
<td>(1) CAL operation ROM table speed operation unit abnormal</td>
<td>LB/CAL</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>(2) CAL operation power ROM unit abnormal</td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>The speed display has no gradation.</td>
<td>(1) CAL operation ROM table speed operation unit abnormal</td>
<td>LB/CAL</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>(2) CAL operation power ROM unit abnormal</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Note: When the number of MDF data is H, the characters SPV are not displayed.
(b) LB test pattern

Normal display should be checked with the CAL test pattern beforehand.

<table>
<thead>
<tr>
<th>No.</th>
<th>Phenomenon</th>
<th>Faulty units</th>
<th>Relevant PWB</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>• There is no gradation of dispersion display.</td>
<td>(1) LB section RAM (including initial value subtraction RAM) abnormal</td>
<td>ADC/LB/CAL</td>
<td>Perform self-diagnosis test.</td>
</tr>
<tr>
<td></td>
<td>• Dispersion display is not performed.</td>
<td>(2) FILTER section abnormal</td>
<td>FIL/CORR</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>(3) CORR section abnormal</td>
<td>FIL/CORR</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>(4) MTI-CONT abnormal</td>
<td>MTI-CONT</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>• There is no gradation of power display.</td>
<td>Same as above</td>
<td>Same as above</td>
<td>Same as above</td>
</tr>
<tr>
<td></td>
<td>• Power display is not performed.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>• There is no gradation of speed display.</td>
<td>Same as above</td>
<td>Same as above</td>
<td>Same as above</td>
</tr>
<tr>
<td></td>
<td>• Speed display is not performed</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

If any of the above phenomena occur, the cause may be the following:

(1) LB RAM read/write abnormal
(2) Initial value subtraction abnormal
(3) MTI-CONT control unit abnormal

(c) CAL Test Patterns 2 and 3 (for checking the DSC interpolation and threshold)

These test patterns are omitted as they are for checking the θ-direction interpolation, r-direction interpolation, θ-direction threshold and r-direction threshold value.
4.7.5 Supplement

Appended illustrations

CAL Test Pattern (Visual)

BDF  L, M, H  However, in case of H on MDF, character
MDF  M, H   "SPVY" is not displayed.)

(For BDF, MDF)

Letter to be within raster.
LB Test Pattern (Visual)

BDF  L, M, H
MDF  M, H

(For BDF, MDF) (Except when alternating rate.)

Note: All values of dispersion, power, etc. represent gradations.
4.8 Maintenance

Maintenance is not part of the test, but is used to support the test.

Initial operation:

Enter [8], at the stage shown in photo 3.3-1-3. The screen shown in figure 4.8-1 appears.

This maintenance menu includes the following menus: the CHECK SUM menu for registering the check sum value of the ROM directly controlled by the CPU, the PWB REVISION menu for displaying the revision of the PWB used currently for the system, and the SYSTEM SETUP menu for DIP SW settings by the software for initialization.

When [4] is selected and is pressed on the screen shown in figure 4.8-1, the system returns to the screen shown in photo 3.3-1-3.
Please wait for about 1 minute.
(Now registration of check-sum is executing.)

Figure 4.8-2

[No. 1] CHECK SUM

On the menu shown in figure 4.8-1, enter [1], and the maintenance procedure described below is performed.

Purpose/outline:

The check sum value for the ROM containing the programs of the CPU (host) is registered. The CPU ROM check described in No. 2 of subsection 4.1.3 will fail without this registration.

In addition to this registration, the check sum value for "self-diagnoses" is also registered simultaneously.

Procedure:

Press [1] on the menu shown in figure 4.8-1. The screen message shown in figure 4.8-2 is displayed during execution. It takes approximately one minute to complete this step of the maintenance. After completion, the screen returns to that shown in photo 3.3-1-3 automatically.
When [Z] is entered on the menu in figure 4.8-1, PWB REVISION is executed as shown below.

**Purpose/outline:**
Displays the revision of each PWB used in the system.

**Procedure:**
When [2] is pressed while the menu in figure 4.8-1 is displayed, PWB revisions are displayed. Figure 4.8-3 shows an example of this.

When (BS) is pressed, the system returns to the screen in figure 4.8-1.

---

**Table: PWB REVISION**

<table>
<thead>
<tr>
<th>PWB NAME</th>
<th>CPU/P-IF/STC</th>
<th>RPO/TR CONT</th>
<th>ECG/NFADS</th>
<th>B&amp;W DSC</th>
<th>COLOR DSC</th>
<th>IMAGE MEM</th>
<th>RGB/CONV</th>
<th>ENC/DEC</th>
<th>MTT CONT</th>
<th>FFT AUDIO</th>
<th>MECHA CONT</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>E F E F</td>
<td>E F F F</td>
<td>O O O</td>
<td>F D E</td>
<td>E D E</td>
<td>F C E</td>
<td>F F F</td>
<td>F F F</td>
<td>E F F F</td>
<td>F F F F</td>
<td>F F F F</td>
</tr>
</tbody>
</table>

**Figure 4.8-3**
[No. 3] SYSTEM SETUP

When [3] is pressed on the menu shown in figure 4.8-1, the following settings are executed.

Purpose/outline:
DIP SW3, DIP SW5, and DIP SW6 are set by the software. By these settings, EEPROM INITIALIZE processing can be started when the system is started.

Procedure:
While the menu shown in figure 4.8-4 is displayed,

When [1] is pressed, DIP SW3 can be set ON/OFF.

When [2] is pressed, DIP SW5 can be set ON/OFF.

When [3] is pressed, DIP SW6 can be set ON/OFF.

When [4] is pressed, all DIP SWs can be set to ON.

When [5] is pressed, all DIP SWs can be set to OFF.

When [6] is pressed on the screen shown in figure 4.8-4, the screen returns to the screen shown in figure 4.8-1.

After the above dip switches are set, EEPROM initialization should be performed by turning the power OFF and then ON again or by resetting the software using the CPU RESET SW on the rear panel.
Supplement:

If one of DIP SW3, DIP SW5, and DIP SW6 on the CPU PWB is set to ON, DIP SW setting by the software is invalid.

DIP SW setting by the software is automatically set to OFF if EEPROM INITIALIZE processing is executed or interrupted.
5. **APPENDIX**

5.1 Error Codes for Self-diagnosis

Explanations up to now have concerned only test systems which are activated by service personnel.

In the SSA-340A in addition to the above test systems, other built-in test systems are provided in the equipment. These test systems monitor the ultrasound system constantly, and whenever an error occurs, a corresponding message is indicated (self-diagnosis).

The messages mentioned above are described in the service manual for the equipment. However, they are also attached here for reference. (Table 5.1-1)
### Table 5.1-1 Error messages for self-diagnostic tests

<table>
<thead>
<tr>
<th>Check item</th>
<th>Purpose of test (nature of check)</th>
<th>Message displayed (error code)</th>
<th>Judge-ment</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>RAM CHECK</td>
<td>Confirmation of RAM operation for CPU programs [The CPU writes data into RAM and reads the same data, then performs checking by comparing the two.]</td>
<td>Abnormal: &quot;ERR = 50&quot;</td>
<td>CPU</td>
<td>Activated once when power is turned ON.</td>
</tr>
<tr>
<td>ROM CHECK</td>
<td>Confirmation of ROM operation for CPU programs [ROM data are added and compared with data added and stored previously, and checking is performed by comparing the two.]</td>
<td>Abnormal: &quot;ERR = 51&quot;</td>
<td>CPU</td>
<td></td>
</tr>
<tr>
<td>GDC FIFO CHECK</td>
<td>When the power is ON and FIFO is not empty, the LED on the CPU PWB lights.</td>
<td>Abnormal: The LED 0 on the CPU PWB lights.</td>
<td>CPU</td>
<td>Incorporating into the Host CPU software as a test routine.</td>
</tr>
<tr>
<td>ERROR CODE</td>
<td>Refer to table 5.1-2.</td>
<td>Same as left</td>
<td>CPU</td>
<td></td>
</tr>
<tr>
<td>ERROR MESSAGE</td>
<td>Refer to table 5.1-3.</td>
<td>Same as left</td>
<td>CPU</td>
<td></td>
</tr>
</tbody>
</table>
Table 5.1-2 Table of error codes

The host CPU detects errors and outputs error codes and messages.

If an error code appears on the monitor, find it in the following list:

<table>
<thead>
<tr>
<th>Error code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>5200</td>
<td>The local CPU of the monochrome DSC generated an interrupt but the host CPU did not receive it.</td>
</tr>
<tr>
<td>5201</td>
<td>No FI interrupt from the PANEL I/F section on the CPU PWB in calculation of TR delay time.</td>
</tr>
<tr>
<td>5202</td>
<td>The local CPU of the ECG/NONFADE board generated an interrupt but the host CPU did not receive it.</td>
</tr>
<tr>
<td>5204</td>
<td>The host CPU failed to access the C-RAM in the monochrome DSC.</td>
</tr>
<tr>
<td>5205</td>
<td>The host CPU failed to access the C-RAM in the color DSC.</td>
</tr>
<tr>
<td>5206</td>
<td>Undefined probe ID detected by the host CPU.</td>
</tr>
<tr>
<td>5208</td>
<td>The local CPU of the COLOR DSC generated an interrupt but the host CPU did not receive it.</td>
</tr>
<tr>
<td>5209</td>
<td>The host CPU failed to access the C-RAM in the FFT/CONT/AUDIO board.</td>
</tr>
<tr>
<td>5215</td>
<td>The host CPU received no OF interrupt from the RPG section on RPG/TRCONT board after sending OF RESET information to the RPG section.</td>
</tr>
<tr>
<td>5218</td>
<td>The host CPU received no OF interrupt from the RPG section before sending TR OFF information to the T/R CONT section on the RPG/TRCONT PWB in freeze on mode.</td>
</tr>
<tr>
<td>5219</td>
<td>The host CPU received no OF interrupt from the RPG section on the RPG/TRCONT PWB before erasing frame memory.</td>
</tr>
<tr>
<td>5223</td>
<td>The host CPU received no OF interrupt from the RPG section on the RPG/TRCONT PWB when it expected the interrupt.</td>
</tr>
<tr>
<td>5224</td>
<td>The host CPU received no OF interrupt (or ECG OF interrupt during ECG SYNC) from the RPG section on the RPG/TRCONT PWB when the freeze switch was pressed during recording in B-LOOP image memory mode.</td>
</tr>
<tr>
<td>5225</td>
<td>The host CPU received no OF interrupt from the RPG section on the RPG/TRCONT while re-recording images in image memory.</td>
</tr>
<tr>
<td>5226</td>
<td>The host CPU received no OF interrupt from the RPG section on the RPG/TRCONT when the image memory is to be erased.</td>
</tr>
<tr>
<td>5450</td>
<td>The host CPU failed to access the C-RAM on the ECG/NONFADE board.</td>
</tr>
</tbody>
</table>
Table 5.1-3 Table of error messages

<table>
<thead>
<tr>
<th>Error message</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>EEPROM CHECK ERROR</td>
<td>Writing in EEPROM for check does not end within 2.5 seconds.</td>
</tr>
<tr>
<td>EEPROM INIT ERROR</td>
<td>EEPROM is not ready to be written (at power on).</td>
</tr>
<tr>
<td>EEPROM WRITE ERROR</td>
<td>Writing in EEPROM does not end within 2.5 seconds after write operation completed.</td>
</tr>
<tr>
<td>TR ERROR ..........</td>
<td>The high voltage falls below a preset limit due to a fault in the TR circuitry.</td>
</tr>
</tbody>
</table>
5.2 Patch Menu Operation

5.2.1 Applicable equipment

SSA-340A

5.2.2 Starting

Important notice:

This starting procedure is for authorized personnel only (for software protection). This procedure must not be disclosed to the user.

(1) SETTING menu, SERVICE >
    ↓
    On the full-keyboard SHIFT, <
    ↓
    Also start with the SERVICE menu, by pressing PATCH.

(2) The PATCH MENU is displayed.

<table>
<thead>
<tr>
<th>PATCH MENU</th>
</tr>
</thead>
<tbody>
<tr>
<td>HIT (1 - 4) KEY</td>
</tr>
</tbody>
</table>

1. MEMORY R/W & DUMP
   To write data (e.g., a test pattern) to a desired memory port

2. COORDINATE CHECK (X, Y)
   To display a point at a desired set of coordinates in graphic memory for coordinate checking

3. IMAGE-CONT EXTERNAL VALUE SET
   Turns off control from the IMAGE CONT and uses fixed values

4. ADDRESS & DATA VALUE SAVE
   To write data to up to 20 ports

(3) To select a patch item from the PATCH menu, press the number key on the full-keyboard. See 5.2.3 to 5.2.6 for descriptions of patch items 1 to 4.

(4) Quit with the SERVICE menu, by pressing PATCH.

Notes:

1. Data set in the PATCH menu cannot be cleared with a CONDITION PRESET operation.

2. Data set in the PATCH menu can be cleared by a NEW PATIENT operation.
5.2.3 Memory R/W & dump

(1) When "1" is entered in the PATCH menu, the following menu is displayed:

<table>
<thead>
<tr>
<th>HIT</th>
<th>1 - 4</th>
<th>KEY</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. I/O READ</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2. I/O WRITE</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3. HEX DUMP</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4. LISTOUT (HEX &amp; ASCII)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(2) To select a desired item from this menu, enter the number (or "R" for item 1, or "W" for item 2) on the full-keyboard.

(3) Functions of the other keys with this menu

(a) [5] key
When this key is pressed, this menu ends and the PATCH menu (see 5.2.2 (2)) is redisplayed.

(b) [→] key
When this key is pressed, the address is increased by two.

(c) [←] key
When this key is pressed, the address is decreased by two.

(d) [↑] key
When this key is pressed, the address is increased by 256.

(e) [↓] key
When this key is pressed, the address is decreased by 256.
5.2.4 Coordinate check (X,Y)

(1) Data to be entered in this menu

(a) X = X coordinate
(b) Y = Y coordinate
(c) X-DOT = Number of dots in the X direction
(d) Y-DOT = Number of dots in the Y direction

Data items (a), (b), (c), and (d) change in that order each time the [CR] key is pressed.

(2) Press the [S] key to terminate operations for this menu and to redisplay the PATCH menu (see 5.2.2 (2)).

5.2.5 Image cont external value set

(1) When "3" is entered in the PATCH menu, the following menu is displayed:

<table>
<thead>
<tr>
<th>ADDRESS</th>
<th>DATA</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. ( )</td>
<td>( )</td>
</tr>
<tr>
<td>2. ( )</td>
<td>( )</td>
</tr>
<tr>
<td>3. ( )</td>
<td>( )</td>
</tr>
<tr>
<td>4. ( )</td>
<td>( )</td>
</tr>
<tr>
<td>5. ( )</td>
<td>( )</td>
</tr>
<tr>
<td>6. ( )</td>
<td>( )</td>
</tr>
<tr>
<td>7. ( )</td>
<td>( )</td>
</tr>
<tr>
<td>8. ( )</td>
<td>( )</td>
</tr>
<tr>
<td>9. ( )</td>
<td>( )</td>
</tr>
<tr>
<td>10. ( )</td>
<td>( )</td>
</tr>
</tbody>
</table>
(2) Functions of the other keys in this menu

(a) [ENTER] key
Press this key after entering an address and data.

(b) [DEL] key
Press this key to delete all addresses and data.

(c) [SPACE] key
Press this key to delete one address and data value.

(d) [↑] key
Press this key to move the cursor up (from 10 to 1).

(e) [↓] key
Press this key to move the cursor down (from 1 to 10).

(3) PATCH MENU display by KEY IN "S". (Return to the status in 5.2.2 (2)).

(4) Data output timing

- IMAGE CONT EXTERNAL VALUE SET is selected in the PATCH menu.

Data is output before hardware-controlling I/O processing is performed.

("(PM3)" is displayed during execution of the program.)

(5) Turn off the PATCH menu. The PATCH program starts.

Note: To terminate processing, call up the PATCH menu again.
5.2.6 Address & data value save

(1) When "4" is entered in the PATCH menu, the following menu is displayed:

<table>
<thead>
<tr>
<th>ADDRESS</th>
<th>DATA</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>(    ) (    )</td>
</tr>
<tr>
<td>2.</td>
<td>(    ) (    )</td>
</tr>
<tr>
<td>3.</td>
<td>(    ) (    )</td>
</tr>
<tr>
<td>4.</td>
<td>(    ) (    )</td>
</tr>
<tr>
<td></td>
<td>...</td>
</tr>
<tr>
<td>17.</td>
<td>(    ) (    )</td>
</tr>
<tr>
<td>18.</td>
<td>(    ) (    )</td>
</tr>
<tr>
<td>19.</td>
<td>(    ) (    )</td>
</tr>
<tr>
<td>20.</td>
<td>(    ) (    )</td>
</tr>
</tbody>
</table>

(2) Functions of the other keys in this menu

(a) [ENTER] key

Press this key after entering an address and data.

(b) [DEL] key

Press this key to delete all addresses and data.

(c) [SPACE] key

Press this key to delete one address and data value.

(d) [↑] key

Press this key to move the cursor up (from 10 to 1).

(e) [↓] key

Press this key to move the cursor down (from 1 to 10).

(3) Display the PATCH MENU by KEY IN "S". (Return to the status in 5.2.2 (2).)

Note: The set data is saved in EEPROM and preserved, even after the power is turned OFF, until the EEPROM is initialized by using DIP SW3.
(4) Data output timing

- ADDRESS & DATA VALUE SAVE is selected in the PATCH menu.

Data is output after hardware-controlling I/O processing is performed ("PM4" is displayed during execution of the program).

(5) Turn off the PATCH menu. The PATCH program starts.

Note: To terminate processing, call up the PATCH menu again.